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## RX671 Group, RX65N/RX651 Group

### Differences Between the RX671 Group and the RX65N Group

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#### Summary

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX671 Group and RX65N Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 145-pin package version of the RX671 Group and the 177-pin package version of the RX65N Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware of the products in question.

#### Target Devices

RX671 Group and RX65N Group

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## 1. Comparison of Built-In Functions of RX671 Group and RX65N Group

A comparison of the built-in functions of the RX671 Group and RX65N Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is a comparison of built-in functions of RX671 Group and RX65N Group.

**Table 1.1 Comparison of Built-In Functions of RX671 Group and RX65N Group**

Function	RX65N		RX671
	Code Flash 1.0 MB or less	Code Flash more than 1.5 MB	
<a href="#">CPU</a>		●	
Operating mode		○	
<a href="#">Address space</a>		▲	
Resets		○	
<a href="#">Option-setting memory (OFSM)</a>		●	
Voltage detection circuit (LVDA)		○	
<a href="#">Clock generation circuit</a>		●	
Clock frequency accuracy measurement circuit (CAC)		○	
<a href="#">Low power consumption function</a>		●/■	
<a href="#">Battery backup function (VBATTB)</a>		●	
<a href="#">Register write protection function</a>		●	
<a href="#">Exception handling</a>		●	
<a href="#">Interrupt controller (ICUB): RX65N, (ICUE): RX671</a>		●/■	
<a href="#">Buses</a>		●/■	
Memory-protection unit (MPU)		○	
<a href="#">DMA controller (DMACa): RX65N, (DMACb): RX671</a>		●	
EXDMA controller (EXDMACa)		○	
Data transfer controller (DTCb)		○	
<a href="#">Event link controller (ELC)</a>		●	
<a href="#">I/O ports</a>		●	
<a href="#">Multi-function pin controller (MPC)</a>		●/■	
Multi-function timer pulse unit 3 (MTU3a)		○	
<a href="#">Port output enable 3 (POE3a)</a>		■	
16-bit timer pulse unit (TPUa)		○	
Programmable pulse generator (PPG)		○	
<a href="#">8-bit timer (TMR): RX65N, (TMRb): RX671</a>		●	
Compare match timer (CMT)		○	
Compare match timer W (CMTW)		○	
Realtime clock (RTCd)		○	
Watchdog timer (WDTA)		○	
Independent watchdog timer (IWDTa)		○	
Ethernet controller (ETHERC)	○		×
DMA controller for the ethernet controller (EDMACa)	○		×
<a href="#">USB 2.0 FS Host/Function module (USBb)</a>		●	
<a href="#">Serial communications interface (SCIg, SCli, SCIh): RX65N, (SCIk, SCIm, SCIh): RX671</a>		●	
Serial communications interface (RSCI)	×		○
I <sup>2</sup> C bus interface (RIICa)		○	
High-speed I <sup>2</sup> C bus interface (RIICHs)	×		○

Function	RX65N		RX671
	Code Flash 1.0 MB or less	Code Flash more than 1.5 MB	
CAN module (CAN)		○	
<a href="#">Serial peripheral interface (RSPIC): RX65N, (RSPID): RX671</a>		●	
Serial peripheral interface (RSPIA)	×		○
<a href="#">Quad serial peripheral interface (QSPI): RX65N, Quad SPI memory interface (QSPIX): RX671</a>		●	
CRC calculator (CRCA)		○	
Serial sound interface (SSIE)	×		○
SD host interface (SDHI)		○	
SD slave interfaces (SDSI)	○		×
Multimedia card interface (MMCIF)	○		×
Parallel data capture unit (PDC)	○		×
Graphic LCD controller (GLCDC)	×	○	×
2D drawing engine (DRW2D)	×	○	×
Remote control signal receiver (REMCa)		×	○
Capacitive touch sensing unit (CTSUA)		×	○
<a href="#">Boundary scan</a>		■	
AESa	○		×
RNG	○		×
Trusted Secure IP (TSIP)		○	
<a href="#">12-bit A/D converter (S12ADFa): RX65N, (S12ADFa): RX671</a>		■	
12-bit D/A converter (R12DAa)	○		×
Temperature sensor (TEMPS)		○	
<a href="#">Data operation circuit (DOCA): RX65N, (DOCA): RX671</a>		●	
<a href="#">RAM</a>		■	
<a href="#">Standby RAM</a>		■	
<a href="#">Flash memory (FLASH)</a>		▲/■	
<a href="#">Packages</a>		●/■	

○: Available, ×: Unavailable, ●: Differs due to added functionality, ▲: Differs due to change in functionality, ■: Differs due to removed functionality.

## 2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, **red text** indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, **red text** indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

### 2.1 CPU

Table 2.1 is a comparative overview of CPU, and Table 2.2 is a comparison of CPU registers.

**Table 2.1 Comparative Overview of CPU**

Item	RX65N	RX671
CPU	<ul style="list-style-type: none"> <li>• Maximum operating frequency: 120 MHz</li> <li>• 32-bit RX CPU (RXv2)</li> <li>• Minimum instruction execution time: One instruction per state (system clock cycle)</li> <li>• Address space: 4 GB, linear</li> <li>• Register set of the CPU                             <ul style="list-style-type: none"> <li>— General purpose: Sixteen 32-bit registers</li> <li>— Control: Ten 32-bit registers</li> <li>— Accumulator: Two 72-bit register</li> </ul> </li> <li>• Basic instructions: 75</li> <li>• Floating-point instructions: 11</li>   <li>• DSP instructions: 23</li>   <li>• Addressing modes: 11</li> <li>• Data arrangement                             <ul style="list-style-type: none"> <li>— Instructions: Little endian</li> <li>— Data: Selectable between little endian or big endian</li> </ul> </li> <li>• On-chip 32-bit multiplier: 32 × 32 → 64 bits</li> <li>• On-chip divider: 32 / 32 → 32 bits</li> <li>• Barrel shifter: 32 bits</li> </ul>	<ul style="list-style-type: none"> <li>• Maximum operating frequency: 120 MHz</li> <li>• 32-bit RX CPU (RXv3)</li> <li>• Minimum instruction execution time: One instruction per state (system clock cycle)</li> <li>• Address space: 4 GB, linear</li> <li>• Register set of the CPU                             <ul style="list-style-type: none"> <li>— General purpose: Sixteen 32-bit registers</li> <li>— Control: Ten 32-bit registers</li> <li>— Accumulator: Two 72-bit registers</li> </ul> </li> <li>• Basic instructions: 77</li> <li>• Single-precision floating point instructions: 11</li> <li>• DSP instructions: 23</li> <li>• Instructions for register bank save function: 2</li> <li>• Addressing modes: 11</li> <li>• Data arrangement                             <ul style="list-style-type: none"> <li>— Instructions: Little endian</li> <li>— Data: Selectable between little endian or big endian</li> </ul> </li> <li>• On-chip 32-bit multiplier: 32 × 32 → 64 bits</li> <li>• On-chip divider: 32 / 32 → 32 bits</li> <li>• Barrel shifter: 32 bits</li> </ul>
FPU	<ul style="list-style-type: none"> <li>• Single-precision floating point (32 bits)</li> <li>• Data types and floating-point exceptions conform to IEEE 754 standard</li> </ul>	<ul style="list-style-type: none"> <li>• Single-precision floating-point (32 bits)</li> <li>• Data types and floating-point exceptions conform to IEEE 754 standard</li> </ul>

Item	RX65N	RX671
Double-precision floating point coprocessor	—	<ul style="list-style-type: none"> <li>• Double-precision floating-point register set                             <ul style="list-style-type: none"> <li>— Double-precision floating-point data registers: 64-bit × 16</li> <li>— Double-precision floating-point control registers: 32-bit × 4</li> </ul> </li> <li>• Double-precision floating-point processing instructions: 21</li> <li>• Function for notifying the interrupt controller of double-precision floating-point exceptions</li> </ul>
Register bank save function	—	<ul style="list-style-type: none"> <li>• Fast collective saving and restoration of the values of CPU registers</li> <li>• 16 save register banks</li> </ul>

**Table 2.2 Comparison of CPU Registers**

Register	Bit	RX65N	RX671
DR0 to DR15	—	—	Double-precision floating-point data registers
DPSW	—	—	Double-precision floating-point status word
DCMR	—	—	Double-precision floating-point comparison result register
DECNT	—	—	Double-precision floating-point exception handling control register
DEPC	—	—	Double-precision floating-point exception program counter

## 2.2 Address Space

Figure 2.1 is a comparative memory map of single-chip mode, Figure 2.2 is a comparative memory map of on-chip ROM enabled extended mode, and Figure 2.3 is a comparative memory map of on-chip ROM disabled extended mode.

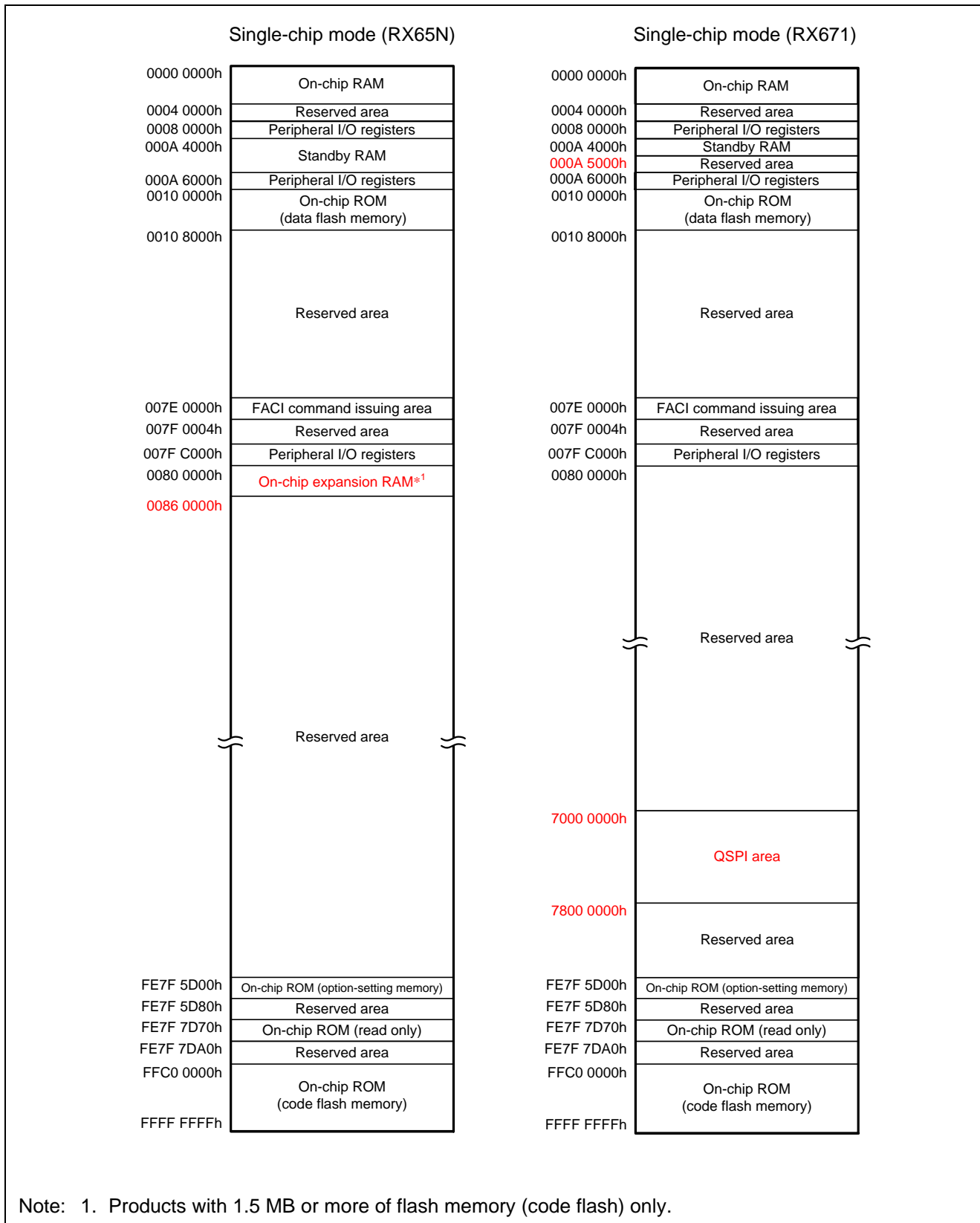
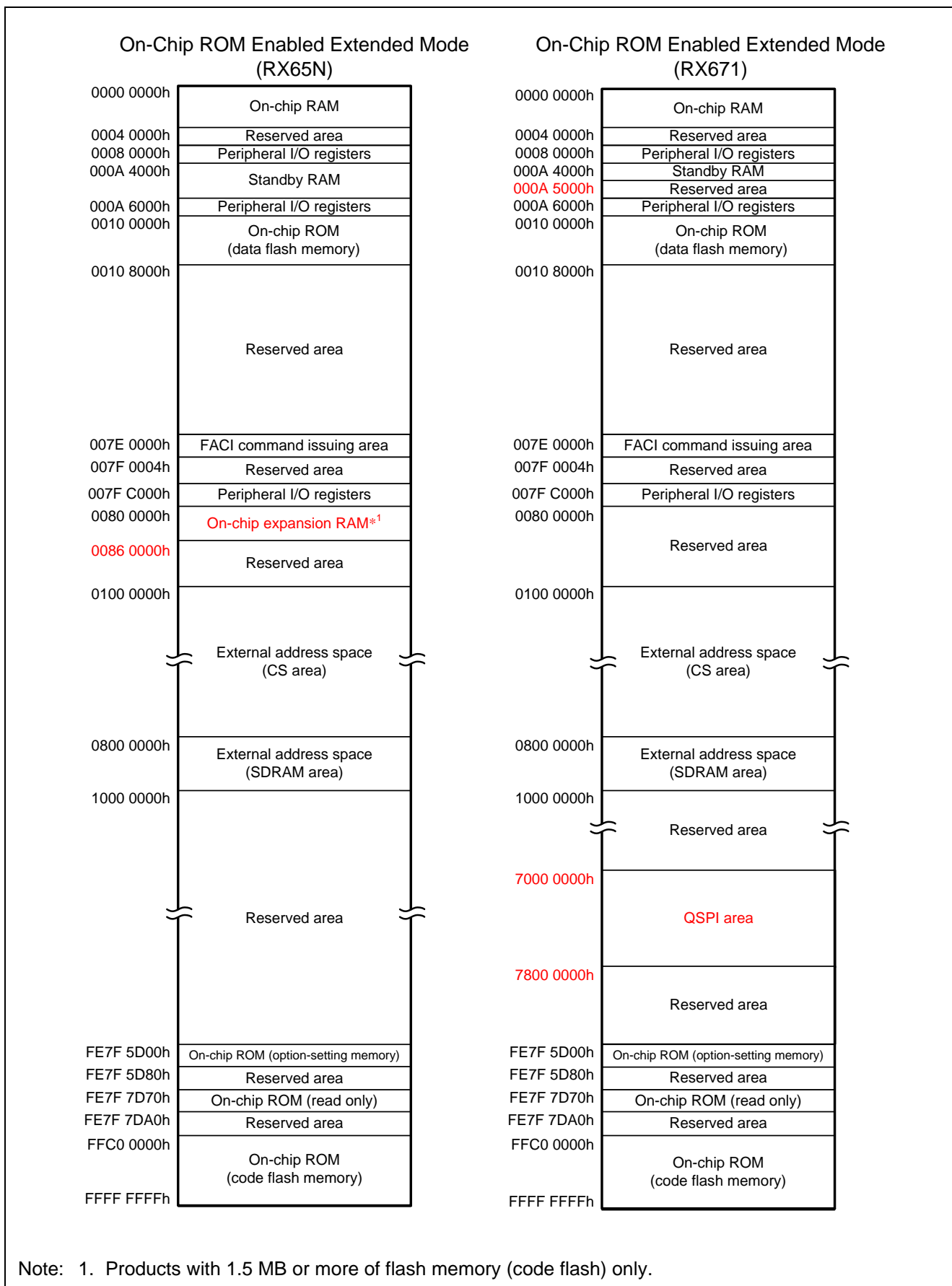


Figure 2.1 Comparative Memory Map of Single-Chip Mode





Note: 1. Products with 1.5 MB or more of flash memory (code flash) only.

Figure 2.2 Comparative Memory Map of On-Chip ROM Enabled Extended Mode

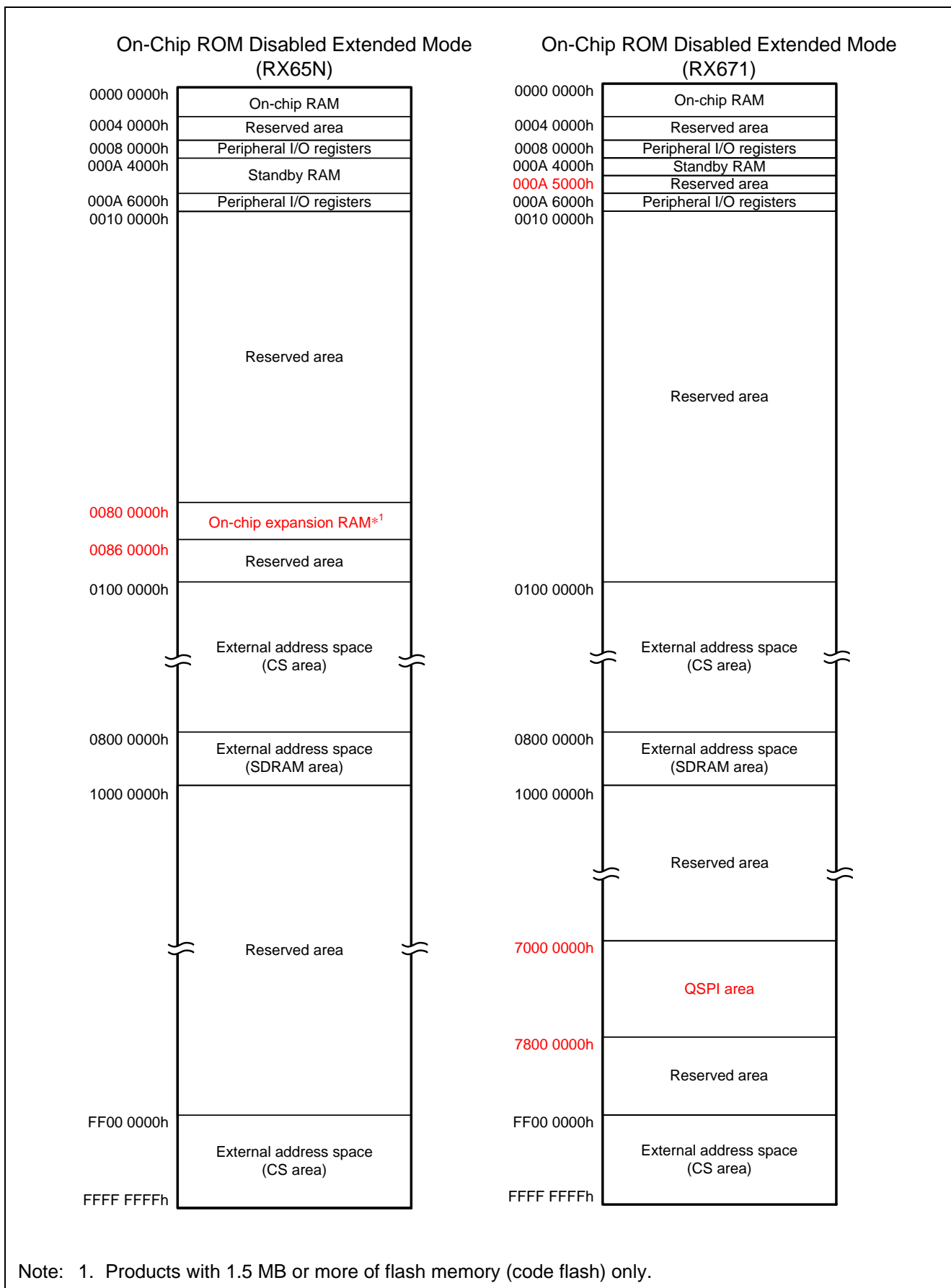


Figure 2.3 Comparative Memory Map of On-Chip ROM Disabled Extended Mode

### 2.3 Option-Setting Memory

Table 2.3 is a comparison of option-setting memory registers.

**Table 2.3 Comparison of Option-Setting Memory Registers**

Register	Bit	RX65N (OFSM)	RX671 (OFSM)
SPCC	OCDE	—	On-chip debugger connection enable bit

## 2.4 Clock Generation Circuit

Table 2.4 is a comparative overview of the clock generation circuits, and Table 2.5 is a comparison of clock generation circuit registers.

**Table 2.4 Comparative Overview of Clock Generation Circuits**

Item	RX65N	RX671
Use	<ul style="list-style-type: none"> <li>Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM.</li> <li>Generates the peripheral module clock (PCLKA) to be supplied to the <b>ETHERC</b>, <b>EDMAC</b>, RSPI, SCLi, MTU3, <b>AES*1</b>, <b>GLCDC*2</b>, and <b>DRW2D*2</b>.</li> <li>Generates the peripheral module clock (PCLKB) to be supplied to the peripheral modules.</li> <li>Generates the peripheral module clocks (for analog conversion) (PCLKC: unit 0; PCLKD: unit 1) to be supplied to the S12AD.</li> <li>Generates the flash-IF clock (FCLK) to be supplied to the flash interface.</li> <li>Generates the external bus clock (BCLK) to be supplied to the external bus.</li> <li>Generates the SDRAM clock (SDCLK) to be supplied to the SDRAM.</li> <li>Generates the USB clock (UCLK) to be supplied to the USBb.</li> <li>Generates the CAC clock (CACCLK) to be supplied to the CAC.</li> <li>Generates the CAN clock (CANMCLK) to be supplied to the CAN.</li> <li>Generates the RTC sub-clock (RTCSCCLK) to be supplied to the RTC.</li> <li>Generates the RTC main clock (RTCMCLK) to be supplied to the RTC.</li> <li>Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.</li> <li>Generates the JTAG clock (JTAGTCK) to be supplied to the JTAG.</li> </ul>	<ul style="list-style-type: none"> <li>Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, <b>QSPIX</b>, code flash memory, and RAM.</li> <li>Generates the peripheral module clock (PCLKA) to be supplied to the RSPI, <b>RSPIA</b>, SCLm, <b>RSCI</b>, MTU, and <b>RIICHS</b>.</li> <li>Generates the peripheral module clock (PCLKB) to be supplied to the peripheral modules.</li> <li>Generates the peripheral module clocks (for analog conversion) (ADCLK = PCLKC (unit 0), PCLKD (unit 1)) to be supplied to the S12AD.</li> <li>Generates the flash-IF clock (FCLK) to be supplied to the flash interface.</li> <li>Generates the external bus clock (BCLK) to be supplied to the external bus.</li> <li>Generates the SDRAM clock (SDCLK) to be supplied to the SDRAM.</li> <li>Generates the USB clock (UCLK) to be supplied to the USB.</li> <li>Generates the CAC clock (CACCLK) to be supplied to the CAC.</li> <li>Generates the CAN clock (CANMCLK) to be supplied to the CAN.</li> <li>Generates the RTC sub-clock (RTCSCCLK) to be supplied to the REMC.</li> <li>Generates the RTC main clock (RTCMCLK) to be supplied to the RTC.</li> <li>Generates the REMC sub-clock (REMSCLK) to be supplied to the REMC.</li> <li>Generates the VBATT clock (VBATCLK) to be supplied to the VBATT.</li> <li>Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.</li> <li>Generates the JTAG clock (JTAGTCK) to be supplied to the JTAG.</li> </ul>

Item	RX65N	RX671
Operating frequency	<ul style="list-style-type: none"> <li>• ICLK: 120 MHz (max.)</li> <li>• PCLKA: 120 MHz (max.)</li> <li>• PCLKB: 60 MHz (max.)</li> <li>• PCLKC: 60 MHz (max.)</li> <li>• PCLKD: 60 MHz (max.)</li> <li>• FCLK:                             <ul style="list-style-type: none"> <li>— 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory)*2)</li> <li>— 60 MHz (max.) (for reading from the data flash memory)*2</li> </ul> </li> <li>• BCLK: 120 MHz (max.)</li> <li>• BCLK pin output: 60 MHz (max.)</li> <li>• SDCLK pin output: 60 MHz (max.)</li> <li>• UCLK: 48 MHz (max.)</li>   <li>• CACCLK: Same as the clocks from the respective oscillators.</li> <li>• CANMCLK: 24 MHz (max.)</li> <li>• RTCSCCLK: 32.768 kHz</li> <li>• RTCMCLK: 8 MHz to 16 MHz</li>   <li>• IWDTCLK: 120 kHz</li> <li>• JTAGTCK: 10 MHz (max.)</li> </ul>	<ul style="list-style-type: none"> <li>• ICLK: 120 MHz (max.)</li> <li>• PCLKA: 120 MHz (max.)</li> <li>• PCLKB: 60 MHz (max.)</li> <li>• PCLKC: 60 MHz (max.)</li> <li>• PCLKD: 60 MHz (max.)</li> <li>• FCLK:                             <ul style="list-style-type: none"> <li>— 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory)</li> <li>— 60 MHz (max.) (for reading from the data flash memory)</li> </ul> </li> <li>• BCLK: 120 MHz (max.)</li> <li>• BCLK pin output: 60 MHz (max.)</li> <li>• SDCLK pin output: 60 MHz (max.)</li> <li>• UCLK: 48 MHz (max.)</li> <li>• <b>CLKOUT pin output: 40 MHz (max.)</b></li> <li>• CACCLK: Same as the clocks from the respective oscillators.</li> <li>• CANMCLK: 24 MHz (max.)</li> <li>• RTCSCCLK: 32.768 kHz</li> <li>• RTCMCLK: <b>1 kHz</b> to 16 MHz</li> <li>• <b>REMSCLK: 32.768 kHz</b></li> <li>• <b>VBATCLK: 32.768 kHz</b></li> <li>• IWDTCLK: 120 kHz</li> <li>• JTAGTCK: 10 MHz (max.)</li> </ul>
Main clock oscillator	<ul style="list-style-type: none"> <li>• Resonator frequency: 8 MHz to 24 MHz</li> <li>• External clock input frequency: 24 MHz (max.)</li> <li>• Connectable resonator or additional circuit: ceramic resonator, crystal resonator</li> <li>• Connection pins: EXTAL, XTAL</li> <li>• Oscillation stop detection function: When oscillation stop is detected on the main clock, the system clock source is switched to LOCO, and the MTU3 pin can be forcedly driven high-impedance.</li> </ul>	<ul style="list-style-type: none"> <li>• Resonator frequency: 8 MHz to 24 MHz</li> <li>• External clock input frequency: 24 MHz (max.)</li> <li>• Connectable resonator or additional circuit: ceramic resonator, crystal resonator</li> <li>• Connection pins: EXTAL, XTAL</li> <li>• Oscillation stop detection function: When oscillation stop is detected on the main clock, the system clock source is switched to LOCO, and the MTU pin can be forcedly driven high-impedance.</li> </ul>
Sub-clock oscillator	<ul style="list-style-type: none"> <li>• Resonator frequency: 32.768 kHz</li> <li>• Connectable resonator or additional circuit: crystal resonator</li> <li>• Connection pins: XCIN, XCOU</li> </ul>	<ul style="list-style-type: none"> <li>• Resonator frequency: 32.768 kHz</li> <li>• Connectable resonator or additional circuit: crystal resonator</li> <li>• Connection pins: XCIN, XCOU</li> </ul>

Item	RX65N	RX671
PLL frequency synthesizer	<ul style="list-style-type: none"> <li>Input clock sources: Main clock, HOCO</li> <li>Input pulse frequency division ratio: Selectable from <math>\times 1/1</math>, <math>\times 1/2</math>, and <math>\times 1/3</math></li> <li>Input frequency: 8 MHz to 24 MHz</li> <li>Frequency multiplication factor: Selectable from 10 to 30</li> <li>Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz</li> </ul>	<ul style="list-style-type: none"> <li>Input clock sources: Main clock, HOCO</li> <li>Input pulse frequency division ratio: Selectable from <math>\times 1/1</math>, <math>\times 1/2</math>, and <math>\times 1/3</math></li> <li>Input frequency: 8 MHz to 24 MHz</li> <li>Frequency multiplication factor: Selectable from 10 to 30</li> <li>Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz</li> </ul>
High-speed on-chip oscillator (HOCO)	<ul style="list-style-type: none"> <li>Oscillation frequency: Selectable among 16 MHz, 18 MHz, and 20 MHz</li> <li>HOCO power supply control</li> </ul>	<ul style="list-style-type: none"> <li>Oscillation frequency: Selectable among 16 MHz, 18 MHz, and 20 MHz</li> <li>HOCO power supply control</li> <li>FLL function</li> <li>Support for user trimming</li> </ul>
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 240 kHz	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 120 kHz	Oscillation frequency: 120 kHz
JTAG external clock input (TCK)	Input clock frequency: 10 MHz (max.)	Input clock frequency: 10 MHz (max.)
Control of output on BCLK pin	<ul style="list-style-type: none"> <li>Selectable between BCLK clock output and high output</li> <li>Selectable between BCLK and BCLK <math>\times 1/2</math></li> </ul>	<ul style="list-style-type: none"> <li>Selectable between BCLK clock output and high output</li> <li>Selectable between BCLK and BCLK <math>\times 1/2</math></li> </ul>
Control of output on SDCLK pin	Selectable between SDCLK clock output and high output SDCLK	Selectable between SDCLK clock output and high output SDCLK
Event link function (output)	Detection of stopping of the main clock oscillator	Detection of stopping of the main clock oscillator
Event link function (input)	Switching of the clock source to the low-speed on-chip oscillator	Switching of the clock source to the low-speed on-chip oscillator

Notes: 1. Implemented only on products with a code flash memory capacity of 1 MB or less.

2. Implemented only on products with a code flash memory capacity of 1.5 MB or more.

**Table 2.5 Comparison of Clock Generation Circuit Registers**

Register	Bit	RX65N	RX671
PLLCR	PLLSRCSEL	PLL Clock Source Select* <sup>1</sup> 0: Main clock oscillator 1: HOCO	PLL Clock Source Select 0: Main clock oscillator 1: HOCO* <sup>2</sup>
ROMWT	ROMWT[1:0]	ROM wait cycle setting bits  b1 b0 0 0: 0 wait cycles 0 1: 1 wait cycle <b>1 0: 2 wait cycles</b>  Settings other than the above are prohibited.	ROM wait cycle setting bits  b1 b0 0 0: 0 wait cycles 0 1: 1 wait cycle  Settings other than the above are prohibited.
CKOCR	—	—	CLKOUT output control register
SOSCCR2	—	—	Sub-clock oscillator control register 2
BKSCCR	—	—	Backup area sub-clock control register
FLLCR1	—	—	FLL control register 1
FLLCR2	—	—	FLL control register 2
HOCOTRRn	—	—	High-speed on-chip oscillator trimming register n (n = 0 to 2)

Note: 1. Set this bit to 0 when using the USB.

Note: 2. When using USB, be sure to enable the FLL function.

## 2.5 Low Power Consumption

Table 2.6 is a comparison of procedures for entering and exiting low power consumption modes and operating states in each mode, and Table 2.7 is a comparison of low power consumption registers.

**Table 2.6 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode**

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX65N	RX671
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM and expansion RAM: RX65N RAM: RX671	Operation possible (retained)	Operation possible (retained)
	Standby RAM	Operation possible (retained)	Operation possible (retained)
	Flash memory	Operation	Operation
	USB 2.0 Host/Function module (USBb)	Operation possible	Operation possible
	Watchdog timer (WDTA)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Operation possible	Operation possible
	Port output enable (POE)	Operation possible	Operation possible
	Remote control signal receiver (REMC)	—	Operation possible
	Voltage detection circuit (LVDA)	Operation possible	Operation possible
Power-on reset circuit	Operation	Operation	
Other peripheral modules	Operation possible	Operation possible	
I/O ports	Operation	Operation	
All-module clock stop mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)



Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX65N	RX671
All-module clock stop mode	RAM and expansion RAM: RX65N RAM: RX671	Stopped (retained)	Stopped (retained)
	Standby RAM	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	USB 2.0 Host/Function module (USBb)	Stopped	Stopped
	Watchdog timer (WDTA)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Operation possible	Operation possible
	Port output enable (POE)	Operation possible*1	Operation possible*1
	Remote control signal receiver (REMC)	—	Operation possible
	Voltage detection circuit (LVDA)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Other peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	retained	retained
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM and expansion RAM: RX65N RAM: RX671	Stopped (retained)	Stopped (retained)
	Standby RAM	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	USB 2.0 Host/Function module (USBb)	Stopped	Stopped
	Watchdog timer (WDTA)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Stopped (retained)	Stopped (retained)
	Port output enable (POE)	Stopped (retained)	Stopped (retained)
	Remote control signal receiver (REMC)	—	Operation possible
	Voltage detection circuit (LVDA)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Other peripheral modules	Stopped (retained)	Stopped (retained)
I/O ports	Retained	Retained	

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX65N	RX671
Deep software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (reset processing)	Program execution state (reset processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Stopped (undefined)	Stopped (undefined)
	PLL	Stopped	Stopped
	CPU	Stopped (undefined)	Stopped (undefined)
	RAM and expansion RAM: RX65N RAM: RX671	Stopped (undefined)	Stopped (undefined)
	Standby RAM	Stopped (retained/undefined)	Stopped (retained/undefined)
	Flash memory	Stopped (retained)	Stopped (retained)
	USB 2.0 Host/Function module (USBb)	Stopped (retained/undefined)	Stopped (retained/undefined)
	Watchdog timer (WDTA)	Stopped (undefined)	Stopped (undefined)
	Independent watchdog timer (IWDT)	Stopped (undefined)	Stopped (undefined)
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Stopped (undefined)	Stopped (undefined)
	Port output enable (POE)	Stopped (undefined)	Stopped (undefined)
	Remote control signal receiver (REMC)	—	Operation possible
Voltage detection circuit (LVDA)	Operation possible	Operation possible	
Power-on reset circuit	Operation	Operation	
Other peripheral modules	Stopped (undefined)	Stopped (undefined)	
I/O ports	Retained	Retained	

Notes: “Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.

“Stopped (retained)” means that internal register values are retained and internal operations are suspended.

“Stopped (undefined)” means that internal register values are undefined and power is not supplied to the internal circuit.

1. If POE interrupts are enabled and a POE interrupt source occurs while the chip is in all-module clock stop mode, return from all-module clock stop mode does not occur but the state of the interrupt source flag is retained. If a different source initiates return from all-module clock stop mode in this state, the POE interrupt is generated after the return.

**Table 2.7 Comparison of Low Power Consumption Registers**

Register	Bit	RX65N	RX671
MSTPCRA	MSTPA19	12-bit D/A converter module stop bit	—
MSTPCRB	MSTPB15	Ethernet controller and Ethernet controller DMA controller (channel 0) modules stop bit	—
	MSTPB18	—	USB 2.0 FS interface 1 module stop bit* <sup>1</sup>
	MSTPB22	Parallel data capture unit module stop bit	—
MSTPCRC	MSTPC2	Expansion RAM module stop bit	—
	MSTPC23	Quad serial peripheral interface module stop bit	—
	MSTPC28	2D drawing engine module stop bit	—
	MSTPC29	Graphic-LCD controller module stop bit	—
MSTPCRD	—	Module stop control register D <b>Initial value after a reset differs.</b>	Module stop control register D
	MSTPD0	Module stop D0 bit	—
	MSTPD1	Module stop D1 bit	<b>Quad SPI memory interface</b> module stop bit
	MSTPD2	Module stop D2 bit	<b>Serial communications interface 11</b> module stop bit
	MSTPD3	Module stop D3 bit	<b>Serial communications interface 10</b> module stop bit
	MSTPD4	Module stop D4 bit	—
	MSTPD5	Module stop D5 bit	<b>High-speed I<sup>2</sup>C bus interface</b> module stop bit
	MSTPD6	Module stop D6 bit	—
	MSTPD7	Module stop D7 bit	<b>Remote control signal receiver</b> module stop bit
	MSTPD12	—	Capacitive touch sensing unit module stop bit
	MSTPD13	SD slave interface module stop bit	—
	MSTPD15	—	Serial sound interface 0 module stop bit
	MSTPD21	MMC host interface module stop bit	—
	MSTPD26	—	Serial peripheral interface module stop bit
	DPSIER3	DRMCIE	—
DPSIER3	DTADIE	—	VBATT tamper detection deep standby cancel signal enable bit
DPSIFR3	DRMCIF	—	Deep standby cancel by REMC interrupt flag
	DTADIF	—	VBATT tamper detection deep standby cancel flag
DPSBK <sub>Ry</sub>	—	Deep standby backup register y (y = 0 to 31)	—

Note: 1. To transition to software standby mode after overwriting the MSTPB18 bit, issue a WAIT instruction once two cycles of the USB clock (UCLK) have elapsed after the MSTPB18 bit was overwritten.

## 2.6 Battery Backup Function

Table 2.8 is a comparative overview of the battery backup functions, and Table 2.9 is a comparison of battery backup function registers.

**Table 2.8 Comparative Overview of Battery Backup Functions**

Item	RX65N	RX671 (VBATTB)
Backup target	<ul style="list-style-type: none"> <li>Sub-clock oscillator</li> <li>Realtime clock (RTC)</li> </ul>	All modules in the backup area <ul style="list-style-type: none"> <li>Backup register</li> <li>Sub-clock oscillator</li> <li>Power-down detection circuit</li> <li>Tamper detection circuit</li> <li>Realtime clock (RTC)</li> </ul>
Backup register	—	128 bytes Can be erased immediately when tamper detection occurs.
Backup area power-down detection	—	Generates a backup area reset signal when the power supply voltage to the backup area drops.
Tamper event detection	—	Detects unauthorized access to the system, and provides notification by setting a flag or generating an interrupt. <ul style="list-style-type: none"> <li>A timestamp can be obtained when tamper detection occurs.</li> <li>Tamper input pins: 3 (TAMPI0 to TAMPI2)</li> <li>Built-in noise filter (sampling rate: 32.768 kHz, three-match detection)</li> <li>Can be used as a source for triggering return from deep software standby mode.</li> </ul>

**Table 2.9 Comparison of Battery Backup Function Registers**

Register	Bit	RX65N	RX671 (VBATTB)
BKPSR	—	—	Backup area power supply status register
TAMPSR	—	—	Tamper status register
TAMPCR	—	—	Tamper control register
TCECR	—	—	Time capture event control register
TAMPICR1	—	—	Tamper/RTCIC input control register 1
TAMPICR2	—	—	Tamper/RTCIC input control register 2
TAMPIMR	—	—	Tamper/RTCIC input monitor register
BKRn	—	—	Backup register n (n = 0 to 127)

## 2.7 Register Write Protection Function

Table 2.10 is a comparative overview of the register write protection functions.

**Table 2.10 Comparative Overview of Register Write Protection Functions**

Item	RX65N	RX671
PRC0 bit	Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOGR, HOCOGR2, OSTDCR, OSTDSR	Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOGR, HOCOGR2, OSTDCR, OSTDSR, <b>CKOCR, FLLCR1, FLLCR2, HOCOTRR0, HOCOTRR1, HOCOTRR2, CTSUTRMR</b>
PRC1 bit	<ul style="list-style-type: none"> <li>Registers related to the operating modes: SYSCR0, SYSCR1</li> <li>Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR3</li> <li>Registers related to the clock generation circuit: MOSCWTCR, SOSCWTCR, MOFCR, HOCOPCR</li> <li>Software reset register: SWRR</li> </ul>	<ul style="list-style-type: none"> <li>Registers related to the operating modes: SYSCR0, SYSCR1</li> <li>Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR3</li> <li>Registers related to the clock generation circuit: MOSCWTCR, SOSCWTCR, MOFCR, HOCOPCR</li> <li>Software reset register: SWRR</li> <li><b>Registers related to battery backup: BKSCCR, BKPSR, SOSCCR2, TAMPSR, TAMPCR, TCECR, TAMPICR1, TAMPICR2, TAMPIMR</b></li> </ul>
PRC3 bit	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

## 2.8 Exception Handling

Table 2.11 is a comparative overview of exception handling, Table 2.12 is a comparative listing of vector tables, and Table 2.13 is a comparative listing of return from exception handling routine instructions.

**Table 2.11 Comparative Overview of Exception Handling**

Item	RX65N	RX671
Exception events	<ul style="list-style-type: none"> <li>• Undefined instruction exception</li> <li>• Privileged instruction exception</li> <li>• Access exception</li>   <li>• Floating-point exception</li> <li>• Reset</li> <li>• Non-maskable interrupt</li> <li>• Interrupt</li> <li>• Unconditional trap</li> </ul>	<ul style="list-style-type: none"> <li>• Undefined instruction exception</li> <li>• Privileged instruction exception</li> <li>• Access exception</li> <li>• <b>Address exception</b></li> <li>• Single-precision floating-point exception</li> <li>• Reset</li> <li>• Non-maskable interrupt</li> <li>• Interrupt</li> <li>• Unconditional trap</li> </ul>

**Table 2.12 Comparative Listing of Vector Tables**

Item	RX65N	RX671	
Undefined instruction exception	Exception vector table (EXTB)	Exception vector table (EXTB)	
Privileged instruction exception	Exception vector table (EXTB)	Exception vector table (EXTB)	
Access exception	Exception vector table (EXTB)	Exception vector table (EXTB)	
Address exception	—	<b>Exception vector table (EXTB)</b>	
Floating-point exception (RX65N)/ single-precision floating-point exception (RX671)	Exception vector table (EXTB)	Exception vector table (EXTB)	
Reset	Exception vector table (EXTB)	Exception vector table (EXTB)	
Non-maskable interrupt	Exception vector table (EXTB)	Exception vector table (EXTB)	
Interrupt	Fast interrupt	FINTV	FINTV
	Other than fast interrupt	Interrupt vector table (INTB)	Interrupt vector table (INTB)
Unconditional trap	Interrupt vector table (INTB)	Interrupt vector table (INTB)	

**Table 2.13 Comparative Listing of Return from Exception Handling Routine Instructions**

Item	RX65N	RX671	
Undefined instruction exception	RTE	RTE	
Privileged instruction exception	RTE	RTE	
Access exception	RTE	RTE	
Address exception	—	<b>RTE</b>	
Floating-point exception (RX65N)/ single-precision floating-point exception (RX671)	RTE	RTE	
Reset	Return not possible	Return not possible	
Non-maskable interrupt	Prohibited	Prohibited	
Interrupt	Fast interrupt	RTFI	RTFI
	Other than fast interrupt	RTE	RTE
Unconditional trap	RTE	RTE	

## 2.9 Interrupt Controller

Table 2.14 is a comparative overview of the interrupt controllers, and Table 2.15 is a comparison of interrupt controller registers.

**Table 2.14 Comparative Overview of Interrupt Controllers**

Item		RX65N (ICUB)	RX671 (ICUE)
Interrupts	Peripheral function interrupts	<p>Interrupts from peripheral modules</p> <ul style="list-style-type: none"> <li>• Interrupt detection method: Edge detection/level detection (fixed for each interrupt source)</li> <li>• Group interrupt: Multiple interrupt sources are grouped together and treated as a single interrupt source.                             <ul style="list-style-type: none"> <li>— Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection)</li> <li>— Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection)</li> <li>— Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection)</li> </ul> </li> <li>• Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207.</li> <li>• Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.</li> </ul>	<p>Interrupts from peripheral modules</p> <ul style="list-style-type: none"> <li>• Interrupt detection method: Edge detection/level detection (fixed for each interrupt source)</li> <li>• Group interrupt: Multiple interrupt sources are grouped together and treated as a single interrupt source.                             <ul style="list-style-type: none"> <li>— Group IE0 interrupt: Interrupt sources of coprocessors that use ICLK as the operating clock (edge detection)</li> <li>— Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection)</li> <li>— Group BL0/BL1 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection)</li> <li>— Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection)</li> </ul> </li> <li>• Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207.</li> <li>• Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.</li> </ul>

Item		RX65N (ICUB)	RX671 (ICUE)
Interrupts	External pin interrupts	Interrupts by input signals on IRQ <sub>i</sub> pins (i = 0 to 15) <ul style="list-style-type: none"> <li>Interrupt detection: Ability to set as source detection of low level, falling edge, rising edge, or rising and falling edges</li> <li>A digital filter can be used to remove noise.</li> </ul>	Interrupts by input signals on IRQ <sub>i</sub> pins (i = 0 to 15) <ul style="list-style-type: none"> <li>Interrupt detection: Ability to set as source detection of low level, falling edge, rising edge, or rising and falling edges</li> <li>A digital filter can be used to remove noise.</li> </ul>
	Software interrupts	<ul style="list-style-type: none"> <li>An interrupt request can be generated by writing to a register.</li> <li>Number of sources: 2</li> </ul>	<ul style="list-style-type: none"> <li>An interrupt request can be generated by writing to a register.</li> <li>Number of sources: 2</li> </ul>
	Interrupt priority	The priority level is set by writing to interrupt source priority register r (IPRr) (r = 000 to 255).	The priority level is set by writing to interrupt source priority register r (IPRr) (r = 000 to 255).
	Fast interrupt function	The CPU's interrupt response time can be reduced. This setting can be used for one interrupt source only.	The CPU's interrupt response time can be reduced. This setting can be used for one interrupt source only.
	DTC/DMAC control	Interrupt sources can be used to start the DTC and DMAC.	Interrupt sources can be used to start the DTC and DMAC.
	EXDMAC control	<ul style="list-style-type: none"> <li>An interrupt selected by software configurable interrupt B source select register 144 or software configurable interrupt A source select register 208 can be used to start EXDMAC0.</li> <li>An interrupt selected by software configurable interrupt B source select register 145 or software configurable interrupt A source select register 209 can be used to start EXDMAC1.</li> </ul>	<ul style="list-style-type: none"> <li>An interrupt selected by software configurable interrupt B source select register 144 or software configurable interrupt A source select register 208 can be used to start EXDMAC0.</li> <li>An interrupt selected by software configurable interrupt B source select register 145 or software configurable interrupt A source select register 209 can be used to start EXDMAC1.</li> </ul>
Non-maskable interrupts	NMI pin interrupt	Interrupt by the input signal on the NMI pin <ul style="list-style-type: none"> <li>Interrupt detection: Falling edge or rising edge</li> <li>Digital filter can be used to remove noise.</li> </ul>	Interrupt by the input signal on the NMI pin <ul style="list-style-type: none"> <li>Interrupt detection: Falling edge or rising edge</li> <li>Digital filter can be used to remove noise.</li> </ul>
	Oscillation stop detection interrupt	Interrupt occurs at detection of main clock oscillation having stopped.	Interrupt occurs at detection of main clock oscillation having stopped.
	WDT underflow/refresh error interrupt	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.
	IWDT underflow/refresh error interrupt	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.



Item		RX65N (ICUB)	RX671 (ICUE)
Non-maskable interrupts	Voltage monitoring 1 interrupt	Interrupt from voltage detection circuit 1 (LVD1)	Interrupt from voltage detection circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Interrupt from voltage detection circuit 2 (LVD2)	Interrupt from voltage detection circuit 2 (LVD2)
	RAM error interrupt	Interrupt occurs when a parity check error is detected in the RAM (including the expansion RAM).	Interrupt occurs when a parity check error is detected in the RAM.
	Double-precision floating-point exceptions	—	Exceptions from double-precision floating-point coprocessor
Return from low power consumption state	Sleep mode	Exit sleep mode by any interrupt source.	Exit sleep mode by any interrupt source.
	All-module clock stop mode	Exit all-module clock stop mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, USB resume, RTC alarm, RTC period, IWD, software configurable interrupt 146 to 157).	Exit all-module clock stop mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, USB0 resume, RTC alarm, RTC period, IWD, VBATT tamper detection, REMC interrupt, or software configurable interrupt 146 to 157).
	Software standby mode	Exit software standby mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period, IWD).	Exit software standby mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB0 resume, RTC alarm, RTC period, IWD, VBATT tamper detection, REMC interrupt).
	Deep software standby mode	Exit deep software standby mode by NMI pin interrupt, any among a subset of external pin interrupts, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period).	Exit deep software standby mode by NMI pin interrupt, any among a subset of external pin interrupts, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB0 resume, RTC alarm, RTC period, VBATT tamper detection, REMC interrupt).

**Table 2.15 Comparison of Interrupt Controller Registers**

Register	Bit	RX65N (ICUB)	RX671 (ICUE)
NMISR	RAMST (RX65N) EXNMIST (RX671)	RAM error interrupt status flag	Expanded non-maskable interrupt status flag
NMIER	RAMEN (RX65N) EXNMIEN (RX671)	RAM error interrupt enable bit	Expanded non-maskable interrupt enable bit
EXNMISR	—	—	Expanded non-maskable interrupt status register
EXNMIER	—	—	Expanded non-maskable interrupt enable register
EXNMICLR	—	—	Expanded non-maskable interrupt status clear register
GRPIE0	—	—	Group IE0 interrupt request register
GRPBL2	—	Group BL2 interrupt request register	—
GENIE0	—	—	Group IE0 interrupt request enable register
GENBL2	—	Group BL2 interrupt request enable register	—
GCRIE0	—	—	Group IE0 interrupt clear register
PIBRk	—	Software configurable interrupt B request register k (k = 0h to Bh)	Software configurable interrupt B request register k (k = 0h to Ch)

## 2.10 Buses

Table 2.16 is a comparative overview of the buses, Table 2.17 is a comparative overview of the external buses, and Table 2.18 is a comparison of bus registers.

**Table 2.16 Comparative Overview of Buses**

Item		RX65N	RX671
CPU buses	Instruction bus	<ul style="list-style-type: none"> <li>Connected to the CPU (for instructions)</li> <li>Connected to on-chip memory (RAM, <b>expansion RAM*1</b>, code flash memory)</li> <li>Operates in synchronization with the system clock (ICLK)</li> </ul>	<ul style="list-style-type: none"> <li>Connected to the CPU (for instructions)</li> <li>Connected to on-chip memory (RAM, code flash memory)</li> <li>Operates in synchronization with the system clock (ICLK)</li> </ul>
	Operand bus	<ul style="list-style-type: none"> <li>Connected to the CPU (for instructions)</li> <li>Connected to on-chip memory (RAM, <b>expansion RAM*1</b>, code flash memory)</li> <li>Operates in synchronization with the system clock (ICLK)</li> </ul>	<ul style="list-style-type: none"> <li>Connected to the CPU (for instructions)</li> <li>Connected to on-chip memory (RAM, code flash memory)</li> <li>Operates in synchronization with the system clock (ICLK)</li> </ul>
Memory buses	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to code flash memory	Connected to code flash memory
	Memory bus 3	<b>Connected to expansion RAM*1</b>	—
Internal main buses	Internal main bus 1	<ul style="list-style-type: none"> <li>Connected to the CPU</li> <li>Operates in synchronization with the system clock (ICLK)</li> </ul>	<ul style="list-style-type: none"> <li>Connected to the CPU</li> <li>Operates in synchronization with the system clock (ICLK)</li> </ul>
	Internal main bus 2	<ul style="list-style-type: none"> <li>Connected to the DMAC, DTC, and <b>extended bus master</b></li> <li>Connected to on-chip memory (RAM, <b>expansion RAM*1</b>, code flash memory)</li> <li>Operates in synchronization with the system clock (ICLK)</li> </ul>	<ul style="list-style-type: none"> <li>Connected to the DMAC and DTC</li> <li>Connected to on-chip memory (RAM, code flash memory)</li> <li>Operates in synchronization with the system clock (ICLK)</li> </ul>
Internal peripheral buses	Internal peripheral bus 1	<ul style="list-style-type: none"> <li>Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section)</li> <li>Operates in synchronization with the system clock (ICLK) (EXDMAC operates in synchronization with the BCLK)</li> </ul>	<ul style="list-style-type: none"> <li>Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section)</li> <li>Operates in synchronization with the system clock (ICLK) (EXDMAC operates in synchronization with the BCLK)</li> </ul>
	Internal peripheral bus 2	<ul style="list-style-type: none"> <li>Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5)</li> <li>Operates in synchronization with the peripheral module clock (PCLKB)</li> </ul>	<ul style="list-style-type: none"> <li>Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5)</li> <li>Operates in synchronization with the peripheral module clock (PCLKB)</li> </ul>

Item		RX65N	RX671
Internal peripheral buses	Internal peripheral bus 3	<ul style="list-style-type: none"> <li>Connected to peripheral modules (USBb, PDC, and standby RAM)</li> <li>Operates in synchronization with the peripheral module clock (PCLKB)</li> </ul>	<ul style="list-style-type: none"> <li>Connected to peripheral modules (USB, DOCA, CTSU, REMC, and standby RAM)</li> <li>Operates in synchronization with the peripheral module clock (PCLKB)</li> </ul>
	Internal peripheral bus 4	<ul style="list-style-type: none"> <li>Connected to peripheral modules (EDMAC, ETHERC, MTU3, SCli, RSPI, and AES*2)</li> <li>Operates in synchronization with the peripheral module clock (PCLKA)</li> </ul>	<ul style="list-style-type: none"> <li>Connected to peripheral modules (MTU, SCIm, and RSPI)</li> <li>Operates in synchronization with the peripheral module clock (PCLKA)</li> </ul>
	Internal peripheral bus 5	<ul style="list-style-type: none"> <li>Connected to peripheral modules (GLCDC and DRW2D)*1</li> <li>Operates in synchronization with the peripheral module clock (PCLKA)</li> </ul>	<ul style="list-style-type: none"> <li>Connected to peripheral modules (RSCI, RSPIA, and RIICHS)</li> <li>Operates in synchronization with the peripheral module clock (PCLKA)</li> </ul>
	Internal peripheral bus 6	<ul style="list-style-type: none"> <li>Connected to code flash (in P/E) and data flash memory*1</li> <li>Operates in synchronization with the Flash-IF clock (FCLK)</li> </ul>	<ul style="list-style-type: none"> <li>Connected to code flash (in P/E) and data flash memory</li> <li>Operates in synchronization with the Flash-IF clock (FCLK)</li> </ul>
External bus	CS area	<ul style="list-style-type: none"> <li>Connected to external devices</li> <li>Operates in synchronization with the external-bus clock (BCLK)</li> </ul>	<ul style="list-style-type: none"> <li>Connected to external devices</li> <li>Operates in synchronization with the external-bus clock (BCLK)</li> </ul>
	SDRAM area	<ul style="list-style-type: none"> <li>Connected to SDRAM</li> <li>Operates in synchronization with the SDRAM clock (SDCLK)</li> </ul>	<ul style="list-style-type: none"> <li>Connected to SDRAM</li> <li>Operates in synchronization with the SDRAM clock (SDCLK)</li> </ul>
Internal expansion bus	QSPI area	—	<ul style="list-style-type: none"> <li>Connected to external SPI devices</li> <li>Operates in synchronization with the system clock (ICLK)</li> </ul>

Notes: 1. Implemented only on products with a code flash memory capacity of 1.5 MB or more.  
 2. Implemented only on products with a code flash memory capacity of 1 MB or less.

**Table 2.17 Comparative Overview of External Buses**

Item	RX65N	RX671
External address space	<ul style="list-style-type: none"> <li>The external address space is divided into eight CS areas (CS0 to CS7) and the SDRAM area (SDCS) for management.</li> <li>Chip select signals can be output for each area.</li> <li>The bus width can be selected independently for each area.                             <ul style="list-style-type: none"> <li>Separate bus: An 8, 16, or <b>32-bit bus space</b> is selectable.</li> <li>Address/data multiplexed bus: An 8 or 16-bit bus space is selectable.</li> </ul> </li> <li>The endian mode can be selected independently for each area.</li> </ul>	<ul style="list-style-type: none"> <li>The external address space is divided into eight CS areas (CS0 to CS7) and the SDRAM area (SDCS) for management.</li> <li>Chip select signals can be output for each area.</li> <li>The bus width can be selected independently for each area.                             <ul style="list-style-type: none"> <li>Separate bus: An 8 or 16-bit bus space is selectable.</li> <li>Address/data multiplexed bus: An 8 or 16-bit bus space is selectable.</li> </ul> </li> </ul> <p>The endian mode can be selected independently for each area.</p>
CS area controller	<ul style="list-style-type: none"> <li>Recovery cycles can be inserted.                             <ul style="list-style-type: none"> <li>Up to 15 cycles for read recovery</li> <li>Up to 15 cycles for write recovery</li> </ul> </li> <li>Cycle wait function: Waits for up to 31 cycles (up to 7 cycles for page access).</li> <li>Wait control                             <ul style="list-style-type: none"> <li>Ability to specify timing of assertion and negation of chip-select signals (CS0# to CS7#)</li> <li>Ability to specify timing of assertion of the read signal (RD#) and write signals (WR0#/WR#, and WR1# to WR3#)</li> <li>Ability to specify data output start and end timing</li> </ul> </li> <li>Write access mode: Single write strobe mode or byte strobe mode</li> <li>Separate bus or address/data multiplexed bus can be specified for each area.</li> </ul>	<ul style="list-style-type: none"> <li>Recovery cycles can be inserted.                             <ul style="list-style-type: none"> <li>Up to 15 cycles for read recovery</li> <li>Up to 15 cycles for write recovery</li> </ul> </li> <li>Cycle wait function: Waits for up to 31 cycles (up to 7 cycles for page access).</li> <li>Wait control                             <ul style="list-style-type: none"> <li>Ability to specify timing of assertion and negation of chip-select signals (CS0# to CS7#)</li> <li>Ability to specify timing of assertion of the read signal (RD#) and write signals (WR0#/WR#, and WR1#)</li> <li>Ability to specify data output start and end timing</li> </ul> </li> <li>Write access mode: Single write strobe mode or byte strobe mode</li> <li>Separate bus or address/data multiplexed bus can be specified for each area.</li> </ul>
SDRAM area controller	<ul style="list-style-type: none"> <li>Multiplexed output of row address/column address (8, 9, 10, or 11 bits)</li> <li>Selectable between self-refresh and auto-refresh</li> <li>CAS latency can be specified from one to three cycles.</li> </ul>	<ul style="list-style-type: none"> <li>Multiplexed output of row address/column address (8, 9, 10, or 11 bits)</li> <li>Selectable between self-refresh and auto-refresh</li> <li>CAS latency can be specified from one to three cycles.</li> </ul>
Write buffer function	Write access by the bus master ends when the write data from the bus master has been written to the write buffer.	Write access by the bus master ends when the write data from the bus master has been written to the write buffer.
Frequencies	<ul style="list-style-type: none"> <li>The CS area controller (CSC) operates in synchronization with BCLK.</li> <li>The SDRAM area controller (SDRAMC) operates in synchronization with SDCLK.</li> </ul>	<ul style="list-style-type: none"> <li>The CS area controller (CSC) operates in synchronization with BCLK.</li> <li>The SDRAM area controller (SDRAMC) operates in synchronization with SDCLK.</li> </ul>

**Table 2.18 Comparison of Bus Registers**

Register	Bit	RX65N	RX671
CSnCR (n = 0 to 7)	BSIZE[1:0]	External bus width select bits  b5 b4 0 0: 16-bit bus space selected 0 1: 32-bit bus space selected 1 0: 8-bit bus space selected 1 1: Setting prohibited	External bus width select bits  b5 b4 0 0: 16-bit bus space selected 0 1: <b>Setting prohibited</b> 1 0: 8-bit bus space selected 1 1: Setting prohibited
SDCCR	BSIZE[1:0]	SDRAM bus width select bits  b5 b4 0 0: 16-bit bus space selected 0 1: 32-bit bus space selected 1 0: 8-bit bus space selected 1 1: Setting prohibited	SDRAM bus width select bits  b5 b4 0 0: 16-bit bus space selected 0 1: <b>Setting prohibited</b> 1 0: 8-bit bus space selected 1 1: Setting prohibited
BERSR1	MST[2:0]	Bus master code bits  b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Extended bus master 1 1 1: EXDMAC	Bus master code bits  b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: <b>Reserved</b> 1 1 1: EXDMAC
BUSPRI	BPRA[1:0]	Memory bus 1 and <b>3</b> (RAM/ <b>expansion RAM</b> ) priority control bits	Memory bus 1 (RAM) priority control bits
	BPXB[1:0]	—	Internal expansion bus priority control bits
EBMAPCR	—	Extended bus master priority control register	—

## 2.11 DMA Controller

Table 2.19 is a comparative overview of the DMA controllers, and Table 2.20 is a comparison of DMA controller registers.

**Table 2.19 Comparative Overview of DMA Controllers**

Item		RX65N (DMACAa)	RX671 (DMACAb)
Number of channels		8 channels (DMAC <sub>m</sub> (m = 0 to 7))	8 channels (DMAC <sub>m</sub> (m = 0 to 7))
Transfer space		512 MB (00000000h to 0FFFFFFFh and F0000000h to FFFFFFFFh, excluding reserved areas)	<b>4 GB</b> (00000000h to FFFFFFFFh, excluding reserved areas)
Maximum transfer volume		64 MB (maximum number of transfers in block transfer mode: 1,024 data × 65,536 blocks)	64 MB (maximum number of transfers in block transfer mode: 1,024 data × 65,536 blocks)
DMA request sources		Activation source selectable for each channel <ul style="list-style-type: none"> <li>• Software trigger</li> <li>• Interrupt requests from peripheral modules or trigger input to external interrupt input pins</li> </ul>	Activation source selectable for each channel <ul style="list-style-type: none"> <li>• Software trigger</li> <li>• Interrupt requests from peripheral modules or trigger input to external interrupt input pins</li> </ul>
Channel priority		Channel 0 > channel 1 > channel 2 > channel 3 ... > channel 7 (channel 0: highest)	Channel 0 > channel 1 > channel 2 > channel 3 ... > channel 7 (channel 0: highest)
Transfer data	Single data	Bit length: 8, 16, 32 bits	Bit length: 8, 16, 32 bits
	Block size	Number of data: 1 to 1,024	Number of data: 1 to 1,024
Transfer modes	Normal transfer mode	<ul style="list-style-type: none"> <li>• One data transfer per DMA transfer request</li> <li>• Setting in which total number of data transfers is not specified (free running mode) is available.</li> </ul>	<ul style="list-style-type: none"> <li>• One data transfer per DMA transfer request</li> <li>• Setting in which total number of data transfers is not specified (free running mode) is available.</li> </ul>
	Repeat transfer mode	<ul style="list-style-type: none"> <li>• One data transfer per DMA transfer request</li> <li>• Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination.</li> <li>• Maximum settable repeat size: 1,024 data</li> </ul>	<ul style="list-style-type: none"> <li>• One data transfer per DMA transfer request</li> <li>• Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination.</li> <li>• Maximum settable repeat size: 1,024 data</li> </ul>
	Block transfer mode	<ul style="list-style-type: none"> <li>• One block data transfer per DMA transfer request</li> <li>• Maximum settable block size: 1,024 data</li> </ul>	<ul style="list-style-type: none"> <li>• One block data transfer per DMA transfer request</li> <li>• Maximum settable block size: 1,024 data</li> </ul>
Selective functions	Extended repeat area function	<ul style="list-style-type: none"> <li>• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed</li> <li>• Area of 2 bytes to 128 MB separately settable as extended repeat area for transfer source or destination</li> </ul>	<ul style="list-style-type: none"> <li>• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed</li> <li>• Area of 2 bytes to 128 MB separately settable as extended repeat area for transfer source or destination</li> </ul>

Item		RX65N (DMACAa)	RX671 (DMACAb)
Interrupt request	Transfer end interrupt	<ul style="list-style-type: none"> <li>Generated when the specified number of transfers is completed in normal transfer mode</li> <li>Generated when the specified repeat count of transfers is completed in repeat transfer mode</li> <li>Generated when the specified block count of transfers is completed in block transfer mode</li> </ul>	<ul style="list-style-type: none"> <li>Generated when the specified number of transfers is completed in normal transfer mode</li> <li>Generated when the specified repeat count of transfers is completed in repeat transfer mode</li> <li>Generated when the specified block count of transfers is completed in block transfer mode</li> </ul>
	Transfer escape end interrupt	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.
Event link function		Event link request generated after one data transfer (or after one block transfer in case of block transfer operation).	Event link request generated after one data transfer (or after one block transfer in case of block transfer operation).
Low power consumption function		Module stop state can be set.	Module stop state can be set.

**Table 2.20 Comparison of DMA Controller Registers**

Register	Bit	RX65N (DMACAa)	RX671 (DMACAb)
DMSAR	—	DMA source address register  Specifies the start address of the transfer source. 00000000h to 0FFFFFFFh (256 MB) F0000000h to FFFFFFFFh (256 MB)	DMA source address register  Specifies the start address of the transfer source. 00000000h to FFFFFFFFh (4 GB)
DMDAR	—	DMA destination address register  Specifies the start address of the transfer destination. 00000000h to 0FFFFFFFh (256 MB) F0000000h to FFFFFFFFh (256 MB)	DMA destination address register  Specifies the start address of the transfer destination. 00000000h to FFFFFFFFh (4 GB)



## 2.12 Event Link Controller

Table 2.21 is a comparative overview of the event link controllers, Table 2.22 is a comparison of event link controller registers, Table 2.23 lists correspondences between ELSRn registers and peripheral modules, and Table 2.24 shows correspondences between values set in ELSRn.ELS[7:0] and event signal names and numbers.

**Table 2.21 Comparative Overview of Event Link Controllers**

Item	RX65N (ELC)	RX671 (ELC)
Event link function	<ul style="list-style-type: none"> <li>82 event signals can be directly connected to modules.</li> <li>Operation of timer modules while inputting an event signal can be selected.</li> <li>Event linkage operation is possible on ports B and E.                             <ul style="list-style-type: none"> <li>Single port*1: Event link operation can be enabled on a single port corresponding to the specified bit.</li> <li>Port group*1: Among the eight I/O ports, event link operation can be enabled for a group of ports corresponding to multiple specified bits.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>99 event signals can be directly interconnected to modules.</li> <li>Operation of timer modules while inputting an event signal can be selected.</li> <li>Event linkage operation is possible on ports B and E.                             <ul style="list-style-type: none"> <li>Single port*1: Event link operation can be specified on a single port.</li> <li>Port group*1: Event linkage operation can be specified by grouping multiple designated ports among up to eight ports.</li> </ul> </li> </ul>
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Note: 1. An event is generated when the corresponding input signal on a single port or port group set to input changes.

**Table 2.22 Comparison of Event Link Controller Registers**

Register	Bit	RX65N (ELC)	RX671 (ELC)
ELSRn	—	Event link setting register n (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 33, 35 to 38, and 45)	Event link setting register n (n = 0, 3, 4, 7, 10 to 15, 18 to 28, 33, 35 to 38, and 45)
	ELS[7:0]	Event link select bits  00h: Event output to the corresponding peripheral module is disabled. 01h to BDh: Specifies the number of the event signal to be linked.  Settings other than the above are prohibited.	Event link select bits  00h: Event signal output to the corresponding peripheral module is disabled. 01h to DFh: Specifies the number of the event signal to be linked.  Settings other than the above are prohibited.

**Table 2.23 Correspondence between ELSRn Registers and Peripheral Modules**

Register	RX65N (ELC)	RX671 (ELC)
ELSR0	MTU0	MTU0
ELSR3	MTU3	MTU3
ELSR4	MTU4	MTU4
ELSR7	CMT1	CMT1
ELSR10	TMR0	TMR0
ELSR11	TMR1	TMR1
ELSR12	TMR2	TMR2
ELSR13	TMR3	TMR3
ELSR14	—	CTSU
ELSR15	S12AD	S12AD
ELSR16	DA0	—
ELSR18	ICU (interrupt 1)	ICU (interrupt 1)
ELSR19	ICU (interrupt 2)	ICU (interrupt 2)
ELSR20	Output port group 1	Output port group 1
ELSR21	Output port group 2	Output port group 2
ELSR22	Input port group 1	Input port group 1
ELSR23	Input port group 2	Input port group 2
ELSR24	Single port 0	Single port 0
ELSR25	Single port 1	Single port 1
ELSR26	Single port 2	Single port 2
ELSR27	Single port 3	Single port 3
ELSR28	Clock source switching to LOCO	Clock source switching to LOCO
ELSR33	CMTW0	CMTW0
ELSR35	TPU0	TPU0
ELSR36	TPU1	TPU1
ELSR37	TPU2	TPU2
ELSR38	TPU3	TPU3
ELSR45	S12AD1 (ELCTRG1N)	S12AD1

**Table 2.24 Correspondence between Values Set in ELSRn.ELS[7:0] Bits and Event Signal Names and Numbers**

Value of ELS[7:0] Bits	Peripheral Module	RX65N (ELC)	RX671 (ELC)
01h	Multifunction timer pulse unit 3	MTU0 compare match 0A	MTU0 compare match 0A
02h		MTU0 compare match 0B	MTU0 compare match 0B
03h		MTU0 compare match 0C	MTU0 compare match 0C
04h		MTU0 compare match 0D	MTU0 compare match 0D
05h		MTU0 compare match 0E	MTU0 compare match 0E
06h		MTU0 compare match 0F	MTU0 compare match 0F
07h		MTU0 overflow	MTU0 overflow
10h		MTU3 compare match 3A	MTU3 compare match 3A
11h		MTU3 compare match 3B	MTU3 compare match 3B
12h		MTU3 compare match 3C	MTU3 compare match 3C
13h		MTU3 compare match 3D	MTU3 compare match 3D
14h		MTU3 overflow	MTU3 overflow
15h		MTU4 compare match 4A	MTU4 compare match 4A
16h		MTU4 compare match 4B	MTU4 compare match 4B
17h		MTU4 compare match 4C	MTU4 compare match 4C
18h		MTU4 compare match 4D	MTU4 compare match 4D
19h		MTU4 overflow	MTU4 overflow
1Ah	MTU4 underflow	MTU4 underflow	
1Fh	Compare match timer	CMT1 compare match 1	CMT1 compare match 1
22h	8-bit timer	TMR0 compare match A0	TMR0 compare match A0
23h		TMR0 compare match B0	TMR0 compare match B0
24h		TMR0 overflow	TMR0 overflow
25h		TMR1 compare match A1	TMR1 compare match A1
26h		TMR1 compare match B1	TMR1 compare match B1
27h		TMR1 overflow	TMR1 overflow
28h		TMR2 compare match A2	TMR2 compare match A2
29h		TMR2 compare match B2	TMR2 compare match B2
2Ah		TMR2 overflow	TMR2 overflow
2Bh		TMR3 compare match A3	TMR3 compare match A3
2Ch		TMR3 compare match B3	TMR3 compare match B3
2Dh	TMR3 overflow	TMR3 overflow	
2Eh	Realtime clock	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)
31h	Independent watchdog timer	IWDT underflow or refresh error	IWDT underflow or refresh error
3Ah	Serial communications interface	SCI5 error (receive error or error signal detection)	SCI5 error (receive error or error signal detection)
3Bh		SCI5 receive data full	SCI5 receive data full
3Ch		SCI5 transmit data empty	SCI5 transmit data empty
3Dh		SCI5 transmit end	SCI5 transmit end
4Eh	I <sup>2</sup> C bus interface	RIIC0 communication error or event generation	RIIC0 communication error or event generation
4Fh		RIIC0 receive data full	RIIC0 receive data full
50h		RIIC0 transmit data empty	RIIC0 transmit data empty
51h		RIIC0 transmit end	RIIC0 transmit end

Value of ELS[7:0] Bits	Peripheral Module	RX65N (ELC)	RX671 (ELC)
52h	Serial peripheral interface	RSPI0 error (mode fault, overrun, underrun, or parity error)	RSPI0 error (mode fault, overrun, underrun, or parity error)
53h		RSPI0 idle	RSPI0 idle
54h		RSPI0 receive data full	RSPI0 receive buffer full
55h		RSPI0 transmit data empty	RSPI0 transmit buffer empty
56h		RSPI0 transmit end	RSPI0 communication end
58h		12-bit A/D converter	S12AD A/D conversion end
5Bh	Voltage detection circuit	LVD1 voltage detection	LVD1 voltage detection
5Ch		LVD2 voltage detection	LVD2 voltage detection
5Dh	DMA controller	DMAC0 transfer end	DMAC0 transfer end
5Eh		DMAC1 transfer end	DMAC1 transfer end
5Fh		DMAC2 transfer end	DMAC2 transfer end
60h		DMAC3 transfer end	DMAC3 transfer end
61h	Data transfer controller	DTC transfer end	DTC transfer end
62h	Clock generation circuit	Oscillation stop detection of clock generation circuit	Oscillation stop detection of clock generation circuit
63h	I/O ports	Input edge detection of input port group 1	Input edge detection of input port group 1
64h		Input edge detection of input port group 2	Input edge detection of input port group 2
65h		Input edge detection of single input port 0	Input edge detection of single input port 0
66h		Input edge detection of single input port 1	Input edge detection of single input port 1
67h		Input edge detection of single input port 2	Input edge detection of single input port 2
68h		Input edge detection of single input port 3	Input edge detection of single input port 3
69h	Event link controller	Software event	Software event
6Ah	Data operation circuit	DOC data operation condition met	DOC data operation condition met
6Ch	12-bit A/D converter	S12AD1 A/D conversion end	S12AD1 A/D conversion end
7Eh	Compare match timer W	CMTW channel 0 compare match	CMTW channel 0 compare match
ACh	16-bit timer pulse unit	TPU0 compare match A	TPU0 compare match A
ADh		TPU0 compare match B	TPU0 compare match B
AEh		TPU0 compare match C	TPU0 compare match C
AFh		TPU0 compare match D	TPU0 compare match D
B0h		TPU0 overflow	TPU0 overflow
B1h		TPU1 compare match A	TPU1 compare match A
B2h		TPU1 compare match B	TPU1 compare match B
B3h		TPU1 overflow	TPU1 overflow
B4h		TPU1 underflow	TPU1 underflow
B5h		TPU2 compare match A	TPU2 compare match A
B6h		TPU2 compare match B	TPU2 compare match B
B7h		TPU2 overflow	TPU2 overflow
B8h		TPU2 underflow	TPU2 underflow

Value of ELS[7:0] Bits	Peripheral Module	RX65N (ELC)	RX671 (ELC)
B9h	16-bit timer pulse unit	TPU3 compare match A	TPU3 compare match A
BAh		TPU3 compare match B	TPU3 compare match B
BBh		TPU3 compare match C	TPU3 compare match C
BCh		TPU3 compare match D	TPU3 compare match D
BDh		TPU3 overflow	TPU3 overflow
D0h	Serial communications interface	—	RSCI10 error
D1h		—	RSCI10 receive data full
D2h		—	RSCI10 receive data match
D3h		—	RSCI10 transmit data empty
D4h		—	RSCI10 transmit end
D5h		—	RSCI10 receive data mismatch
D6h	High-speed I <sup>2</sup> C bus interface	—	RSCI10 valid edge detection
D7h		—	RIICHS0 communication error, event occurrence
D8h		—	RIICHS0 receive data full
D9h		—	RIICHS0 transmit data empty
DAh	Serial peripheral interface	—	RSPIA0 transmit end
DBh		—	RSPIA0 error
DCh		—	RSPIA0 idle
DDh		—	RSPIA0 receive buffer full
DEh		—	RSPIA0 transmit buffer empty
DFh	—	RSPIA0 communication end	
Settings other than the above are prohibited.			

## 2.13 I/O Ports

Table 2.25 to Table 2.27 are comparative overviews of I/O ports, Table 2.28 is comparison of I/O port functions on RX65N products with a code flash memory capacity of 1 MB or less, Table 2.29 is comparison of I/O port functions on RX65N products with a code flash memory capacity of 1.5 MB or more, and Table 2.30 is a comparison of I/O port registers.

**Table 2.25 Comparative Overview of I/O Ports on 145- and 144-Pin Packages**

Port Symbol	RX65N (145-, 144-Pin)	RX671 (145-, 144-Pin)
PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P56	P50 to P56
PORT6	P60 to P67	P60 to P67
PORT7	P70 to P77	P70 to P77*1
PORT8	P80 to P83, P86, P87	P80 to P83, P86, P87
PORT9	P90 to P93	P90 to P93
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTF	PF5	PF5
PORTH	—	PH1, PH2
PORTJ	PJ3, PJ5	PJ3, PJ5

Note: 1. The 145-pin TFLGA (0.65 mm pitch) product does not have pins P71 and P72.

**Table 2.26 Comparative Overview of I/O Ports on 100-Pin Packages**

Port Symbol	RX65N (100-Pin)	RX671 (100-Pin)
PORT0	P05, P07	P05, P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTH	—	PH1, PH2
PORTJ	PJ3	PJ3

**Table 2.27 Comparative Overview of I/O Ports on 64-Pin Packages**

Port Symbol	RX65N (64-Pin)	RX671 (64-Pin)
PORT0	P05*1	P05*1
PORT1	P12, P13, P16, P17	P12, P13, P16, P17
PORT2	P26, P27	P26, P27
PORT3	P30, P31, P34 to P37	P30, P31, P34 to P37
PORT4	P40 to P43	P40 to P43
PORT5	P53	P53
PORTA	PA1, PA2, PA4, PA6, PA7	PA1, PA2, PA4, PA6, PA7
PORTB	PB5 to PB7	PB5 to PB7
PORTC	PC0, PC1, PC4 to PC7	PC0, PC1, PC4 to PC7
PORTD	PD2 to PD7	PD2 to PD7
PORTE	PE0 to PE2, PE6, PE7	PE0 to PE2, PE6, PE7
PORTH	—	PH1, PH2

Note: 1. Not present on the 64-pin TFBGA product.

**Table 2.28 Comparison of I/O Port Functions (Products with Code Flash Memory Capacity of 1 MB or Less (RX65N))**

Item	Port Symbol	RX65N	RX671
Input pull-up	PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
	PORT1	P12 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P56	P50 to P56
	PORT6	P60 to P67	P60 to P67
	PORT7	P70 to P77	P70 to P77
	PORT8	P80 to P83, P86, P87	P80 to P83, P86, P87
	PORT9	P90 to P93	P90 to P93
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
Open-drain output	PORTF	PF5	PF5
	PORTH	—	PH1, PH2
	PORTJ	PJ3, PJ5	PJ3, PJ5
	PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
	PORT1	P12 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P56	P50 to P56
	PORT6	P60 to P67	P60 to P67
	PORT7	P70 to P77	P70 to P77
	PORT8	P80 to P83, P86, P87	P80 to P83, P86, P87
	PORT9	P90 to P93	P90 to P93
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7	
PORTD	PD0 to PD7	PD0 to PD7	

Item	Port Symbol	RX65N	RX671
Open-drain output	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	PF5	PF5
	PORTH	—	PH1, PH2
	PORTJ	PJ3, PJ5	PJ3, PJ5
Driving ability switching	PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
	PORT1	P12 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P56	P50 to P56
	PORT6	P60 to P67	P60 to P67
	PORT7	P70 to P77	P70 to P77
	PORT8	P80 to P83, P86, P87	P80 to P83, P86, P87
	PORT9	P90 to P93	P90 to P93
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	PF5	PF5
PORTH	—	PH1, PH2	
PORTJ	PJ3, PJ5	PJ3, PJ5	
5 V tolerant	PORT0	P07	P07
	PORT1	P12 to P17	P12 to P17
	PORT2	P20, P21	P20, P21
	PORT3	P30 to P33	P30 to P33
	PORT6	P67	P67
	PORT7	—	P73
	PORTC	PC0 to PC3	PC0 to PC3
	PORTJ	—	PJ3



**Table 2.29 Comparison of I/O Port Functions (Products with Code Flash Memory Capacity of 1.5 MB or More (RX65N))**

Item	Port Symbol	RX65N	RX671
Input pull-up	PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
	PORT1	P10 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P57	P50 to P56
	PORT6	P60 to P67	P60 to P67
	PORT7	P70 to P77	P70 to P77
	PORT8	P80 to P87	P80 to P83, P86, P87
	PORT9	P90 to P97	P90 to P93
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	PF0 to PF5	PF5
PORTG	PG0 to PG7	—	
PORTH	—	PH1, PH2	
PORTJ	PJ0 to PJ3, PJ5	PJ3, PJ5	
Open-drain output	PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
	PORT1	P10 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P57	P50 to P56
	PORT6	P60 to P67	P60 to P67
	PORT7	P70 to P77	P70 to P77
	PORT8	P80 to P87	P80 to P83, P86, P87
	PORT9	P90 to P97	P90 to P93
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	PF0 to PF5	PF5
PORTG	PG0 to PG7	—	
PORTH	—	PH1, PH2	
PORTJ	PJ0 to PJ3, PJ5	PJ3, PJ5	
Driving ability switching	PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
	PORT1	P10 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P57	P50 to P56
	PORT6	P60 to P67	P60 to P67
	PORT7	P70 to P77	P70 to P77
	PORT8	P80 to P87	P80 to P83, P86, P87
	PORT9	P90 to P97	P90 to P93

Item	Port Symbol	RX65N	RX671
Driving ability switching	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	PF0 to PF5	PF5
	PORTG	PG0 to PG7	—
	PORTH	—	PH1, PH2
	PORTJ	PJ0 to PJ3, PJ5	PJ3, PJ5
5 V tolerant	PORT0	P07	P07
	PORT1	P11 to P17	P12 to P17
	PORT2	P20, P21	P20, P21
	PORT3	P30 to P33	P30 to P33
	PORT6	P67	P67
	PORT7	—	P73
	PORTC	PC0 to PC3	PC0 to PC3
	PORTJ	—	PJ3

**Table 2.30 Comparison of I/O Port Registers**

Register	Bit	RX65N	RX671
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to G, J)	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to F, H, J)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 9, A to G, J)	Pm0 to Pm7 output data store bits (m = 0 to 9, A to F, H, J)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 9, A to G, J)	Pm0 to Pm7 bits (m = 0 to 9, A to F, H, J)
PMR	B0 to B7	Pm0 to Pm7 pin mode control bits (m = 0 to 9, A to G, J)	Pm0 to Pm7 pin mode control bits (m = 0 to 9, A to F, H, J)
ODR0	B0	Pm0 output type select bit (m = 0 to 9, A to G, J)	Pm0 output type select bit (m = 0 to 9, A to E, H, J)
	B2	Pm1 output type select bit (m = 0 to 9, A to G, J)	Pm1 output type select bit (m = 0 to 9, A to E, H, J)
	B3	PE1 output type select bit (m = 0 to 9, A to G, J)	PE1 output type select bit (m = 0 to 9, A to E, H, J)
	B4	Pm2 output type select bit (m = 0 to 9, A to G, J)	Pm2 output type select bit (m = 0 to 9, A to E, H, J)
	B6	Pm3 output type select bit (m = 0 to 9, A to G, J)	Pm3 output type select bit (m = 0 to 9, A to E, H, J)
ODR1	B0	Pm4 output type select bit (m = 0 to 9, A to G, J)	Pm4 output type select bit (m = 0 to 8, A to F, J)
	B2	Pm5 output type select bit (m = 0 to 9, A to G, J)	Pm5 output type select bit (m = 0 to 8, A to F, J)
	B4	Pm6 output type select bit (m = 0 to 9, A to G, J)	Pm6 output type select bit (m = 0 to 8, A to F, J)
	B6	Pm7 output type select bit (m = 0 to 9, A to G, J)	Pm7 output type select bit (m = 0 to 8, A to F, J)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to G, J)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to F, H, J)
DSCR	B0 to B7	Pm0 to Pm7 drive capacity control bits (m = 0 to 2, 5, 7 to 9, A to E, G, J)	Pm0 to Pm7 drive capacity control bits (m = 0 to 2, 5, 7 to 9, A to E, H)
DSCR2	B0 to B7	Pm0 to Pm7 drive capacity control bits 2 (m = 0 to 3, 5, 7 to 9, A to E, G, J)	Pm0 to Pm7 drive capacity control bits 2 (m = 0 to 3, 5, 7 to 9, A to E, H)

## 2.14 Multi-Function Pin Controller

Table 2.31 is a comparison of the assignments of multiplexed pins, and Table 2.32 to Table 2.49 are comparisons of multi-function pin controller registers.

In the following comparison of the assignments of multiplexed pins, **light blue text** designates pins that exist on the RX671 Group only and **orange text** pins that exist on the RX65N Group only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented. A filled circle (●) indicates cases where all pins are present among pin functions where there is a difference in the pins present on the RX671 Group and RX65N Group.

**Table 2.31 Comparison of Multiplexed Pin Assignments**

Module/ Function	Pin Function	Port Allocation	RX65N			RX671		
			145-/ 144- Pin	100- Pin	64- Pin	145-/ 144- Pin	100- Pin	64- Pin
Interrupt	NMI (input)	P35	○	○	○	○	○	○
EXDMA controller	EDREQ0 (input)	P22	○	○	×	○	○	×
		P55	○	○	×	○	○	×
		P80	○	×	×	○	×	×
	EDACK0 (output)	P23	○	○	×	○	○	×
		P54	○	○	×	○	○	×
		P81	○	×	×	○	×	×
	EDREQ1 (input)	P24	○	○	×	○	○	×
		P33	○	○	×	○	○	×
		P82	○	×	×	○	×	×
	EDACK1 (output)	P25	○	○	×	○	○	×
		P56	○	×	×	○	×	×
		P83	○	×	×	○	×	×
PJ3		○	○	×	○	○	×	
Interrupt	IRQ0-DS (input)	P30	○	○	○	○	○	○
	IRQ0 (input)	PD0	○	○	×	○	○	×
		P50	×	×	×	○	○	×
		P60	×	×	×	○	×	×
		P70	×	×	×	○	×	×
		P90	×	×	×	○	×	×
		PA0	×	×	×	○	○	×
		PH1	×	×	×	○	○	○
	IRQ1-DS (input)	P31	○	○	○	○	○	○
	IRQ1 (input)	PD1	○	○	×	○	○	×
		P51	×	×	×	○	○	×
		P61	×	×	×	○	×	×
		P71	×	×	×	○ <sup>*3</sup>	×	×
		PH2	×	×	×	○	○	○
	IRQ2-DS (input)	P32	○	○	×	○	○	×
	IRQ2 (input)	P12	○	○	○	○	○	○
		PD2	○	○	○	○	○	○
		P52	×	×	×	○	○	×
		P62	×	×	×	○	×	×
		P82	×	×	×	○	×	×
PB2		×	×	×	○	○	×	

Module/ Function	Pin Function	Port Allocation	RX65N			RX671		
			145-/ 144- Pin	100- Pin	64- Pin	145-/ 144- Pin	100- Pin	64- Pin
Interrupt	IRQ3-DS (input)	P33	○	○	×	○	○	×
	IRQ3 (input)	P13	○	○	○	○	○	○
		PD3	○	○	○	○	○	○
		P23	×	×	×	○	○	×
		P53	×	×	×	○	○	○
		P63	×	×	×	○	×	×
		P83	×	×	×	○	×	×
		PB3	×	×	×	○	○	×
	IRQ4-DS (input)	PB1	○	○	×	○	○	×
	IRQ4 (input)	P14	○	○	×	○	○	×
		P34	○	○	○	○	○	○
		PD4	○	○	○	○	○	○
		PF5	○	×	×	○	×	×
		P54	×	×	×	○	○	×
		P64	×	×	×	○	×	×
		PB4	×	×	×	○	○	×
	IRQ5-DS (input)	PA4	○	○	○	○	○	○
	IRQ5 (input)	P15	○	○	×	○	○	×
		PD5	○	○	○	○	○	○
		PE5	○	○	×	○	○	×
		P25	×	×	×	○	○	×
		PA5	×	×	×	○	○	×
		PC5	×	×	×	○	○	○
	IRQ6-DS (input)	PA3	○	○	×	○	○	×
	IRQ6 (input)	P16	○	○	○	○	○	○
		PD6	○	○	○	○	○	○
		PE6	○	○	○	○	○	○
		P26	×	×	×	○	○	○
		P56	×	×	×	○	×	×
		PB6	×	×	×	○	○	○
	IRQ7-DS (input)	PE2	○	○	○	○	○	○
	IRQ7 (input)	P17	○	○	○	○	○	○
		PD7	○	○	○	○	○	○
		PE7	○	○	○	○	○	○
		P27	×	×	×	○	○	○
		P77	×	×	×	○	×	×
		PA7	×	×	×	○	○	○
	IRQ8-DS (input)	P40	○	○	○	○	○	○
	IRQ8 (input)	P00	○	×	×	○	×	×
		P20	○	○	×	○	○	×
		P73	×	×	×	○	×	×
P80		×	×	×	○	×	×	
PE0		×	×	×	○	○	○	
IRQ9-DS (input)	P41	○	○	○	○	○	○	

Module/ Function	Pin Function	Port Allocation	RX65N			RX671		
			145-/ 144- Pin	100- Pin	64- Pin	145-/ 144- Pin	100- Pin	64- Pin
Interrupt	IRQ9 (input)	P01	○	×	×	○	×	×
		P21	○	○	×	○	○	×
		P81	×	×	×	○	×	×
		P91	×	×	×	○	×	×
		PE1	×	×	×	○	○	○
	IRQ10-DS (input)	P42	○	○	○	○	○	○
	IRQ10 (input)	P02	○	×	×	○	×	×
		P55	○	○	×	○	○	×
		P72	×	×	×	○*3	×	×
		P92	×	×	×	○	×	×
		PA2	×	×	×	○	○	○
		PC2	×	×	×	○	○	×
	IRQ11-DS (input)	P43	○	○	○	○	○	○
	IRQ11 (input)	P03	○	×	×	○	×	×
		PA1	○	○	○	○	○	○
		P93	×	×	×	○	×	×
		PC3	×	×	×	○	○	×
		PE3	×	×	×	○	○	×
		PJ3	×	×	×	○	○	×
	IRQ12-DS (input)	P44	○	○	×	○	○	×
	IRQ12 (input)	PB0	○	○	×	○	○	×
		PC1	○	○	○	○	○	○
		P24	×	×	×	○	○	×
		P74	×	×	×	○	×	×
		PC4	×	×	×	○	○	○
		PE4	×	×	×	○	○	×
	IRQ13-DS (input)	P45	○	○	×	○	○	×
	IRQ13 (input)	P05	○	○	○*5	○	○	○*5
		PC6	○	○	○	○	○	○
		P65	×	×	×	○	×	×
		P75	×	×	×	○	×	×
		PB5	×	×	×	○	○	○
		PJ5	×	×	×	○	×	×
	IRQ14-DS (input)	P46	○	○	×	○	○	×
	IRQ14 (input)	PC0	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
		P66	×	×	×	○	×	×
		P76	×	×	×	○	×	×
		P86	×	×	×	○	×	×
		PA6	×	×	×	○	○	○
	IRQ15-DS (input)	P47	○	○	×	○	○	×
	IRQ15 (input)	P07	○	○	×	○	○	×
		P67	○	×	×	○	×	×
		P22	×	×	×	○	○	×
		P87	×	×	×	○	×	×
PB7		×	×	×	○	○	○	

Module/ Function	Pin Function	Port Allocation	RX65N			RX671		
			145-/ 144- Pin	100- Pin	64- Pin	145-/ 144- Pin	100- Pin	64- Pin
Multi-function timer pulse unit 3	MTIOC0A (input/output)	P34	○	○	○	○	○	○
		PB3	○	○	×	○	○	×
	MTIOC0B (input/output)	P13	○	○	○	○	○	○
		P15	○	○	×	○	○	×
		PA1	○	○	○	○	○	○
	MTIOC0C (input/output)	P32	○	○	×	○	○	×
		PB1	○	○	×	○	○	×
	MTIOC0D (input/output)	P33	○	○	×	○	○	×
		PA3	○	○	×	○	○	×
	MTIOC1A (input/output)	P20	○	○	×	○	○	×
		PE4	○	○	×	○	○	×
	MTIOC1B (input/output)	P21	○	○	×	○	○	×
		PB5	○	○	○	○	○	○
	MTIOC2A (input/output)	P26	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
	MTIOC2B (input/output)	P27	○	○	○	○	○	○
		PE5	○	○	×	○	○	×
	MTIOC3A (input/output)	P14	○	○	×	○	○	×
		P17	○	○	○	○	○	○
		PC1	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	MTIOC3B (input/output)	P17	○	○	○	○	○	○
		P22	○	○	×	○	○	×
		P80	○	×	×	○	×	×
		PB7	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	PE1	○	○	○	○	○	○	
	MTIOC3C (input/output)	P16	○	○	○	○	○	○
		P56	○	×	×	○	×	×
		PC0	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
		PJ3	○	○	×	○	○	×
	MTIOC3D (input/output)	P16	○	○	○	○	○	○
		P23	○	○	×	○	○	×
		P81	○	×	×	○	×	×
		PB6	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
		PE0	○	○	○	○	○	○
	MTIOC4A (input/output)	P21	○	○	×	○	○	×
		P24	○	○	×	○	○	×
		P82	○	×	×	○	×	×
		PA0	○	○	×	○	○	×
		PB3	○	○	×	○	○	×
		PE2	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX671		
			145-/ 144- Pin	100- Pin	64- Pin	145-/ 144- Pin	100- Pin	64- Pin
Multi-function timer pulse unit 3	MTIOC4B (input/output)	P17	○	○	○	○	○	○
		P30	○	○	○	○	○	○
		P54	○	○	×	○	○	×
		PC2	○	○	×	○	○	×
		PD1	○	○	×	○	○	×
		PE3	○	○	×	○	○	×
	MTIOC4C (input/output)	P25	○	○	×	○	○	×
		P83	○	×	×	○	×	×
		P87	○	×	×	○	×	×
		PB1	○	○	×	○	○	×
		PE1	○	○	○	○	○	○
		PE5	○	○	×	○	○	×
	MTIOC4D (input/output)	P31	○	○	○	○	○	○
		P55	○	○	×	○	○	×
		P86	○	×	×	○	×	×
		PC3	○	○	×	○	○	×
		PD2	○	○	○	○	○	○
		PE4	○	○	×	○	○	×
	MTIC5U (input)	P12	×	×	×	○	○	○
		PA4	○	○	○	○	○	○
		PD7	○	○	○	○	○	○
	MTIC5V (input)	PA6	○	○	○	○	○	○
		PD6	○	○	○	○	○	○
	MTIC5W (input)	PB0	○	○	×	○	○	×
		PD5	○	○	○	○	○	○
	MTIOC6A (input/output)	PE7	○	○	○	○	○	○
	MTIOC6B (input/output)	PA5	○	○	×	○	○	×
	MTIOC6C (input/output)	PE6	○	○	○	○	○	○
	MTIOC6D (input/output)	PA0	○	○	×	○	○	×
	MTIOC7A (input/output)	PA2	○	○	○	○	○	○
	MTIOC7B (input/output)	PA1	○	○	○	○	○	○
	MTIOC7C (input/output)	P67	○	×	×	○	×	×
	MTIOC7D (input/output)	P66	○	×	×	○	×	×
MTIOC8A (input/output)	PD6	○	○	○	○	○	○	
MTIOC8B (input/output)	PD4	○	○	○	○	○	○	
MTIOC8C (input/output)	PD5	○	○	○	○	○	○	
MTIOC8D (input/output)	PD3	○	○	○	○	○	○	

Module/ Function	Pin Function	Port Allocation	RX65N			RX671		
			145-/ 144- Pin	100- Pin	64- Pin	145-/ 144- Pin	100- Pin	64- Pin
Multi-function timer pulse unit 3	MTCLKA (input)	P14	○	○	×	○	○	×
		P24	○	○	×	○	○	×
		PA4	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	MTCLKB (input)	P15	○	○	×	○	○	×
		P25	○	○	×	○	○	×
		PA6	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	MTCLKC (input)	P22	○	○	×	○	○	×
		PA1	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	MTCLKD (input)	P23	○	○	×	○	○	×
		PA3	○	○	×	○	○	×
		PC5	○	○	○	○	○	○
	Port output enable 3	POE0# (input)	P32	○	○	×	○	○
P93			○	×	×	○	×	×
PC4			○	○	○	○	○	○
PD1			○	○	×	○	○	×
PD7			○	○	○	○	○	○
POE4# (input)		P33	○	○	×	○	○	×
		P92	○	×	×	○	×	×
		PB5	○	○	○	○	○	○
		PD0	○	○	×	○	○	×
		PD6	○	○	○	○	○	○
POE8# (input)		P17	○	○	○	○	○	○
		P30	○	○	○	○	○	○
		PD3	○	○	○	○	○	○
		PE3	○	○	×	○	○	×
		PJ5	○	×	×	○	×	×
POE10# (input)		P32	○	○	×	○	○	×
		P34	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
		PD5	○	○	○	○	○	○
POE11# (input)		P33	○	○	×	○	○	×
		PB3	○	○	×	○	○	×
	PD4	○	○	○	○	○	○	
16-bit timer pulse unit	TIOCA0 (input/output)	P86	○	×	×	○	×	×
		PA0	○	○	×	○	○	×
	TIOCB0 (input/output)	P17	○	○	○	○	○	○
		PA1	○	○	○	○	○	○
	TIOCC0 (input/output)	P32	○	○	×	○	○	×
	TIOCD0 (input/output)	P33	○	○	×	○	○	×
		PA3	○	○	×	○	○	×
	TIOCA1 (input/output)	P56	○	×	×	○	×	×
		PA4	○	○	○	○	○	○
	TIOCB1 (input/output)	P16	○	○	○	○	○	○
PA5		○	○	×	○	○	×	



Module/ Function	Pin Function	Port Allocation	RX65N			RX671		
			145-/ 144- Pin	100- Pin	64- Pin	145-/ 144- Pin	100- Pin	64- Pin
16-bit timer pulse unit	TIOCA2 (input/output)	P87	○	×	×	○	×	×
		PA6	○	○	○	○	○	○
	TIOCB2 (input/output)	P15	○	○	×	○	○	×
		PA7	○	○	○	○	○	○
	TIOCA3 (input/output)	P21	○	○	×	○	○	×
		PB0	○	○	×	○	○	×
	TIOCB3 (input/output)	P20	○	○	×	○	○	×
		PB1	○	○	×	○	○	×
	TIOCC3 (input/output)	P22	○	○	×	○	○	×
		PB2	○	○	×	○	○	×
	TIOCD3 (input/output)	P23	○	○	×	○	○	×
		PB3	○	○	×	○	○	×
	TIOCA4 (input/output)	P25	○	○	×	○	○	×
		PB4	○	○	×	○	○	×
	TIOCB4 (input/output)	P24	○	○	×	○	○	×
		PB5	○	○	○	○	○	○
	TIOCA5 (input/output)	P13	○	○	○	○	○	○
		PB6	○	○	○	○	○	○
	TIOCB5 (input/output)	P14	○	○	×	○	○	×
		PB7	○	○	○	○	○	○
	TCLKA (input)	P14	○	○	×	○	○	×
		PC2	○	○	×	○	○	×
	TCLKB (input)	P15	○	○	×	○	○	×
		PA3	○	○	×	○	○	×
		PC3	○	○	×	○	○	×
	TCLKC (input)	P16	○	○	○	○	○	○
		PB2	○	○	×	○	○	×
		PC0	○	○	○	○	○	○
	TCLKD (input)	P17	○	○	○	○	○	○
		PB3	○	○	×	○	○	×
PC1		○	○	○	○	○	○	
Programmable pulse generator	PO0 (output)	P20	○	○	×	○	○	×
	PO1 (output)	P21	○	○	×	○	○	×
	PO2 (output)	P22	○	○	×	○	○	×
	PO3 (output)	P23	○	○	×	○	○	×
	PO4 (output)	P24	○	○	×	○	○	×
	PO5 (output)	P25	○	○	×	○	○	×
	PO6 (output)	P26	○	○	×	○	○	×
	PO7 (output)	P27	○	○	×	○	○	×
	PO8 (output)	P30	○	○	×	○	○	×
	PO9 (output)	P31	○	○	×	○	○	×
	PO10 (output)	P32	○	○	×	○	○	×
	PO11 (output)	P33	○	○	×	○	○	×
	PO12 (output)	P34	○	○	×	○	○	×
	PO13 (output)	P13	○	○	×	○	○	×
		P15	○	○	×	○	○	×
PO14 (output)	P16	○	○	×	○	○	×	

Module/ Function	Pin Function	Port Allocation	RX65N			RX671		
			145-/ 144- Pin	100- Pin	64- Pin	145-/ 144- Pin	100- Pin	64- Pin
Programmable pulse generator	PO15 (output)	P14	○	○	×	○	○	×
		P17	○	○	×	○	○	×
	PO16 (output)	P73	○	×	×	○	×	×
		PA0	○	○	×	○	○	×
	PO17 (output)	PA1	○	○	×	○	○	×
		PC0	○	○	×	○	○	×
	PO18 (output)	PA2	○	○	×	○	○	×
		PC1	○	○	×	○	○	×
		PE1	○	○	×	○	○	×
	PO19 (output)	P74	○	×	×	○	×	×
		PA3	○	○	×	○	○	×
	PO20 (output)	P75	○	×	×	○	×	×
		PA4	○	○	×	○	○	×
	PO21 (output)	PA5	○	○	×	○	○	×
		PC2	○	○	×	○	○	×
	PO22 (output)	P76	○	×	×	○	×	×
		PA6	○	○	×	○	○	×
	PO23 (output)	P77	○	×	×	○	×	×
		PA7	○	○	×	○	○	×
		PE2	○	○	×	○	○	×
	PO24 (output)	PB0	○	○	×	○	○	×
		PC3	○	○	×	○	○	×
	PO25 (output)	PB1	○	○	×	○	○	×
		PC4	○	○	×	○	○	×
	PO26 (output)	P80	○	×	×	○	×	×
		PB2	○	○	×	○	○	×
		PE3	○	○	×	○	○	×
	PO27 (output)	P81	○	×	×	○	×	×
		PB3	○	○	×	○	○	×
	PO28 (output)	P82	○	×	×	○	×	×
		PB4	○	○	×	○	○	×
PE4		○	○	×	○	○	×	
PO29 (output)	PB5	○	○	×	○	○	×	
	PC5	○	○	×	○	○	×	
PO30 (output)	PB6	○	○	×	○	○	×	
	PC6	○	○	×	○	○	×	
PO31 (output)	PB7	○	○	×	○	○	×	
	PC7	○	○	×	○	○	×	
8-bit timer	TMO0 (output)	P22	○	○	×	○	○	×
		PB3	○	○	×	○	○	×
		PH1	×	×	×	○	○	○
	TMCI0 (input)	P01	○	×	×	○	×	×
		P21	○	○	×	○	○	×
		PB1	○	○	×	○	○	×
	TMRI0 (input)	P00	○	×	×	○	×	×
		P20	○	○	×	○	○	×
PA4		○	○	○	○	○	○	
PH2		×	×	×	○	○	○	

Module/ Function	Pin Function	Port Allocation	RX65N			RX671		
			145-/ 144- Pin	100- Pin	64- Pin	145-/ 144- Pin	100- Pin	64- Pin
8-bit timer	TMO1 (output)	P17	○	○	○	○	○	○
		P26	○	○	○	○	○	○
	TMCI1 (input)	P02	○	×	×	○	×	×
		P12	○	○	○	○	○	○
		P54	○	○	×	○	○	×
		PC4	○	○	○	○	○	○
	TMRI1 (input)	P24	○	○	×	○	○	×
		PB5	○	○	○	○	○	○
	TMO2 (output)	P16	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	TMCI2 (input)	P15	○	○	×	○	○	×
		P31	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	TMRI2 (input)	P14	○	○	×	○	○	×
		PC5	○	○	○	○	○	○
	TMO3 (output)	P13	○	○	○	○	○	○
		P32	○	○	×	○	○	×
		P55	○	○	×	○	○	×
	TMCI3 (input)	P27	○	○	○	○	○	○
		P34	○	○	○	○	○	○
PA6		○	○	○	○	○	○	
TMRI3 (input)	P30	○	○	○	○	○	○	
	P33	○	○	×	○	○	×	
Compare match timer W	TOC0 (output)	PC7	○	○	○	○	○	○
	TIC0 (input)	PC6	○	○	○	○	○	○
	TOC1 (output)	PE7	○	○	○	○	○	○
	TIC1 (input)	PE6	○	○	○	○	○	○
	TOC2 (output)	PD3	○	○	○	○	○	○
	TIC2 (input)	PD2	○	○	○	○	○	○
	TOC3 (output)	PE3	○	○	×	○	○	×
	TIC3 (input)	PE2	○	○	○	○	○	○
Ethernet controller	REF50CK0 (input)	P76	○	×	×			
		PB2	○	○	×			
		PE5	○	○	×			
	RMII0_CRS_DV (input)	P83	○	×	×			
		PB7	○	○	×			
	RMII0_TXD0 (output)	P81	○	×	×			
		PB5	○	○	×			
	RMII0_TXD1 (output)	P82	○	×	×			
		PB6	○	○	×			
	RMII0_RXD0 (input)	P75	○	×	×			
		PB1	○	○	×			
	RMII0_RXD1 (input)	P74	○	×	×			
		PB0	○	○	×			
	RMII0_TXD_EN (output)	P80	○	×	×			
PA0		○	○	×				
PB4		○	○	×				

Module/ Function	Pin Function	Port Allocation	RX65N			RX671		
			145-/ 144- Pin	100- Pin	64- Pin	145-/ 144- Pin	100- Pin	64- Pin
Ethernet controller	RMII0_RX_ER (input)	P77	○	×	×			
		PB3	○	○	×			
	ET0_CRG (input)	P83	○	×	×			
		PB7	○	○	×			
	ET0_RX_DV (input)	PC2	○	○	×			
	ET0_EXOUT (output)	P55	○	○	×			
		PA6	○	○	×			
		PJ3	○	○	×			
	ET0_LINKSTA (input)	P34	○	○	×			
		P54	○	○	×			
		PA5	○	○	×			
	ET0_ETXD0 (output)	P81	○	×	×			
		PB5	○	○	×			
	ET0_ETXD1 (output)	P82	○	×	×			
		PB6	○	○	×			
	ET0_ETXD2 (output)	PC5	○	○	×			
	ET0_ETXD3 (output)	PC6	○	○	×			
	ET0_ERXD0 (input)	P75	○	×	×			
		PB1	○	○	×			
	ET0_ERXD1 (input)	P74	○	×	×			
		PB0	○	○	×			
	ET0_ERXD2 (input)	PC1	○	○	×			
		PE4	○	○	×			
	ET0_ERXD3 (input)	PC0	○	○	×			
		PE3	○	○	×			
	ET0_TX_EN (output)	P80	○	×	×			
		PA0	○	○	×			
		PB4	○	○	×			
	ET0_TX_ER (output)	PC3	○	○	×			
	ET0_RX_ER (input)	P77	○	×	×			
		PB3	○	○	×			
	ET0_TX_CLK (input)	PC4	○	○	×			
	ET0_RX_CLK (input)	P76	○	×	×			
		PB2	○	○	×			
		PE5	○	○	×			
	ET0_COL (input)	PC7	○	○	×			
	ET0_WOL (output)	P73	○	×	×			
		PA1	○	○	×			
		PA7	○	○	×			
	ET0_MDC (output)	P72	○	×	×			
PA4		○	○	×				
ET0_MDIO (input/output)	P71	○	×	×				
	PA3	○	○	×				

Module/ Function	Pin Function	Port Allocation	RX65N			RX671		
			145-/ 144- Pin	100- Pin	64- Pin	145-/ 144- Pin	100- Pin	64- Pin
Serial communications interface	RXD0 (input) / SMISO0	P21	○	○	×	○	○	×
	(input/output) / SSCL0 (input/output)	P33	○	○	×	○	○	×
	TXD0 (output) / SMOSI0	P20	○	○	×	○	○	×
	(input/output) / SSDA0 (input/output)	P32	○	○	×	○	○	×
	SCK0 (input/output)	P22	○	○	×	○	○	×
		P34	○	○	×	○	○	×
	CTS0# (input) / RTS0# (output) / SS0# (input)	P23	○	○	×	○	○	×
		PJ3	○	○	×	○	○	×
	RXD1 (input) / SMISO1	P15	○	○	×	○	○	×
		(input/output) / SSCL1 (input/output)	P30	○	○	○	○	○
	TXD1 (output) / SMOSI1	P16	○	○	○	○	○	○
		(input/output) / SSDA1 (input/output)	P26	○	○	○	○	○
	SCK1 (input/output)	P17	○	○	○	○	○	○
		P27	○	○	○	○	○	○
	CTS1# (input) / RTS1# (output) / SS1# (input)	P14	○	○	×	○	○	×
		P31	○	○	○	○	○	○
	RXD2 (input) / SMISO2	P12	○	○	○*6	○	○	○
		(input/output) / SSCL2 (input/output)	P52	○	○	×	○	○
	TXD2 (output) / SMOSI2	P13	○	○	○*6	○	○	○
		(input/output) / SSDA2 (input/output)	P50	○	○	×	○	○
	SCK2 (input/output)	P51	○	○	×	○	○	×
	CTS2# (input) / RTS2# (output) / SS2# (input)	P54	○	○	×	○	○	×
		PJ5	○	×	×	○	×	×
	RXD3 (input) / SMISO3	P16	○	○	○*6	○	○	○
		(input/output) / SSCL3 (input/output)	P25	○	○	×	○	○
	TXD3 (output) / SMOSI3	P17	○	○	○*6	○	○	○
		(input/output) / SSDA3 (input/output)	P23	○	○	×	○	○
	SCK3 (input/output)	P15	○	○	×	○	○	×
		P24	○	○	×	○	○	×
	CTS3# (input) / RTS3# (output) / SS3# (input)	P26	○	○	○*6	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX671		
			145-/ 144- Pin	100- Pin	64- Pin	145-/ 144- Pin	100- Pin	64- Pin
Serial communications interface	RXD4 (input) / SMISO4 (input/output) / SSCL4 (input/output)	PB0	○	×	×	○	×	×
	TXD4 (output) / SMOSI4 (input/output) / SSDA4 (input/output)	PB1	○	×	×	○	×	×
	SCK4 (input/output)	PB3	○	×	×	○	×	×
	CTS4# (input) / RTS4# (output) / SS4# (input)	PB2	○	×	×	○	×	×
	RXD5 (input) / SMISO5 (input/output) / SSCL5 (input/output)	PA2	○	○	○	○	○	○
		PA3	○	○	×	○	○	×
		PC2	○	○	×	○	○	×
	TXD5 (output) / SMOSI5 (input/output) / SSDA5 (input/output)	PA4	○	○	○	○	○	○
		PC3	○	○	×	○	○	×
	SCK5 (input/output)	PA1	○	○	○	○	○	○
		PC1	○	○	×	○	○	○
		PC4	○	○	×	○	○	○
	CTS5# (input) / RTS5# (output) / SS5# (input)	PA6	○	○	○	○	○	○
		PC0	○	○	×	○	○	○
	RXD6 (input) / SMISO6 (input/output) / SSCL6 (input/output)	P01	○	×	×	○	×	×
		P33	○	○	×	○	○	×
		PB0	○	○	×	○	○	×
	TXD6 (output) / SMOSI6 (input/output) / SSDA6 (input/output)	P00	○	×	×	○	×	×
		P32	○	○	×	○	○	×
		PB1	○	○	×	○	○	×
	SCK6 (input/output)	P02	○	×	×	○	×	×
		P34	○	○	×	○	○	×
		PB3	○	○	×	○	○	×
	CTS6# (input) / RTS6# (output) / SS6# (input)	PB2	○	○	×	○	○	×
		PJ3	○	○	×	○	○	×
	RXD7 (input) / SMISO7 (input/output) / SSCL7 (input/output)	P92	○	×	×	○	×	×
	TXD7 (output) / SMOSI7 (input/output) / SSDA7 (input/output)	P55	○*2	×	×	○	×	×
		P90	○	×	×	○	×	×
	SCK7 (input/output)	P56	○*2	×	×	○	×	×
		P91	○	×	×	○	×	×

Module/ Function	Pin Function	Port Allocation	RX65N			RX671		
			145-/ 144- Pin	100- Pin	64- Pin	145-/ 144- Pin	100- Pin	64- Pin
Serial communications interface	CTS7# (input) / RTS7# (output) / SS7# (input)	P93	○	×	×	○	×	×
	RXD8 (input) / SMISO8 (input/output) / SSCL8 (input/output)	PC6	○	○	○	○	○	○
	TXD8 (output) / SMOSI8 (input/output) / SSDA8 (input/output)	PC7	○	○	○	○	○	○
	SCK8 (input/output)	PC5	○	○	○	○	○	○
	CTS8# (input) / RTS8# (output) / SS8# (input)	PC4	○	○	○	○	○	○
	RXD9 (input) / SMISO9 (input/output) / SSCL9 (input/output)	PB6	○	○	○*6	○	○	○
	TXD9 (output) / SMOSI9 (input/output) / SSDA9 (input/output)	PB7	○	○	○*6	○	○	○
	SCK9 (input/output)	PB5	○	○	○	○	○	○
	CTS9# (input) / RTS9# (output) / SS9# (input)	PB4	○	○	×	○	○	×
	RXD10 (input) / SMISO10 (input/output) / SSCL10 (input/output)	P81	○	×	×	○	×	×
		P86	○	×	×	○	×	×
		PC6	○	○	○	○	○	○
	TXD10 (output) / SMOSI10 (input/output) / SSDA10 (input/output)	P82	○	×	×	○	×	×
		P87	○	×	×	○	×	×
		PC7	○	○	○	○	○	○
	SCK10 (input/output)	P80	○	×	×	○	×	×
		P83	○	×	×	○	×	×
		PC5	○	○	○	○	○	○
	RTS10# (output)	P80	○	×	×	○	×	×
	CTS10# (input) / SS10# (input)	P83	○	×	×	○	×	×
	CTS10# (input) / RTS10# (output) / SS10# (input)	PC4	○	○	○	○	○	○
	RXD11 (input) / SMISO11 (input/output) / SSCL11 (input/output)	P76	○	×	×	○	×	×
PB6		○	○	○*6	○	○	○	

Module/ Function	Pin Function	Port Allocation	RX65N			RX671		
			145-/ 144- Pin	100- Pin	64- Pin	145-/ 144- Pin	100- Pin	64- Pin
Serial communications interface	TXD11 (output) / SMOSI11 (input/output) / SSDA11 (input/output)	P77	○	×	×	○	×	×
		PB7	○	○	○*6	○	○	○
	SCK11 (input/output)	P75	○	×	×	○	×	×
		PB5	○	○	○	○	○	○
	RTS11# (output)	P75	○	×	×	○	×	×
	CTS11# (input) / SS11# (input)	P74	○	×	×	○	×	×
	CTS11# (input) / RTS11# (output) / SS11# (input)	PB4	○	○	×	○	○	×
	RXD12 (input) / SMISO12 (input/output) / SSCL12 (input/output) / RXDX12 (input)	PE2	○	○	○*6	○	○	○
		PA2	×	×	×	○	○	○
	TXD12 (output) / SMOSI12 (input/output) / SSDA12 (input/output) / TXDX12 (output) / SIOX12 (input/output)	PE1	○	○	○*6	○	○	○
		PA4	×	×	×	○	○	○
	SCK12 (input/output)	PE0	○	○	○	○	○	○
PA1		×	×	×	○	○	○	
I <sup>2</sup> C bus interface	CTS12# (input) / RTS12# (output) / SS12# (input)	PE3	○	○	×	○	○	×
		PA6	×	×	×	○	○	○
	SCL0[FM+] (input/output)	P12	○	○	○	○	○	○
	SDA0[FM+] (input/output)	P13	○	○	○	○	○	○
	SCL1 (input/output)	P21	○	○	×	○	○	×
	SDA1 (input/output)	P20	○	○	×	○	○	×
	SCL2-DS (input/output)	P16	○	○	○	○	○	○
	SDA2-DS (input/output)	P17	○	○	○	○	○	○
USB 2.0 FS Host/Function module	USB0_VBUS (input)	P16	○	○	○	○	○	○
	USB0_EXICEN (output)	P21	○	○	×	○	○	×
	USB0_VBUSEN (output)	P16	○	○	×	○	○	×
		P24	○	○	×	○	○	×
		P32	○	○	×	○	○	×
	USB0_OVRCURA (input)	P14	○	○	×	○	○	×



Module/ Function	Pin Function	Port Allocation	RX65N			RX671		
			145-/ 144- Pin	100- Pin	64- Pin	145-/ 144- Pin	100- Pin	64- Pin
USB 2.0 FS Host/Function module	USB0_OVRCURB (input)	P16	○	○	×	○	○	×
		P22	○	○	×	○	○	×
	USB0_ID (input)	P20	○	○	×	○	○	×
	USB0_DP (input/output)*1	PH1				○	○	○
	USB0_DM (input/output)*1	PH2				○	○	○
	USB1_VBUS (input)	P73				○*4	×	×
	USB1_EXICEN (output)	P80				○*4	×	×
	USB1_VBUSEN (output)	P73				○*4	×	×
		P74				○*4	×	×
		P82				○*4	×	×
	USB1_OVRCURA (input)	P75				○*4	×	×
	USB1_OVRCURB (input)	P73				○*4	×	×
		P81				○*4	×	×
USB1_ID (input)	P77				○*4	×	×	
CAN module	CRX0 (input)	P33	○	○	×	○	○	×
		PD2	○	○	×	○	○	×
	CTX0 (output)	P32	○	○	×	○	○	×
		PD1	○	○	×	○	○	×
	CRX1-DS (input)	P15	○	○	×	○	○	×
	CRX1 (input)	P55	○	○	×	○	○	×
	CTX1 (output)	P14	○	○	×	○	○	×
		P54	○	○	×	○	○	×
Serial peripheral interface	RSPCKA (input/output)	PA5	○	○	×	○	○	×
		PC5	○	○	○	○	○	○
	MOSIA (input/output)	PA6	○	○	×	○	○	○
		PC6	○	○	○	○	○	○
	MISOA (input/output)	PA7	○	○	×	○	○	○
		PC7	○	○	○	○	○	○
	SSLA0 (input/output)	PA4	○	○	×	○	○	○
		PC4	○	○	○	○	○	○
	SSLA1 (output)	PA0	○	○	×	○	○	×
		PC0	○	○	○	○	○	○
	SSLA2 (output)	PA1	○	○	×	○	○	○
		PC1	○	○	○	○	○	○
	SSLA3 (output)	PA2	○	○	×	○	○	○
		PC2	○	○	×	○	○	×
	RSPCKB (input/output)	P27	○	○	○	○	○	○
		PE5	○	○	×	○	○	×
	MOSIB (input/output)	P26	○	○	○	○	○	○
		PE6	○	○	×	○	○	○
	MISOB (input/output)	P30	○	○	○	○	○	○
		PE7	○	○	×	○	○	○
SSLB0 (input/output)	P31	○	○	○	○	○	○	
	PE4	○	○	×	○	○	×	

Module/ Function	Pin Function	Port Allocation	RX65N			RX671		
			145-/ 144- Pin	100- Pin	64- Pin	145-/ 144- Pin	100- Pin	64- Pin
Serial peripheral interface	SSLB1 (output)	P50	○	○	×	○	○	×
		PE0	○	○	×	○	○	○
	SSLB2 (output)	P51	○	○	×	○	○	×
		PE1	○	○	×	○	○	○
	SSLB3 (output)	P52	○	○	×	○	○	×
		PE2	○	○	×	○	○	○
	RSPCKC (input/output)	P56	×	×	×	○	×	×
		PD3	○	○	×	○	○	×
	MOSIC (input/output)	P54	×	×	×	○	○	×
		PD1	○	○	×	○	○	×
	MISOC (input/output)	P55	×	×	×	○	○	×
		PD2	○	○	×	○	○	×
	SSLC0 (input/output)	P57	×	×	×	×	×	×
		PD4	○	○	×	○	○	×
	SSLC1 (output)	PD5	○	○	×	○	○	×
		PJ0	×	×	×	×	×	×
	SSLC2 (output)	PD6	○	○	×	○	○	×
		PJ1	×	×	×	×	×	×
SSLC3 (output)	PD7	○	○	×	○	○	×	
	PJ2	×	×	×	×	×	×	
Realtime clock	RTCOU (output)	P16	○	○	○	○	○	○
		P32	○	○	×	○	○	×
	RTCIC0 (input)* <sup>1</sup>	P30	○	○	○	○	○	○
	RTCIC1 (input)* <sup>1</sup>	P31	○	○	○	○	○	○
	RTCIC2 (input)* <sup>1</sup>	P32	○	○	×	○	○	×
12-bit A/D converter	AN000 (input)* <sup>1</sup>	P40	○	○	○	○	○	○
		P41	○	○	○	○	○	○
	AN001 (input)* <sup>1</sup>	P42	○	○	○	○	○	○
		P43	○	○	○	○	○	○
	AN002 (input)* <sup>1</sup>	P44	○	○	×	○	○	×
		P45	○	○	×	○	○	×
	AN003 (input)* <sup>1</sup>	P46	○	○	×	○	○	×
		P47	○	○	×	○	○	×
	ADTRG0# (input)	P07	○	○	×	○	○	×
		P16	○	○	○	○	○	○
		P25	○	○	×	○	○	×
	AN100 (input)* <sup>1</sup>	PE2	○	○	×	×	×	×
		PD7	×	×	×	○	○	○
	AN101 (input)* <sup>1</sup>	PE3	○	○	×	×	×	×
		PD6	×	×	×	○	○	○
	AN102 (input)* <sup>1</sup>	PE4	○	○	×	×	×	×
		PD5	×	×	×	○	○	○
	AN103 (input)* <sup>1</sup>	PE5	○	○	×	×	×	×
		PD4	×	×	×	○	○	○
	AN104 (input)* <sup>1</sup>	PE6	○	○	×	×	×	×
		PD3	×	×	×	○	○	○
	AN105 (input)* <sup>1</sup>	PE7	○	○	×	×	×	×
		PD2	×	×	×	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX671		
			145-/ 144- Pin	100- Pin	64- Pin	145-/ 144- Pin	100- Pin	64- Pin
12-bit A/D converter	AN106 (input)*1	PD6	○	○	○	×	×	×
		PD1	×	×	×	○	○	×
	AN107 (input)*1	PD7	○	○	○	×	×	×
		PD0	×	×	×	○	○	×
	AN108 (input)*1	PD0	○	○	×	×	×	×
		P90	×	×	×	○	×	×
	AN109 (input)*1	PD1	○	○	×	×	×	×
		P02	×	×	×	○	×	×
	AN110 (input)*1	PD2	○	○	○	×	×	×
		P01	×	×	×	○	×	×
	AN111 (input)*1	PD3	○	○	○	×	×	×
		P00	×	×	×	○	×	×
	AN112 (input)*1	PD4	○	○	○			
	AN113 (input)*1	PD5	○	○	○			
	AN114 (input)*1	P90	○	×	×			
	AN115 (input)*1	P91	○	×	×			
	AN116 (input)*1	P92	○	×	×			
	AN117 (input)*1	P93	○	×	×			
	AN118 (input)*1	P00	○	×	×			
	AN119 (input)*1	P01	○	×	×			
AN120 (input)*1	P02	○	×	×				
ANEX0 (output)*1	PE0	○	○	○	○	○	○	
ANEX1 (input)*1	PE1	○	○	○	○	○	○	
ADTRG1# (input)	P13	○	○	○	○	○	○	
	P17	○	○	○	○	○	○	
12-bit D/A converter	DA0 (output)*1	P03	○	×	×			
	DA1 (output)*1	P05	○	○	○*5			
Parallel data capture unit	PIXCLK (input)	P24	○	×	×			
	VSYNC (input)	P32	○	×	×			
	HSYNC (input)	P25	○	×	×			
	PIXD0 (input)	P15	○	×	×			
	PIXD1 (input)	P86	○	×	×			
	PIXD2 (input)	P87	○	×	×			
	PIXD3 (input)	P17	○	×	×			
	PIXD4 (input)	P20	○	×	×			
	PIXD5 (input)	P21	○	×	×			
	PIXD6 (input)	P22	○	×	×			
	PIXD7 (input)	P23	○	×	×			
PCKO (output)	P33	○	×	×				
MMC host interface	MMC_RES# (output)	P75	○	×	×			
		PE7	○	○	×			
	MMC_CLK (output)	P77	○	×	×			
		PD5	○	○	×			
	MMC_CD (input)	PC2	○	×	×			
		PE6	○	○	×			
MMC_CMD (input/output)	P76	○	×	×				
	PD4	○	○	×				

Module/ Function	Pin Function	Port Allocation	RX65N			RX671		
			145-/ 144- Pin	100- Pin	64- Pin	145-/ 144- Pin	100- Pin	64- Pin
MMC host interface	MMC_D0 (input/output)	PC3	○	×	×			
		PD6	○	○	×			
	MMC_D1 (input/output)	PC4	○	×	×			
		PD7	○	○	×			
	MMC_D2 (input/output)	P80	○	×	×			
		PD2	○	○	×			
	MMC_D3 (input/output)	P81	○	×	×			
		PD3	○	○	×			
	MMC_D4 (input/output)	P82	○	×	×			
		PE0	○	○	×			
	MMC_D5 (input/output)	PC5	○	×	×			
		PE1	○	○	×			
	MMC_D6 (input/output)	PC6	○	×	×			
		PE2	○	○	×			
MMC_D7 (input/output)	PC7	○	×	×				
	PE3	○	○	×				
SD host interface	SDHI_CLK (output)	P21	○*2	×	×	○	○	×
		P77	○	×	×	○	×	×
		PD5	○	○	○	○	○	○
	SDHI_CMD (input/output)	P20	○*2	×	×	○	○	×
		P76	○	×	×	○	×	×
		PD4	○	○	○	○	○	○
	SDHI_CD (input)	P25	○*2	×	×	○	○	×
		P81	○	×	×	○	×	×
		PE6	○	○	○	○	○	○
		PA1	×	×	×	○	○	○
	SDHI_WP (input)	P24	○*2	×	×	○	○	×
		P80	○	×	×	○	×	×
		PE7	○	○	○	○	○	○
		PA2	×	×	×	○	○	○
	SDHI_D0 (input/output)	P22	○*2	×	×	○	○	×
		PC3	○	×	×	○	○	×
		PD6	○	○	○	○	○	○
		PE6	×	×	×	○	○	○
	SDHI_D1 (input/output)	P23	○*2	×	×	○	○	×
		PC4	○	×	×	○	○	○
		PD7	○	○	○	○	○	○
		PE7	×	×	×	○	○	○
	SDHI_D2 (input/output)	P75	○	×	×	○	×	×
		P87	○*2	×	×	○	×	×
PD2		○	○	○	○	○	○	
SDHI_D3 (input/output)	P17	○*2	×	×	○	○	○	
	PC2	○	×	×	○	○	×	
	PD3	○	○	○	○	○	○	

Module/ Function	Pin Function	Port Allocation	RX65N			RX671		
			145-/ 144- Pin	100- Pin	64- Pin	145-/ 144- Pin	100- Pin	64- Pin
SD slave interface	SDSI_CLK (input)	P77	○	×	×			
		PB5	○	○	×			
	SDSI_CMD (input/output)	P76	○	×	×			
		PB4	○	○	×			
	SDSI_D0 (input/output)	PC3	○	×	×			
		PB6	○	○	×			
	SDSI_D1 (input/output)	PC4	○	×	×			
		PB7	○	○	×			
SDSI_D2 (input/output)	P75	○	×	×				
	PB2	○	○	×				
SDSI_D3 (input/output)	PC2	○	×	×				
	PB3	○	○	×				
Clock frequency measurement circuit	CACREF (input)	PC7	○	○	○	○	○	○
		PA0	○	○	×	○	○	×
Quad serial peripheral interface (RX65N)/ quad SPI memory interface (RX671)	QSPCLK (input/output)	P77	○	×	×	○	×	×
		PD5	○	○	○	○	○	○
	QSSL (input/output)	P76	○	×	×	○	×	×
		PD4	○	○	○	○	○	○
	QMO/QIO0 (input/output)	PC3	●	×	×	○	○	×
		PD6	●	●	●	○	○	○
		PE6	×	×	×	○	○	○
	QMI/QIO1 (input/output)	PC4	●	×	×	○	○	○
		PD7	●	●	●	○	○	○
		PE7	×	×	×	○	○	○
	QIO2 (input/output)	P80	○	×	×	○	×	×
		PD2	○	○	○	○	○	○
QIO3 (input/output)	P81	○	×	×	○	×	×	
	PD3	○	○	○	○	○	○	
LCD control*2	LCD_EXTCLK (input)	PD0	○	○	×			
	LCD_CLK (output)	PB5	○	○	×			
	LCD_TCON0 (output)	PB4	○	○	×			
	LCD_TCON1 (output)	PB3	○	○	×			
	LCD_TCON2 (output)	PB2	○	○	×			
	LCD_TCON3 (output)	PB1	○	○	×			
	LCD_DATA0 (output)	PB0	○	○	×			
	LCD_DATA1 (output)	PA7	○	○	×			
	LCD_DATA2 (output)	PA6	○	○	×			
	LCD_DATA3 (output)	PA5	○	○	×			
	LCD_DATA4 (output)	PA4	○	○	×			
	LCD_DATA5 (output)	PA3	○	○	×			
	LCD_DATA6 (output)	PA2	○	○	×			
	LCD_DATA7 (output)	PA1	○	○	×			
LCD_DATA8 (output)	PA0	○	○	×				

Module/ Function	Pin Function	Port Allocation	RX65N			RX671		
			145-/ 144- Pin	100- Pin	64- Pin	145-/ 144- Pin	100- Pin	64- Pin
LCD control*2	LCD_DATA9 (output)	PE7	○	○	×			
	LCD_DATA10 (output)	PE6	○	○	×			
	LCD_DATA11 (output)	PE5	○	○	×			
	LCD_DATA12 (output)	PE4	○	○	×			
	LCD_DATA13 (output)	PE3	○	○	×			
	LCD_DATA14 (output)	PE2	○	○	×			
	LCD_DATA15 (output)	PE1	○	○	×			
	LCD_DATA16 (output)	PE0	○	○	×			
	LCD_DATA17 (output)	PD7	○	○	×			
	LCD_DATA18 (output)	PD6	○	○	×			
	LCD_DATA19 (output)	PD5	○	○	×			
	LCD_DATA20 (output)	PD4	○	○	×			
	LCD_DATA21 (output)	PD3	○	○	×			
	LCD_DATA22 (output)	PD2	○	○	×			
	LCD_DATA23 (output)	PD1	○	○	×			
Battery backup	TAMPIO (input)*1	P30				○	○	○
	TAMPI1 (input)*1	P31				○	○	○
	TAMPI2 (input)*1	P32				○	○	×
Serial communications interface	RXD010 (input) / SMISO010 (input/output) / SSCL010 (input/output)	P81				○	×	×
		P86				○	×	×
		PC6				○	○	○
	TXD010 (output) / SMOSI010 (input/output) / SSDA010 (input/output)	P82				○	×	×
		P87				○	×	×
		PC7				○	○	○
	SCK010 (input/output)	P80				○	×	×
		P83				○	×	×
		PC5				○	○	○
	RTS010# (output)	P80				○	×	×
CTS010# (input) / SS010# (input)	P83				○	×	×	
CTS010# (input) / RTS010# (output) / SS010# (input)	PC4				○	○	○	

Module/ Function	Pin Function	Port Allocation	RX65N			RX671		
			145-/ 144- Pin	100- Pin	64- Pin	145-/ 144- Pin	100- Pin	64- Pin
Serial communications interface	DE010 (output)	P80				○	×	×
		PC4				○	○	○
	RXD011 (input) / SMISO011 (input/output) / SSCL011 (input/output)	P76				○	×	×
		PB6				○	○	○
	TXD011 (output) / SMOSI011 (input/output) / SSDA011 (input/output)	PC0				○	○	○
		P77				○	×	×
		PB7				○	○	○
	SCK011 (input/output)	PC1				○	○	○
		P75				○	×	×
	TXDA011 (output)	PB5				○	○	○
		PC1				○	○	○
	TXDB011 (output)	PC2				○	○	×
	RTS011# (output)	P75				○	×	×
	CTS011# (input) / SS011# (input)	P74				○	×	×
		PB4				○	○	×
CTS011# (input) / RTS011# (output) / SS011# (input)								
	DE011 (output)	P75				○	×	×
PB4					○	○	×	
High-speed I <sup>2</sup> C bus interface	SCLHS0[FM+ /HS] (input/output)	P12				○	○	○
	SDAHS0[FM+ /HS] (input/output)	P13				○	○	○
Serial peripheral interface	RSPCK0 (input/output)	PA5				○	○	×
		PC5				○	○	○
	MOSI0 (input/output)	PA6				○	○	○
		PC6				○	○	○
	MISO0 (input/output)	PA7				○	○	○
		PC7				○	○	○
	SSL00 (input/output)	PA4				○	○	○
		PC4				○	○	○
	SSL01 (output)	PA0				○	○	×
		PC0				○	○	○
	SSL02 (output)	PA1				○	○	○
		PC1				○	○	○
SSL03 (output)	PA2				○	○	○	
	PC2				○	○	×	

Module/ Function	Pin Function	Port Allocation	RX65N			RX671		
			145-/ 144- Pin	100- Pin	64- Pin	145-/ 144- Pin	100- Pin	64- Pin
Serial sound interface	AUDIO_CLK (input)	P22				○	○	×
		PC4				○	○	○
	SSIBCK0 (input/output)	P23				○	○	×
		PC5				○	○	○
	SSILRCK0 (input/output)	P21				○	○	×
		PC6				○	○	○
	SSIRXD0 (input)	P20				○	○	×
		P53				○	○	○
SSITXD0 (output)	P17				○	○	○	
	PC7				○	○	○	
Clock generation circuit	CLKOUT (output)	P25				○	○	×
	EXCIN (input)*1	PJ3				○	○	×
	EXTAL (input)*1	P36	○	○	○	○	○	○
	XTAL (output)*1	P37	○	○	○	○	○	○
Capacitive touch sensing unit	TSCAP (—)	PC4				○	○	○
	TS0 (output)	P34				○	○	○
	TS1 (output)	P33				○	○	×
	TS2 (output)	P27				○	○	○
	TS3 (output)	P26				○	○	○
	TS4 (output)	P25				○	○	×
	TS5 (output)	P24				○	○	×
	TS6 (output)	P23				○	○	×
	TS7 (output)	P22				○	○	×
	TS8 (output)	P21				○	○	×
	TS9 (output)	P20				○	○	×
	TS10 (output)	P15				○	○	×
	TS11 (output)	P14				○	○	×
	TS12 (output)	P53				○	○	○
	TS13 (output)	PC6				○	○	○
	TS14 (output)	PC5				○	○	○
TS15 (output)	PC1				○	○	○	
TS16 (output)	PC0				○	○	○	
Remote control signal receiver	PMC0-DS (input)*1	P53				○	○	○
		PB3				○	○	×
		PC3				○	○	×

Notes: 1. For these pin functions, ensure that the corresponding pin is set as general input (PORTm.PDR.Bn and PORTm.PMR.Bn bits cleared to 0).

2. Not supported on products with a code flash memory capacity of 1 MB or less.
3. Not present on the 145-pin TFLGA product.
4. Supported on the 145-pin TFLGA product only.
5. Supported on the 64-pin TFBGA product only.
6. Simple SPI mode is not supported.



**Table 2.32 Comparison of P0n Pin Function Control Register (P0nPFS)**

Register	Bit	RX65N (n = 0 to 3, 5, 7)	RX671 (n = 0 to 3, 5, 7)
P0nPFS	ASEL	Analog function select bit  0: Used as other than as analog pin 1: Used as analog pin P00: AN118 (177/176/145/144-pin) P01: AN119 (177/176/145/144-pin) P02: AN120 (177/176/145/144-pin) P03: DA0 (177/176/145/144-pin) P05: DA1 (177/176/145/144/100/ 64-pin)	Analog function select bit  0: Used as other than as analog pin 1: Used as analog pin P00: AN111 (145/144-pin) P01: AN110 (145/144-pin) P02: AN109 (145/144-pin)

**Table 2.33 Comparison of P1n Pin Function Control Register (P1nPFS)**

Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 2 to 7)
P10PFS	—	P10 pin function control register	—
P11PFS	—	P11 pin function control register	—
P12PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIC5U 000101b: TMC11 001010b: RXD2/SMISO2/SSCL2 001111b: SCL0[FM+] 100101b: LCD_TCON1-A*1	Pin function select bits  000000b: Hi-Z 000001b: MTIC5U 000101b: TMC11 001010b: RXD2/SMISO2/SSCL2 001111b: SCL0[FM+] 101111b: SCLHS0[FM+/HS]
P13PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC0B 000011b: TIOCA5 000101b: TMO3 000110b: PO13 001001b: ADTRG1# 001010b: TXD2/SMOSI2/SSDA2 001111b: SDA0[FM+] 100101b: LCD_TCON0-A*1	Pin function select bits  000000b: Hi-Z 000001b: MTIOC0B 000011b: TIOCA5 000101b: TMO3 000110b: PO13 001001b: ADTRG1# 001010b: TXD2/SMOSI2/SSDA2 001111b: SDA0[FM+] 101111b: SDAHS0[FM+/HS]
P14PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000011b: TIOCB5 000100b: TCLKA 000101b: TMRI2 000110b: PO15 001011b: CTS1#/RTS1#/SS1# 010000b: CTX1 010010b: USB0_OVRCURA 100101b: LCD_CLK-A*1	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000011b: TIOCB5 000100b: TCLKA 000101b: TMRI2 000110b: PO15 001011b: CTS1#/RTS1#/SS1# 010000b: CTX1 010010b: USB0_OVRCURA 101011b: TS11

Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 2 to 7)
P15PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKB 000011b: TIOCB2 000100b: TCLKB 000101b: TMC12 000110b: PO13 001010b: RXD1/SMISO1/SSCL1 001011b: SCK3 010000b: CRX1-DS 011100b: PIXD0	Pin function select bits  000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKB 000011b: TIOCB2 000100b: TCLKB 000101b: TMC12 000110b: PO13 001010b: RXD1/SMISO1/SSCL1 001011b: SCK3 010000b: CRX1-DS  101011b: TS10
P17PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3A 000010b: MTIOC3B 000011b: TIOCB0 000100b: TCLKD 000101b: TMO1 000110b: PO15 000111b: POE8# 001000b: MTIOC4B 001001b: ADTRG1# 001010b: SCK1 001011b: TXD3/SMOSI3/SSDA3 001111b: SDA2-DS  011010b: SDHI_D3-C*1 011100b: PIXD3	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3A 000010b: MTIOC3B 000011b: TIOCB0 000100b: TCLKD 000101b: TMO1 000110b: PO15 000111b: POE8# 001000b: MTIOC4B 001001b: ADTRG1# 001010b: SCK1 001011b: TXD3/SMOSI3/SSDA3 001111b: SDA2-DS  010111b: SSITXD0 011010b: SDHI_D3-C
P1nPFS	ISEL	Interrupt input function select bit  0: Not used as IRQn input pin 1: Used as IRQn input pin P10: IRQ0 (177/176-pin) P11: IRQ1 (177/176-pin) P12: IRQ2 (177/176/145/144/100/64-pin) P13: IRQ3 (177/176/145/144/100/64-pin) P14: IRQ4 (177/176/145/144/100-pin) P15: IRQ5 (177/176/145/144/100-pin) P16: IRQ6 (177/176/145/144/100/64-pin) P17: IRQ7 (177/176/145/144/100/64-pin)	Interrupt input function select bit  0: Not used as IRQn input pin 1: Used as IRQn input pin  P12: IRQ2 (145/144/100/64/48-pin) P13: IRQ3 (145/144/100/64/48-pin) P14: IRQ4 (145/144/100-pin) P15: IRQ5 (145/144/100-pin) P16: IRQ6 (145/144/100/64/48-pin) P17: IRQ7 (145/144/100/64/48-pin)

Note: 1. Not supported on products with a code flash memory capacity of 1 MB or less.

**Table 2.34 Comparison of P2n Pin Function Control Register (P2nPFS)**

Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 0 to 7)
P20PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC1A 000011b: TIOCB3 000101b: TMRIO 000110b: PO0 001010b: TXD0/SMOSIO/SSDA0 001111b: SDA1*1 010011b: USB0_ID  011010b: SDHI_CMD-C*1 011100b: PIXD4	Pin function select bits  000000b: Hi-Z 000001b: MTIOC1A 000011b: TIOCB3 000101b: TMRIO 000110b: PO0 001010b: TXD0/SMOSIO/SSDA0 001111b: SDA1 010011b: USB0_ID 010111b: SSIRXD0 011010b: SDHI_CMD-C  101011b: TS9
P21PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC1B 000011b: TIOCA3 000101b: TMCIO 000110b: PO1 001000b: MTIOC4A 001010b: RXD0/SMISO0/SSCL0 001111b: SCL1*1 010011b: USB0_EXICEN  011010b: SDHI_CLK-C*1 011100b: PIXD5	Pin function select bits  000000b: Hi-Z 000001b: MTIOC1B 000011b: TIOCA3 000101b: TMCIO 000110b: PO1 001000b: MTIOC4A 001010b: RXD0/SMISO0/SSCL0 001111b: SCL1 010011b: USB0_EXICEN 010111b: SSILRCK0 011010b: SDHI_CLK-C  101011b: TS8
P22PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKC 000011b: TIOCC3 000101b: TMO0 000110b: PO2 001010b: SCK0 010011b: USB0_OVRCURB  011000b: EDREQ0 011010b: SDHI_D0-C*1 011100b: PIXD6	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKC 000011b: TIOCC3 000101b: TMO0 000110b: PO2 001010b: SCK0 010011b: USB0_OVRCURB 010111b: AUDIO_CLK 011000b: EDREQ0 011010b: SDHI_D0-C  101011b: TS7

Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 0 to 7)
P23PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKD 000011b: TIOCD3 000110b: PO3 001010b: TXD3/SMOSI3/SSDA3 001011b: CTS0#/RTS0#/SS0#  011000b: EDACK0 011010b: SDHI_D1-C*1 011100b: PIXD7	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKD 000011b: TIOCD3 000110b: PO3 001010b: TXD3/SMOSI3/SSDA3 001011b: CTS0#/RTS0#/SS0# 010111b: SSIBCK0 011000b: EDACK0 011010b: SDHI_D1-C  101011b: TS6
P24PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4A 000010b: MTCLKA 000011b: TIOCB4 000101b: TMR11 000110b: PO4 001010b: SCK3 010011b: USB0_VBUSEN 011000b: EDREQ1 011010b: SDHI_WP*1 011100b: PIXCLK	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4A 000010b: MTCLKA 000011b: TIOCB4 000101b: TMR11 000110b: PO4 001010b: SCK3 010011b: USB0_VBUSEN 011000b: EDREQ1 011010b: SDHI_WP  101011b: TS5
P25PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4C 000010b: MTCLKB 000011b: TIOCA4 000110b: PO5 001001b: ADTRG0# 001010b: RXD3/SMISO3/SSCL3 011000b: EDACK1 011010b: SDHI_CD*1 011100b: HSYNC	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4C 000010b: MTCLKB 000011b: TIOCA4 000110b: PO5 001001b: ADTRG0# 001010b: RXD3/SMISO3/SSCL3 011000b: EDACK1 011010b: SDHI_CD  101010b: CLKOUT 101011b: TS4
P26PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC2A 000101b: TMO1 000110b: PO6 001010b: TXD1/SMOSI1/SSDA1 001011b: CTS3#/RTS3#/SS3# 001101b: MOSIB-A	Pin function select bits  000000b: Hi-Z 000001b: MTIOC2A 000101b: TMO1 000110b: PO6 001010b: TXD1/SMOSI1/SSDA1 001011b: CTS3#/RTS3#/SS3# 001101b: MOSIB-A  101011b: TS3

Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 0 to 7)
P27PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC2B 000101b: TMCi3 000110b: PO7 001010b: SCK1 001101b: RSPCKB-A	Pin function select bits  000000b: Hi-Z 000001b: MTIOC2B 000101b: TMCi3 000110b: PO7 001010b: SCK1 001101b: RSPCKB-A 101011b: TS2
P2nPFS	ISEL	Interrupt input function select bit  0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ8 (177/176/145/144/100-pin) P21: IRQ9 (177/176/145/144/100-pin)	Interrupt input function select bit  0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ8 (145/144/100-pin) P21: IRQ9 (145/144/100-pin) P22: IRQ15 (145/144/100-pin) P23: IRQ3 (145/144/100-pin) P24: IRQ12 (145/144/100-pin) P25: IRQ5 (145/144/100-pin) P26: IRQ6 (145/144/100/64/48-pin) P27: IRQ7 (145/144/100/64/48-pin)

Note: 1. Not supported on products with a code flash memory capacity of 1 MB or less.

**Table 2.35 Comparison of P3n Pin Function Control Register (P3nPFS)**

Register	Bit	RX65N (n = 0 to 4)	RX671 (n = 0 to 4)
P32PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC0C 000011b: TIOCC0 000101b: TMO3 000110b: PO10 000111b: RTCOUT 001000b: POE0# 001010b: TXD6/SMOSI6/SSDA6 001011b: TXD0/SMOSI0/SSDA0 010000b: CTX0 010011b: USB0_VBUSEN 011100b: VSYNC 100001b: POE10#	Pin function select bits  000000b: Hi-Z 000001b: MTIOC0C 000011b: TIOCC0 000101b: TMO3 000110b: PO10 000111b: RTCOUT 001000b: POE0# 001010b: TXD6/SMOSI6/SSDA6 001011b: TXD0/SMOSI0/SSDA0 010000b: CTX0 010011b: USB0_VBUSEN  100001b: POE10#
P33PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC0D 000011b: TIOCD0 000101b: TMRI3 000110b: PO11 001000b: POE4# 001010b: RXD6/SMISO6/SSCL6 001011b: RXD0/SMISO0/SSCL0 010000b: CRX0 011000b: EDREQ1 011100b: PCKO 100001b: POE11#	Pin function select bits  000000b: Hi-Z 000001b: MTIOC0D 000011b: TIOCD0 000101b: TMRI3 000110b: PO11 001000b: POE4# 001010b: RXD6/SMISO6/SSCL6 001011b: RXD0/SMISO0/SSCL0 010000b: CRX0 011000b: EDREQ1  100001b: POE11# 101011b: TS1
P34PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC0A 000101b: TMCi3 000110b: PO12 000111b: POE10# 001010b: SCK6 001011b: SCK0 010001b: ET0_LINKSTA	Pin function select bits  000000b: Hi-Z 000001b: MTIOC0A 000101b: TMCi3 000110b: PO12 000111b: POE10# 001010b: SCK6 001011b: SCK0  101011b: TS0

**Table 2.36 Comparison of P5n Pin Function Control Register (P5nPFS)**

Register	Bit	RX65N (n = 0 to 2, 4 to 7)	RX671 (n = 0 to 6)
P53PFS	—	—	P53 pin function control register
P54PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4B 000101b: TMC11 001011b: CTS2#/RTS2#/SS2# 001101b: MOSIC-B 010000b: CTX1 010001b: ET0_LINKSTA 011000b: EDACK0 100101b: LCD_DATA6-A	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4B 000101b: TMC11 001011b: CTS2#/RTS2#/SS2# 001101b: MOSIC-B 010000b: CTX1  011000b: EDACK0
P55PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4D 000101b: TMO3 001010b: TXD7/SMOSI7/SSDA7 001101b: MISOC-B 010000b: CRX1 010001b: ET0_EXOUT 011000b: EDREQ0 100101b: LCD_DATA5-A	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4D 000101b: TMO3 001010b: TXD7/SMOSI7/SSDA7 001101b: MISOC-B 010000b: CRX1  011000b: EDREQ0
P56PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3C 000011b: TIOCA1 001010b: SCK7*1 001101b: RSPCKC-B 011000b: EDACK1 100101b: LCD_DATA4-A	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3C 000011b: TIOCA1 001010b: SCK7 001101b: RSPCKC-B 011000b: EDACK1
P57PFS	—	P57 pin function control register	—
P5nPFS	ISEL	Interrupt input function select bit  0: Not used as IRQn input pin 1: Used as IRQn input pin  P55: IRQ10 (177/176/145/144/100-pin)	Interrupt input function select bit  0: Not used as IRQn input pin 1: Used as IRQn input pin  P50: IRQ0 (145/144/100-pin) P51: IRQ1 (145/144/100-pin) P52: IRQ2 (145/144/100-pin) P53: IRQ3 (145/144/100/64/48-pin) P54: IRQ4 (145/144/100-pin) P55: IRQ10 (145/144/100-pin)  P56: IRQ6 (145/144-pin)

Note: 1. Not supported on products with a code flash memory capacity of 1 MB or less.

**Table 2.37 Comparison of P6n Pin Function Control Register (P6nPFS)**

Register	Bit	RX65N (n = 6, 7)	RX671 (n = 0 to 7)
P60PFS	—	—	P60 pin function control register
P61PFS	—	—	P61 pin function control register
P62PFS	—	—	P62 pin function control register
P63PFS	—	—	P63 pin function control register
P64PFS	—	—	P64 pin function control register
P65PFS	—	—	P65 pin function control register
P6nPFS	ISEL	Interrupt input function select bit  0: Not used as IRQn input pin 1: Used as IRQn input pin   P67: IRQ15 (177/176/145/144-pin)	Interrupt input function select bit  0: Not used as IRQn input pin 1: Used as IRQn input pin  P60: IRQ0 (145/144-pin) P61: IRQ1 (145/144-pin) P62: IRQ2 (145/144-pin) P63: IRQ3 (145/144-pin) P64: IRQ4 (145/144-pin) P65: IRQ13 (145/144-pin) P66: IRQ14 (145/144-pin) P67: IRQ15 (145/144-pin)

**Table 2.38 Comparison of P7n Pin Function Control Register (P7nPFS)**

Register	Bit	RX65N (n = 1 to 7)	RX671 (n = 0 to 7)
P70PFS	—	—	P70 pin function control register
P71PFS	PSEL[5:0]	Pin function select bits	—
P72PFS	PSEL[5:0]	Pin function select bits	—
P73PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000110b: PO16 010001b: ET0_WOL  100101b: LCD_EXTCLK-A*1	Pin function select bits  000000b: Hi-Z 000110b: PO16 010001b: USB1_VBUS 010010b: USB1_VBUSEN 010011b: USB1_OVRCURB
P74PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000110b: PO19 001011b: CTS11#/SS11# 010001b: ET0_ERXD1 010010b: RMII0_RXD1  100101b: LCD_DATA21-A*1	Pin function select bits  000000b: Hi-Z 000110b: PO19 001011b: CTS11#/SS11#  010011b: USB1_VBUSEN  101101b: CTS011#/SS011#



Register	Bit	RX65N (n = 1 to 7)	RX671 (n = 0 to 7)
P75PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000110b: PO20 001010b: SCK11 001011b: RTS11# 010001b: ET0_ERXD0 010010b: RMII0_RXD0 011001b: MMC_RES#-A 011010b: SDHI_D2-A 100011b: SDSI_D2 100101b: LCD_DATA20-A*1	Pin function select bits  000000b: Hi-Z 000110b: PO20 001010b: SCK11 001011b: RTS11#  010010b: USB1_OVRCURA  011010b: SDHI_D2-A  101100b: SCK011 101101b: RTS011# 101110b: DE011
P76PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000110b: PO22 001010b: RXD11/SMISO11/SSCL11 010001b: ET0_RX_CLK 010010b: REF50CK0 011001b: MMC_CMD-A 011010b: SDHI_CMD-A 011011b: QSSL-A 100011b: SDSI_CMD 100101b: LCD_DATA18-A*1	Pin function select bits  000000b: Hi-Z 000110b: PO22 001010b: RXD11/SMISO11/SSCL11  011010b: SDHI_CMD-A 011011b: QSSL-A  101100b: RXD011/SMISO011/ SSCL011
P77PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000110b: PO23 001010b: TXD11/SMOSI11/SSDA11 010001b: ET0_RX_ER 010010b: RMII0_RX_ER  011001b: MMC_CLK-A 011010b: SDHI_CLK-A 011011b: QSPCLK-A 100011b: SDSI_CLK 100101b: LCD_DATA17-A*1	Pin function select bits  000000b: Hi-Z 000110b: PO23 001010b: TXD11/SMOSI11/SSDA11  010011b: USB1_ID  011010b: SDHI_CLK-A 011011b: QSPCLK-A  101100b: TXD011/SMOSI011/ SSDA011
P7nPFSs	ISEL	—	Interrupt input function select bit

Note: 1. Not supported on products with a code flash memory capacity of 1 MB or less.

**Table 2.39 Comparison of P8n Pin Function Control Register (P8nPFS)**

Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 0 to 3, 6, 7)
P80PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3B 000110b: PO26 001010b: SCK10 001011b: RTS10# 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN  011000b: EDREQ0 011001b: MMC_D2-A 011010b: SDHI_WP 011011b: QIO2-A 100101b: LCD_DATA14-A	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3B 000110b: PO26 001010b: SCK10 001011b: RTS10#  010011b: USB1_EXICEN 011000b: EDREQ0  011010b: SDHI_WP 011011b: QIO2-A  101100b: SCK010 101101b: RTS010# 101110b: DE010
P81PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3D 000110b: PO27 001010b: RXD10/SMISO10/SSCL10 010001b: ET0_ETXD0 010010b: RMII0_TXD0  011000b: EDACK0 011001b: MMC_D3-A 011010b: SDHI_CD 011011b: QIO3-A 100101b: LCD_DATA13-A	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3D 000110b: PO27 001010b: RXD10/SMISO10/SSCL10  010011b: USB1_OVRCURB 011000b: EDACK0  011010b: SDHI_CD 011011b: QIO3-A  101100b: RXD010/SMISO010/ SSCL010
P82PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4A 000110b: PO28 001010b: TXD10/SMOSI10/SSDA10 010001b: ET0_ETXD1  010010b: RMII0_TXD1 011000b: EDREQ1 011001b: MMC_D4-A 100101b: LCD_DATA12-A	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4A 000110b: PO28 001010b: TXD10/SMOSI10/SSDA10  010011b: USB1_VBUSEN  011000b: EDREQ1  101100b: TXD010/SMOSI010/ SSDA010

Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 0 to 3, 6, 7)
P83PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4C 001010b: SCK10 001011b: CTS10#/SS10# 010001b: ET0_CRS 010010b: RMII0_CRS_DV 011000b: EDACK1 100101b: LCD_DATA8-A	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4C 001010b: SCK10 001011b: CTS10#/SS10#  011000b: EDACK1  101100b: SCK010 101101b: CTS010#/SS010#
P84PFS	—	P84 pin function control register	—
P85PFS	—	P85 pin function control register	—
P86PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000011b: TIOCA0 001000b: MTIOC4D 001010b: RXD10/SMISO10/SSCL10 011100b: PIXD1	Pin function select bits  000000b: Hi-Z 000011b: TIOCA0 001000b: MTIOC4D 001010b: RXD10/SMISO10/SSCL10  101100b: RXD010/SMISO010/ SSCL010
P87PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000011b: TIOCA2 001000b: MTIOC4C 001010b: TXD10/SMOSI10/SSDA10 011010b: SDHI_D2-C*1 011100b: PIXD2	Pin function select bits  000000b: Hi-Z 000011b: TIOCA2 001000b: MTIOC4C 001010b: TXD10/SMOSI10/SSDA10 011010b: SDHI_D2-C  101100b: TXD010/SMOSI010/ SSDA010
P8nPFS	ISEL	—	Interrupt input function select bit

Note: 1. Not supported on products with a code flash memory capacity of 1 MB or less.

**Table 2.40 Comparison of P9n Pin Function Control Register (P9nPFS)**

Register	Bit	RX65N (n = 0 to 3)	RX671 (n = 0 to 3)
P9nPFS	ISEL	—	Interrupt input function select bit

**Table 2.41 Comparison of PAn Pin Function Control Register (PAnPFS)**

Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 0 to 7)
PA0PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4A 000011b: TIOCA0 000110b: PO16 000111b: CACREF 001000b: MTIOC6D 001101b: SSLA1-B  010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 100101b: LCD_DATA8-B*1	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4A 000011b: TIOCA0 000110b: PO16 000111b: CACREF 001000b: MTIOC6D 001101b: SSLA1-B 001110b: SSL01-B
PA1PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKC 000011b: TIOCB0 000110b: PO17 001000b: MTIOC7B 001010b: SCK5  001101b: SSLA2-B  010001b: ET0_WOL 100101b: LCD_DATA7-B*1	Pin function select bits  000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKC 000011b: TIOCB0 000110b: PO17 001000b: MTIOC7B 001010b: SCK5 001100b: SCK12 001101b: SSLA2-B 001110b: SSL02-B  110001b: SDHI_CD
PA2PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000110b: PO18 001000b: MTIOC7A 001010b: RXD5/SMISO5/SSCL5  001101b: SSLA3-B  100101b: LCD_DATA6-B*1	Pin function select bits  000000b: Hi-Z 000110b: PO18 001000b: MTIOC7A 001010b: RXD5/SMISO5/SSCL5 001100b: RXD12/SMISO12/ SSCL12/RXD12 001101b: SSLA3-B 001110b: SSL03-B  110001b: SDHI_WP
PA3PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC0D 000010b: MTCLKD 000011b: TIOCD0 000100b: TCLKB 000110b: PO19 001010b: RXD5/SMISO5/SSCL5 010001b: ET0_MDIO 100101b: LCD_DATA5-B*1	Pin function select bits  000000b: Hi-Z 000001b: MTIOC0D 000010b: MTCLKD 000011b: TIOCD0 000100b: TCLKB 000110b: PO19 001010b: RXD5/SMISO5/SSCL5

Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 0 to 7)
PA4PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIC5U 000010b: MTCLKA 000011b: TIOCA1 000101b: TMRIO 000110b: PO20 001010b: TXD5/SMOSI5/SSDA5  001101b: SSLA0-B  010001b: ET0_MDC 100101b: LCD_DATA4-B*1	Pin function select bits  000000b: Hi-Z 000001b: MTIC5U 000010b: MTCLKA 000011b: TIOCA1 000101b: TMRIO 000110b: PO20 001010b: TXD5/SMOSI5/SSDA5 001100b: TXD12/SMOSI12/ SSDA12/TXD12/SIOX12 001101b: SSLA0-B 001110b: SSL00-B
PA5PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000011b: TIOCB1 000110b: PO21 001000b: MTIOC6B 001101b: RSPCKA-B 010001b: ET0_LINKSTA 100101b: LCD_DATA3-B*1	Pin function select bits  000000b: Hi-Z 000011b: TIOCB1 000110b: PO21 001000b: MTIOC6B 001101b: RSPCKA-B 001110b: RSPCK0-B
PA6PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIC5V 000010b: MTCLKB 000011b: TIOCA2 000101b: TMC13 000110b: PO22 000111b: POE10# 001011b: CTS5#/RTS5#/SS5#  001101b: MOSIA-B  010001b: ET0_EXOUT 100101b: LCD_DATA2-B*1	Pin function select bits  000000b: Hi-Z 000001b: MTIC5V 000010b: MTCLKB 000011b: TIOCA2 000101b: TMC13 000110b: PO22 000111b: POE10# 001011b: CTS5#/RTS5#/SS5# 001100b: CTS12#/RTS12#/SS12# 001101b: MOSIA-B 001110b: MOSI0-B
PA7PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000011b: TIOCB2 000110b: PO23 001101b: MISOA-B  010001b: ET0_WOL 100101b: LCD_DATA1-B	Pin function select bits  000000b: Hi-Z 000011b: TIOCB2 000110b: PO23 001101b: MISOA-B 001110b: MIS00-B

Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 0 to 7)
PAnPFS	ISEL	Interrupt input function select bit  0: Not used as IRQn input pin 1: Used as IRQn input pin  PA1: IRQ11 (177/176/145/144/100/64-pin)  PA3: IRQ6-DS (177/176/145/144/100-pin)  PA4: IRQ5-DS (177/176/145/144/100/64-pin)	Interrupt input function select bit  0: Not used as IRQn input pin 1: Used as IRQn input pin  PA0: IRQ0 (145/144/100-pin) PA1: IRQ11 (145/144/100/64/48-pin) PA2: IRQ10 (145/144/100/64/48-pin) PA3: IRQ6-DS (145/144/100-pin) PA4: IRQ5-DS (145/144/100/64/48-pin) PA5: IRQ5 (145/144/100-pin) PA6: IRQ14 (145/144/100/64/48-pin) PA7: IRQ7 (145/144/100/64-pin)

Note: 1. Not supported on products with a code flash memory capacity of 1 MB or less.

**Table 2.42 Comparison of P<sub>Bn</sub> Pin Function Control Register (P<sub>Bn</sub>PFS)**

Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 0 to 7)
PB0PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIC5W 000011b: TIOCA3 000110b: PO24 001010b: RXD4/SMISO4/SSCL4 001011b: RXD6/SMISO6/SSCL6 010001b: ET0_ERXD1 010010b: RMII0_RXD1 100101b: LCD_DATA0-B	Pin function select bits  000000b: Hi-Z 000001b: MTIC5W 000011b: TIOCA3 000110b: PO24 001010b: RXD4/SMISO4/SSCL4 001011b: RXD6/SMISO6/SSCL6
PB1PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC0C 000010b: MTIOC4C 000011b: TIOCB3 000101b: TMCI0 000110b: PO25 001010b: TXD4/SMOSI4/SSDA4 001011b: TXD6/SMOSI6/SSDA6 010001b: ET0_ERXD0 010010b: RMII0_RXD0 100101b: LCD_TCON3-B	Pin function select bits  000000b: Hi-Z 000001b: MTIOC0C 000010b: MTIOC4C 000011b: TIOCB3 000101b: TMCI0 000110b: PO25 001010b: TXD4/SMOSI4/SSDA4 001011b: TXD6/SMOSI6/SSDA6

Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 0 to 7)
PB2PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000011b: TIOCC3 000100b: TCLKC 000110b: PO26 001010b: CTS4#/RTS4#/SS4# 001011b: CTS6#/RTS6#/SS6# 010001b: ET0_RX_CLK 010010b: REF50CK0 100011b: SDSI_D2 100101b: LCD_TCON2-B*1	Pin function select bits  000000b: Hi-Z 000011b: TIOCC3 000100b: TCLKC 000110b: PO26 001010b: CTS4#/RTS4#/SS4# 001011b: CTS6#/RTS6#/SS6#
PB3PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC0A 000010b: MTIOC4A 000011b: TIOCD3 000100b: TCLKD 000101b: TMO0 000110b: PO27 000111b: POE11# 001010b: SCK4 001011b: SCK6 010001b: ET0_RX_ER 010010b: RMII0_RX_ER 100011b: SDSI_D3 100101b: LCD_TCON1-B*1	Pin function select bits  000000b: Hi-Z 000001b: MTIOC0A 000010b: MTIOC4A 000011b: TIOCD3 000100b: TCLKD 000101b: TMO0 000110b: PO27 000111b: POE11# 001010b: SCK4 001011b: SCK6
PB4PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000011b: TIOCA4 000110b: PO28 001011b: CTS9#/RTS9#/SS9# 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 100011b: SDSI_CMD 100100b: CTS11#/RTS11#/SS11# 100101b: LCD_TCON0-B*1	Pin function select bits  000000b: Hi-Z 000011b: TIOCA4 000110b: PO28 001011b: CTS9#/RTS9#/SS9#  100100b: CTS11#/RTS11#/SS11#  101100b: CTS011#**2/RTS011#**2/ SS011# 101110b: DE011

Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 0 to 7)
PB5PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC2A 000010b: MTIOC1B 000011b: TIOCB4 000101b: TMR11 000110b: PO29 000111b: POE4# 001010b: SCK9 010001b: ET0_ETXD0 010010b: RMII0_TXD0 100011b: SDSI_CLK 100100b: SCK11 100101b: LCD_CLK-B*1	Pin function select bits  000000b: Hi-Z 000001b: MTIOC2A 000010b: MTIOC1B 000011b: TIOCB4 000101b: TMR11 000110b: PO29 000111b: POE4# 001010b: SCK9  100100b: SCK11  101100b: SCK011
PB6PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3D 000011b: TIOCA5 000110b: PO30 001010b: RXD9/SMISO9/SSCL9 010001b: ET0_ETXD1 010010b: RMII0_TXD1 100011b: SDSI_D0 100100b: RXD11/SMISO11/SSCL11	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3D 000011b: TIOCA5 000110b: PO30 001010b: RXD9/SMISO9/SSCL9  100100b: RXD11/SMISO11/SSCL11 101100b: RXD011/SMISO011/SSCL011
PB7PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3B 000011b: TIOCB5 000110b: PO31 001010b: TXD9/SMOSI9/SSDA9 010001b: ET0_CRS 010010b: RMII0_CRS_DV 100011b: SDSI_D1 100100b: TXD11/SMOSI11/SSDA11	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3B 000011b: TIOCB5 000110b: PO31 001010b: TXD9/SMOSI9/SSDA9  100100b: TXD11/SMOSI11/SSDA11 101100b: TXD011/SMOSI011/SSDA011



Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 0 to 7)
PBnPFS	ISEL	Interrupt input function select bit  0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ12 (177/176/145/144/100-pin) PB1: IRQ4-DS (177/176/145/144/100-pin)	Interrupt input function select bit  0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ12 (145/144/100-pin) PB1: IRQ4-DS (145/144/100-pin) PB2: IRQ2 (145/144/100-pin) PB3: IRQ3 (145/144/100-pin) PB4: IRQ4 (145/144/100-pin) PB5: IRQ13 (145/144/100/64/48-pin) PB6: IRQ6 (145/144/100/64/48-pin) PB7: IRQ15 (145/144/100/64/48-pin)

Notes: 1. Not supported on products with a code flash memory capacity of 1 MB or less.  
 2. Not usable as CTS011# when SCR1.CRSEP = 1. Can be used as RTS011#.

**Table 2.43 Comparison of PCn Pin Function Control Register (PCnPFS)**

Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 0 to 7)
PC0PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3C 000011b: TCLKC 000110b: PO17 001011b: CTS5#/RTS5#/SS5# 001101b: SSLA1-A  010001b: ET0_ERXD3	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3C 000011b: TCLKC 000110b: PO17 001011b: CTS5#/RTS5#/SS5# 001101b: SSLA1-A 001110b: SSL01-A  101011b: TS16 101100b: RXD011/SMISO011/ SSCL011
PC1PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3A 000011b: TCLKD 000110b: PO18 001010b: SCK5 001101b: SSLA2-A  010001b: ET0_ERXD2 100101b: LCD_DATA22-A	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3A 000011b: TCLKD 000110b: PO18 001010b: SCK5 001101b: SSLA2-A 001110b: SSL02-A  101011b: TS15 101100b: TXD011/SMOSI011/ SSSDA011/TXDA011

Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 0 to 7)
PC2PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4B 000011b: TCLKA 000110b: PO21 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3-A  010001b: ET0_RX_DV 011001b: MMC_CD-A 011010b: SDHI_D3-A 100011b: SDSI_D3 100101b: LCD_DATA19-A*1	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4B 000011b: TCLKA 000110b: PO21 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3-A 001110b: SSL03-A  011010b: SDHI_D3-A  101100b: TXDB011
PC3PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4D 000011b: TCLKB 000110b: PO24 001010b: TXD5/SMOSI5/SSDA5 010001b: ET0_TX_ER 011001b: MMC_D0-A 011010b: SDHI_D0-A 011011b: QIO0-A/QMO-A 100011b: SDSI_D0 100101b: LCD_DATA16-A*1	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4D 000011b: TCLKB 000110b: PO24 001010b: TXD5/SMOSI5/SSDA5  011010b: SDHI_D0-A 011011b: QIO0-A
PC4PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKC 000101b: TMCI1 000110b: PO25 000111b: POE0# 001010b: SCK5 001011b: CTS8#/RTS8#/SS8# 001101b: SSLA0-A  010001b: ET0_TX_CLK  011001b: MMC_D1-A 011010b: SDHI_D1-A 011011b: QIO1-A/QMI-A 100011b: SDSI_D1 100100b: CTS10#/RTS10#/SS10# 100101b: LCD_DATA15-A*1	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKC 000101b: TMCI1 000110b: PO25 000111b: POE0# 001010b: SCK5 001011b: CTS8#/RTS8#/SS8# 001101b: SSLA0-A 001110b: SSL00-A  010111b: AUDIO_CLK  011010b: SDHI_D1-A 011011b: QIO1-A  100100b: CTS10#/RTS10#/SS10#  101011b: TSCAP 101100b: CTS010#**2/RTS010#**2/ SS010# 101110b: DE010

Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 0 to 7)
PC5PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKD 000101b: TMRI2 000110b: PO29 001010b: SCK8 001101b: RSPCKA-A  010001b: ET0_ETXD2  011001b: MMC_D5-A 100100b: SCK10 100101b: LCD_DATA11-A*1	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKD 000101b: TMRI2 000110b: PO29 001010b: SCK8 001101b: RSPCKA-A 001110b: RSPCK0-A  010111b: SSIBCK0  100100b: SCK10  101011b: TS14 101100b: SCK010
PC6PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKA 000101b: TMC12 000110b: PO30 001010b: RXD8/SMISO8/SSCL8 001101b: MOSIA-A  010001b: ET0_ETXD3  011001b: MMC_D6-A 011101b: TIC0 100100b: RXD10/SMISO10/SSCL10 100101b: LCD_DATA10-A*1	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKA 000101b: TMC12 000110b: PO30 001010b: RXD8/SMISO8/SSCL8 001101b: MOSIA-A 001110b: MOSI0-A  010111b: SSILRCK0  011101b: TIC0 100100b: RXD10/SMISO10/SSCL10  101011b: TS13 101100b: RXD010/SMISO010/ SSCL010

Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 0 to 7)
PC7PFS	PSEL[5:0]	<p>Pin function select bits</p> <p>000000b: Hi-Z                      000001b: MTIOC3A                      000010b: MTCLKB                      000101b: TMO2                      000110b: PO31                      000111b: CACREF                      001010b: TXD8/SMOSI8/SSDA8                      001101b: MISOA-A</p> <p>010001b: ET0_COL</p> <p>011001b: MMC_D7-A                      011101b: TOC0                      100100b: TXD10/SMOSI10/SSDA10                      100101b: LCD_DATA9-A*1</p>	<p>Pin function select bits</p> <p>000000b: Hi-Z                      000001b: MTIOC3A                      000010b: MTCLKB                      000101b: TMO2                      000110b: PO31                      000111b: CACREF                      001010b: TXD8/SMOSI8/SSDA8                      001101b: MISOA-A                      001110b: MISOO-A</p> <p>010111b: SSITXD0</p> <p>011101b: TOC0                      100100b: TXD10/SMOSI10/SSDA10</p> <p>101100b: TXD010/SMOSI010/                      SSDA010</p>
PCnPFS	ISEL	<p>Interrupt input function select bit</p> <p>0: Not used as IRQn input pin                      1: Used as IRQn input pin</p> <p>PC0: IRQ14                      (177/176/145/144/100/64-pin)</p> <p>PC1: IRQ12                      (177/176/145/144/100/64-pin)</p> <p>PC6: IRQ13                      (177/176/145/144/100/64-pin)</p> <p>PC7: IRQ14                      (177/176/145/144/100/64-pin)</p>	<p>Interrupt input function select bit</p> <p>0: Not used as IRQn input pin                      1: Used as IRQn input pin</p> <p>PC0: IRQ14                      (145/144/100/64-pin)</p> <p>PC1: IRQ12                      (145/144/100/64-pin)</p> <p>PC2: IRQ10 (145/144/100-pin)                      PC3: IRQ11 (145/144/100-pin)                      PC4: IRQ12 (145/144/100/64/48-pin)                      PC5: IRQ5 (145/144/100/64/48-pin)</p> <p>PC6: IRQ13                      (145/144/100/64/48-pin)</p> <p>PC7: IRQ14                      (145/144/100/64/48-pin)</p>

Notes: 1. Not supported on products with a code flash memory capacity of 1 MB or less.  
 2. Not usable as CTS011# when SCR1.CRSEP = 1. Can be used as RTS011#.

**Table 2.44 Comparison of PDn Pin Function Control Register (PDnPFS)**

Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 0 to 7)
PD0PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 001000b: POE4# <b>100101b: LCD_EXTCLK-B*1</b>	Pin function select bits  000000b: Hi-Z 001000b: POE4#
PD1PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4B 001000b: POE0# 001101b: MOSIC-A 010000b: CTX0 <b>100101b: LCD_DATA23-B*1</b>	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4B 001000b: POE0# 001101b: MOSIC-A 010000b: CTX0
PD2PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4D 001101b: MISOC-A 010000b: CRX0 <b>011001b: MMC_D2-B</b> 011010b: SDHI_D2-B 011011b: QIO2-B 011101b: TIC2 <b>100101b: LCD_DATA22-B*1</b>	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4D 001101b: MISOC-A 010000b: CRX0  011010b: SDHI_D2-B 011011b: QIO2-B 011101b: TIC2
PD3PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000111b: POE8# 001000b: MTIOC8D 001101b: RSPCKC-A <b>011001b: MMC_D3-B</b> 011010b: SDHI_D3-B 011011b: QIO3-B 011101b: TOC2 <b>100101b: LCD_DATA21-B*1</b>	Pin function select bits  000000b: Hi-Z 000111b: POE8# 001000b: MTIOC8D 001101b: RSPCKC-A  011010b: SDHI_D3-B 011011b: QIO3-B 011101b: TOC2
PD5PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIC5W 000111b: POE10# 001000b: MTIOC8C 001101b: SSLC1-A <b>011001b: MMC_CLK-B</b> 011010b: SDHI_CLK-B 011011b: QSPCLK-B <b>100101b: LCD_DATA19-B*1</b>	Pin function select bits  000000b: Hi-Z 000001b: MTIC5W 000111b: POE10# 001000b: MTIOC8C 001101b: SSLC1-A  011010b: SDHI_CLK-B 011011b: QSPCLK-B

Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 0 to 7)
PD6PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIC5V 000111b: POE4# 001000b: MTIOC8A 001101b: SSLC2-A 011001b: MMC_D0-B 011010b: SDHI_D0-B 011011b: QIO0-B/QMO-B 100101b: LCD_DATA18-B*1	Pin function select bits  000000b: Hi-Z 000001b: MTIC5V 000111b: POE4# 001000b: MTIOC8A 001101b: SSLC2-A  011010b: SDHI_D0-B 011011b: QIO0-B
PD7PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIC5U 000111b: POE0# 001101b: SSLC3-A 011001b: MMC_D1-B 011010b: SDHI_D1-B 011011b: QIO1-B/QMI-B 100101b: LCD_DATA17-B*1	Pin function select bits  000000b: Hi-Z 000001b: MTIC5U 000111b: POE0# 001101b: SSLC3-A  011010b: SDHI_D1-B 011011b: QIO1-B
PDnPFS	ASEL	Analog input function select bit  0: Used as other than as analog pin 1: Used as analog pin PD0: AN108 (177/176/145/144/100-pin) PD1: AN109 (177/176/145/144/100-pin) PD2: AN110 (177/176/145/144/100/64-pin) PD3: AN111 (177/176/145/144/100/64-pin) PD4: AN112 (177/176/145/144/100/64-pin) PD5: AN113 (177/176/145/144/100/64-pin) PD6: AN106 (177/176/145/144/100/64-pin) PD7: AN107 (177/176/145/144/100/64-pin)	Analog input function select bit  0: Used as other than as analog pin 1: Used as analog pin PD0: AN107 (145/144/100-pin) PD1: AN106 (145/144/100-pin) PD2: AN105 (145/144/100/64/48-pin) PD3: AN104 (145/144/100/64/48-pin) PD4: AN103 (145/144/100/64/48-pin) PD5: AN102 (145/144/100/64/48-pin) PD6: AN101 (145/144/100/64-pin) PD7: AN100 (145/144/100/64-pin)

Note: 1. Not supported on products with a code flash memory capacity of 1 MB or less.

**Table 2.45 Comparison of PEn Pin Function Control Register (PEnPFS)**

Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 0 to 7)
PE0PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 001000b: MTIOC3D 001100b: SCK12 001101b: SSLB1-B 011001b: MMC_D4-B 100101b: LCD_DATA16-B*1	Pin function select bits  000000b: Hi-Z 001000b: MTIOC3D 001100b: SCK12 001101b: SSLB1-B
PE1PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4C 000110b: PO18 001000b: MTIOC3B 001100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12 001101b: SSLB2-B 011001b: MMC_D5-B 100101b: LCD_DATA15-B*1	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4C 000110b: PO18 001000b: MTIOC3B 001100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12 001101b: SSLB2-B
PE2PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4A 000110b: PO23 001100b: RXD12/SMISO12/SSCL12/ RXDX12 001101b: SSLB3-B 011001b: MMC_D6-B 011101b: TIC3 100101b: LCD_DATA14-B*1	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4A 000110b: PO23 001100b: RXD12/SMISO12/SSCL12/ RXDX12 001101b: SSLB3-B 011101b: TIC3
PE3PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4B 000110b: PO26 000111b: POE8# 001100b: CTS12#/RTS12#/SS12# 010001b: ET0_ERXD3 011001b: MMC_D7-B 011101b: TOC3 100101b: LCD_DATA13-B*1	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4B 000110b: PO26 000111b: POE8# 001100b: CTS12#/RTS12#/SS12# 011101b: TOC3
PE4PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4D 000010b: MTIOC1A 000110b: PO28 001101b: SSLB0-B 010001b: ET0_ERXD2 100101b: LCD_DATA12-B*1	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4D 000010b: MTIOC1A 000110b: PO28 001101b: SSLB0-B

Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 0 to 7)
PE5PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4C 000010b: MTIOC2B 001101b: RSPCKB-B 010001b: ET0_RX_CLK 010010b: REF50CK0 100101b: LCD_DATA11-B*1	Pin function select bits  000000b: Hi-Z 000001b: MTIOC4C 000010b: MTIOC2B 001101b: RSPCKB-B
PE6PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 001000b: MTIOC6C 001101b: MOSIB-B 011001b: MMC_CD-B 011010b: SDHI_CD  011101b: TIC1 100101b: LCD_DATA10-B*1	Pin function select bits  000000b: Hi-Z 001000b: MTIOC6C 001101b: MOSIB-B  011010b: SDHI_CD 011011b: QIO0-B 011101b: TIC1  110001b: SDHI_D0-B
PE7PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 001000b: MTIOC6A 001101b: MISOB-B 011001b: MMC_RES#-B 011010b: SDHI_WP  011101b: TOC1 100101b: LCD_DATA9-B*1	Pin function select bits  000000b: Hi-Z 001000b: MTIOC6A 001101b: MISOB-B  011010b: SDHI_WP 011011b: QIO1-B 011101b: TOC1  110001b: SDHI_D1-B
PEnPFS	ISEL	Interrupt input function select bit  0: Not used as IRQn input pin 1: Used as IRQn input pin  PE2: IRQ7-DS (177/176/145/144/100/64-pin)  PE5: IRQ5 (177/176/145/144/100-pin) PE6: IRQ6 (177/176/145/144/100/64-pin) PE7: IRQ7 (177/176/145/144/100/64-pin)	Interrupt input function select bit  0: Not used as IRQn input pin 1: Used as IRQn input pin PE0: IRQ8 (145/144/100/64-pin) PE1: IRQ9 (145/144/100/64-pin) PE2: IRQ7-DS (145/144/100/64-pin) PE3: IRQ11 (145/144/100-pin) PE4: IRQ12 (145/144/100-pin) PE5: IRQ5 (145/144/100-pin) PE6: IRQ6 (145/144/100/64/48-pin) PE7: IRQ7 (145/144/100/64/48-pin)



Register	Bit	RX65N (n = 0 to 7)	RX671 (n = 0 to 7)
PEnPFS	ASEL	Analog input function select bit  0: Used as other than as analog pin 1: Used as analog pin PE0: ANEX0 (177/176/145/144/100/64-pin) PE1: ANEX1 (177/176/145/144/100/64-pin) PE2: AN100 (177/176/145/144/100-pin) PE3: AN101 (177/176/145/144/100-pin) PE4: AN102 (177/176/145/144/100-pin) PE5: AN103 (177/176/145/144/100-pin) PE6: AN104 (177/176/145/144/100-pin) PE7: AN105 (177/176/145/144/100-pin)	Analog input function select bit  0: Used as other than as analog pin 1: Used as analog pin PE0: ANEX0 (145/144/100/64-pin) PE1: ANEX1 (145/144/100/64-pin)

Note: 1. Not supported on products with a code flash memory capacity of 1 MB or less.

**Table 2.46 Comparison of PFn Pin Function Control Register (PFnPFS)**

Register	Bit	RX65N (n = 0 to 2, 5)	RX671 (n = 5)
PF0PFS	—	PF0 pin function control register	—
PF1PFS	—	PF1 pin function control register	—
PF2PFS	—	PF2 pin function control register	—
PF5PFS	PSEL[5:0]	—	Pin function select bits

**Table 2.47 Comparison of PHn Pin Function Control Register (PHnPFS)**

Register	Bit	RX65N	RX671
PHnPFS	—	—	PHn pin function control register (n = 1, 2)

**Table 2.48 Comparison of PJn Pin Function Control Register (PJnPFS)**

Register	Bit	RX65N (n = 0 to 3, 5)	RX671 (n = 3, 5)
PJ0PFS	—	PJ0 pin function control register	—
PJ1PFS	—	PJ1 pin function control register	—
PJ2PFS	—	PJ2 pin function control register	—
PJ3PFS	PSEL[5:0]	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3C 001010b: CTS6#/RTS6#/SS6# 001011b: CTS0#/RTS0#/SS0# 010001b: ET0_EXOUT 011000b: EDACK1	Pin function select bits  000000b: Hi-Z 000001b: MTIOC3C 001010b: CTS6#/RTS6#/SS6# 001011b: CTS0#/RTS0#/SS0#  011000b: EDACK1
PJnPFS	ISEL	—	Interrupt input function select bit

**Table 2.49 Comparison of Multi-Function Pin Controller Registers**

Register	Bit	RX65N (MPC)	RX671 (MPC)
PFBCR0	ADRHMS ADRHMS2	A16 to A23 output enable bit A16 to A23 output enable 2 bit  ADRHMS / ADRHMS2 0 / 0: Set PC0 to PC7. 0 / 1: Set PC0, PC1, P71, P72, P74, and PC5 to PC7. 1 / 0: Products with 1.5 MB or more of code flash memory: <b>Set P90 to P97.</b> Products with 1 MB or less of code flash memory: Set P90 to P93 (A20 to A23 not assigned). 1 / 1: Setting prohibited.	A16 to A23 output enable bit A16 to A23 output enable 2 bit  ADRHMS / ADRHMS2 0 / 0: Set PC0 to PC7. 0 / 1: Set PC0, PC1, P71, P72, P74, and PC5 to PC7. 1 / 0:  Set P90 to P93 (A20 to A23 not assigned). 1 / 1: Setting prohibited.  <b>Pins P71 and P72 are not present on the 145-pin TFLGA (PTLG0145JB-A) product, so the ADRHMS and ADRHMS2 bits should be set to 00b or 10b when using external address buses A16 to A23.</b>
	DH32E	D16 to D31 output enable bit* <sup>1</sup>	—
	WR32BC32E	WR3#/BC3# and WR2#/BC2# output enable bit* <sup>1</sup>	—
PFBCR1	ALES	ALE select bit* <sup>1</sup>	—
PFENET	—	Ethernet control register	—

Note: 1. This bit is reserved for products with 1 MB of code flash memory or less. This bit is read as 0. The write value should be 0.

## 2.15 Port Output Enable 3

Table 2.50 is a comparison of port output enable 3 registers.

**Table 2.50 Comparative Overview of Port Output Enable 3**

Register	Bit	RX65N (POE3a)	RX671 (POE3a)
M6SELR	—	MTU6 pin select register	—

## 2.16 8-Bit Timer

Table 2.51 is a comparative overview of 8-bit timer.

**Table 2.51 Comparative Overview of 8-Bit Timer**

Item	RX65N (TMR)	RX671 (TMR <sup>b</sup> )
Count clocks	<ul style="list-style-type: none"> <li>Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192</li> <li>External clock: External count clock</li> </ul>	<ul style="list-style-type: none"> <li>Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192</li> <li>External clock: External count clock</li> </ul>
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 2 units
Compare match	<ul style="list-style-type: none"> <li>8-bit mode (compare match A, compare match B)</li> <li>16-bit mode (compare match A, compare match B)</li> </ul>	<ul style="list-style-type: none"> <li>8-bit mode (compare match A, compare match B)</li> <li>16-bit mode (compare match A, compare match B)</li> </ul>
Counter clear	Selectable among compare match A or B, or an external counter reset signal.	Selectable among compare match A or B, or an external counter reset signal.
Timer output	Output pulses with a user-defined duty cycle or PWM output	Output pulses with a user-defined duty cycle or PWM output
Cascading of two channels	<ul style="list-style-type: none"> <li>16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits)</li> <li>Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).</li> </ul>	<ul style="list-style-type: none"> <li>16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits)</li> <li>Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).</li> </ul>
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	Compare match A, compare match B, and overflow (TMR0 to TMR3)	Compare match A, compare match B, and overflow (TMR0 to TMR3)
Event link function (input)	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0 to TMR3) (2) Event counter (TMR0 to TMR3) (3) Counter restart (TMR0 to TMR3)	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0 to TMR3) (2) Event counter (TMR0 to TMR3) (3) Counter restart (TMR0 to TMR3)
DTC activation	The DTC can be activated by compare match A interrupts or compare match B interrupts.	The DTC can be activated by compare match A interrupts or compare match B interrupts.
Generation of trigger to start A/D converter	Compare match A of TMR0 or TMR2	Compare match A of TMR0 or TMR2
Generation of baud rate clock for SCI	Generation of baud rate clock for SCI	Generation of SCI basic clock
Generation of REMC operation clock	—	Generation of REMC (remote control signal receiver) operation clock
Low power consumption function	Each unit can be placed in a module stop state.	Each unit can be placed in a module stop state.

## 2.17 USB 2.0 Host/Function Module

Table 2.52 is a comparative overview of the USB 2.0 Host/Function module.

**Table 2.52 Comparative Overview of USB 2.0 Host/Function Module**

Item	RX65N (USBb)	RX671 (USBb)
Number of channels	1 channel	2 channels
Features	<ul style="list-style-type: none"> <li>Integrated USB Device Controller (UDC) and transceiver for USB 2.0                             <ul style="list-style-type: none"> <li>Support for Host controller, Function controller, and on-the-go (OTG) functionality (1 channels)</li> </ul> </li> <li>Software can switch between the Host controller and Function controller modes.</li> <li>Self-power mode or bus-power mode can be selected.</li> </ul>	<ul style="list-style-type: none"> <li>Integrated USB Device Controller (UDC) and transceiver for USB 2.0                             <ul style="list-style-type: none"> <li>Support for Host controller, Function controller, and on-the-go (OTG) functionality (2 channels)</li> </ul> </li> <li>Software can switch between the Host controller and Function controller modes.</li> <li>Self-power mode or bus-power mode can be selected.</li> </ul>
	When Host controller operation is selected: <ul style="list-style-type: none"> <li>Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) are supported.</li> <li>Automatic scheduling of SOF and packet transmissions</li> <li>Transfer interval setting function for isochronous and interrupt transfers</li> <li>Communication with multiple peripheral devices connected via a single hub</li> </ul>	When Host controller operation is selected: <ul style="list-style-type: none"> <li>Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) are supported.</li> <li>Automatic scheduling of SOF and packet transmissions</li> <li>Transfer interval setting function for isochronous and interrupt transfers</li> <li>Communication with multiple peripheral devices connected via a single hub</li> </ul>
	When Function controller operation is selected: <ul style="list-style-type: none"> <li>Support for full-speed transfer (12 Mbps)*1</li> <li>Control transfer stage control function</li> <li>Device state control function</li> <li>Auto response function for SET_ADDRESS requests</li> <li>SOF interpolation function</li> </ul>	When Function controller operation is selected: <ul style="list-style-type: none"> <li>Support for full-speed transfer (12 Mbps)*1</li> <li>Control transfer stage control function</li> <li>Device state control function</li> <li>Auto response function for SET_ADDRESS requests</li> <li>SOF interpolation function</li> </ul>
Communication data transfer types	<ul style="list-style-type: none"> <li>Control transfer</li> <li>Bulk transfer</li> <li>Interrupt transfer</li> <li>Isochronous transfer</li> </ul>	<ul style="list-style-type: none"> <li>Control transfer</li> <li>Bulk transfer</li> <li>Interrupt transfer</li> <li>Isochronous transfer</li> </ul>
Pipe configuration	<ul style="list-style-type: none"> <li>Buffer memory for USB communication is provided.</li> <li>Up to ten pipes can be selected (including the default control pipe).</li> <li>Endpoint numbers can be assigned flexibly to PIPE1 to PIPE9.</li> </ul>	<ul style="list-style-type: none"> <li>Buffer memory for USB communication is provided.</li> <li>Up to ten pipes can be selected (including the default control pipe).</li> <li>Endpoint numbers can be assigned flexibly to PIPE1 to PIPE9.</li> </ul>

Item	RX65N (USBb)	RX671 (USBb)
Pipe configuration	Transfer conditions that can be set for each pipe: <ul style="list-style-type: none"> <li>• PIPE0: Control transfer, 64-byte single buffer</li> <li>• PIPE1 and PIPE2:                             <ul style="list-style-type: none"> <li>— 64-byte double buffer can be specified for bulk transfer.</li> <li>— 256-byte double buffer can be specified for isochronous transfer.</li> </ul> </li> <li>• PIPE3 to PIPE5: Bulk transfer, 64-byte double buffer</li> <li>• PIPE6 to PIPE9: Interrupt transfer, 64-byte single buffer</li> </ul>	Transfer conditions that can be set for each pipe: <ul style="list-style-type: none"> <li>• PIPE0: Control transfer, 64-byte single buffer</li> <li>• PIPE1 and PIPE2:                             <ul style="list-style-type: none"> <li>— 64-byte double buffer can be specified for bulk transfer.</li> <li>— 256-byte double buffer can be specified for isochronous transfer.</li> </ul> </li> <li>• PIPE3 to PIPE5: Bulk transfer, 64-byte double buffer</li> <li>• PIPE6 to PIPE9: Interrupt transfer, 64-byte single buffer</li> </ul>
Other functions	<ul style="list-style-type: none"> <li>• Reception end function using transaction count</li> <li>• Function that changes the BRDY interrupt event notification timing (BFRE)</li> <li>• Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO port (n = 0 or 1) has been read (DCLRM)</li> <li>• NAK setting function for response PID generated by end of transfer (SHTNAK)</li> <li>• On-chip D+/D- pull-up and pull-down resistors</li> </ul>	<ul style="list-style-type: none"> <li>• Reception end function using transaction count</li> <li>• Function that changes the BRDY interrupt event notification timing (BFRE)</li> <li>• Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO port (n = 0 or 1) has been read (DCLRM)</li> <li>• NAK setting function for response PID generated by end of transfer (SHTNAK)</li> <li>• On-chip D+/D- pull-up and pull-down resistors</li> </ul>
Low power consumption function	Ability to transition to module stop state.	Ability to transition to module stop state.

Note: 1. Low-speed transfer (1.5 Mbps) is not supported when Function controller operation is selected.

## 2.18 Serial Communications Interface

Table 2.53 is a comparative overview of the serial communications interfaces, Table 2.54 is a comparative listing of serial communications interface channels, Table 2.55 is a comparison of serial communications interface registers, and Table 2.56 is a comparison of TXDn pin control settings.

**Table 2.53 Comparative Overview of Serial Communications Interfaces**

Item	RX65N (SCIg, SCli, SCih)	RX671 (SCIk, SCIm, SCih)	
Number of channels	<ul style="list-style-type: none"> <li>• SCIg: 10 channels</li> <li>• SCli: 2 channels</li> <li>• SCih: 1 channel</li> </ul>	<ul style="list-style-type: none"> <li>• SCIk: 10 channels</li> <li>• SCIm: 2 channels</li> <li>• SCih: 1 channel</li> </ul>	
Serial communications modes	<ul style="list-style-type: none"> <li>• Asynchronous operation</li> <li>• Clock synchronous operation</li> <li>• Smart card interface</li> <li>• Simple I<sup>2</sup>C bus</li> <li>• Simple SPI bus</li> </ul>	<ul style="list-style-type: none"> <li>• Asynchronous operation</li> <li>• Clock synchronous operation</li> <li>• Smart card interface</li> <li>• Simple I<sup>2</sup>C bus</li> <li>• Simple SPI bus</li> </ul>	
Transfer speed	Bit rate specifiable using on-chip baud rate generator.	Bit rate specifiable using on-chip baud rate generator.	
Full-duplex communication	<ul style="list-style-type: none"> <li>• Transmitter: Support for continuous transmission using double-buffering</li> <li>• Receiver: Support for continuous reception using double-buffering</li> </ul>	<ul style="list-style-type: none"> <li>• Transmitter: Support for continuous transmission using double-buffering</li> <li>• Receiver: Support for continuous reception using double-buffering</li> </ul>	
Data transfer	Selectable between LSB-first and MSB-first	Selectable between LSB-first and MSB-first	
I/O signal level inversion	—	Ability to invert levels of input and output signals independently (SCIO to SCI11)	
Interrupt sources	<ul style="list-style-type: none"> <li>• Transmit end, transmit data empty, receive data full, receive error (SCIO to SCI12)</li> <li>• Data match (SCI10 and SCI11)</li> <li>• Receive data ready (SCI10 and SCI11)</li> <li>• Completion of generation of a start condition, restart condition, or stop condition (simple I<sup>2</sup>C mode) (SCIO to SCI12)</li> </ul>	<ul style="list-style-type: none"> <li>• Transmit end, transmit data empty, receive data full, receive error (SCIO to SCI12)</li> <li>• Data match (SCIO to SCI11)</li> <li>• Receive data ready (SCI10 and SCI11)</li> <li>• Completion of generation of a start condition, restart condition, or stop condition (simple I<sup>2</sup>C mode) (SCIO to SCI12)</li> </ul>	
Low power consumption function	Ability to transition each channel to module stop state	Ability to transition each channel to module stop state	
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even, odd, or none	Even, odd, or none
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	Ability to use CTSn# and RTSn# pins for transmission and reception control	Ability to use CTSn# and RTSn# pins for transmission and reception control

Item		RX65N (SCIg, SCli, SCih)	RX671 (SCIk, SCIm, SCih)
Asynchronous mode	Transmit/receive FIFO	Ability to use 16-stage FIFOs for transmission and reception (SCI10 and SCI11)	Ability to use 16-stage FIFOs for transmission and reception (SCI10 and SCI11)
	Data match detection	Ability to compare receive data and comparison data, and generates an interrupt when they match (SCI10 and SCI11)	Ability to compare receive data and comparison data, and generates an interrupt when they match (SCI0 to SCI11)
	Start-bit detection	Selectable between low level and falling edge	Selectable between low level and falling edge
	Receive data sampling timing adjustment	—	Ability to change the sampling point for receive data forward or backward relative to a reference point at the center of the data (SCI0 to SCI11)
	Transmit signal change timing adjustment	—	Ability to delay the falling or rising edge of the transmit data (SCI0 to SCI11)
	Break detection	<ul style="list-style-type: none"> <li>Ability to detect a break when a framing error occurs by reading the level of the RXDn pin directly (SCI0 to SCI12)</li> <li>Ability to detect a break by reading the SPTR.RXDMON flag (SCI10 and SCI11)</li> </ul>	<ul style="list-style-type: none"> <li>Ability to detect a break when a framing error occurs by reading the level of the RXDn pin directly (SCI0 to SCI12)</li> <li>Ability to detect a break by reading the SPTR.RXDMON flag (SCI0 to SCI11)</li> </ul>
	Clock source	<ul style="list-style-type: none"> <li>Selectable between internal or external clock (SCI0 to SCI12)</li> <li>Ability to input transfer rate clock from TMR (SCI5, SCI6, and SCI12)</li> </ul>	<ul style="list-style-type: none"> <li>Selectable between internal or external clock (SCI0 to SCI12)</li> <li>Ability to input transfer rate clock from TMR (SCI5, SCI6, and SCI12)</li> </ul>
	Double-speed mode	Ability to select baud rate generator double-speed mode	Ability to select baud rate generator double-speed mode
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation function	The input signal paths from the RXDn pins incorporate digital noise filters.	The input signal paths from the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	Ability to use CTSn# and RTSn# pins for transmission and reception control	Ability to use CTSn# and RTSn# pins for transmission and reception control
	Transmit/receive FIFO	Ability to use 16-stage FIFOs for transmission and reception (SCI10 and SCI11)	Ability to use 16-stage FIFOs for transmission and reception (SCI10 and SCI11)
Smart card interface mode	Error processing	<ul style="list-style-type: none"> <li>Automatic transmission of an error signal at detection of a parity error during reception</li> <li>Automatic re-transmission of data at reception of an error signal during transmission</li> </ul>	<ul style="list-style-type: none"> <li>Automatic transmission of an error signal at detection of a parity error during reception</li> <li>Automatic re-transmission of data at reception of an error signal during transmission</li> </ul>
	Data type	Support for direct convention and inverse convention	Support for direct convention and inverse convention



Item		RX65N (SCIg, SCII, SCIH)	RX671 (SCIk, SCIm, SCIH)
Simple I <sup>2</sup> C mode	Communication format	I <sup>2</sup> C bus format	I <sup>2</sup> C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	Support for fast mode	Support for fast mode
	Noise cancellation	<ul style="list-style-type: none"> <li>The SSCLn and SSDAn input signal paths incorporate digital noise filters.</li> <li>The noise cancellation interval is adjustable.</li> </ul>	<ul style="list-style-type: none"> <li>The SSCLn and SSDAn input signal paths incorporate digital noise filters.</li> <li>The noise cancellation interval is adjustable.</li> </ul>
Simple SPI mode	Data length	8 bits	8 bits
	Error detection	Overrun error	Overrun error
	SS input pin function	Ability to place output pins in high-impedance state by applying a high-level signal to the SSn# pin.	Ability to place output pins in high-impedance state by applying a high-level signal to the SSn# pin.
	Clock settings	Ability to select among four clock phase and clock polarity settings	Ability to select among four clock phase and clock polarity settings
Extended serial mode (supported by SCI12 only)	Start Frame transmission	<ul style="list-style-type: none"> <li>Ability to output Break Field low width/output completion interrupt function</li> <li>Bus collision detection function/detection interrupt function</li> </ul>	<ul style="list-style-type: none"> <li>Ability to output Break Field low width/output completion interrupt function</li> <li>Bus collision detection function/detection interrupt function</li> </ul>
	Start Frame reception	<ul style="list-style-type: none"> <li>Ability to detect Break Field low width/detection completion interrupt function</li> <li>Control Field 0 and Control Field 1 data comparison/match interrupt function</li> <li>Ability to select between two data types for comparison (primary and secondary) in Control Field 1</li> <li>Ability to set priority interrupt bit in Control Field 1</li> <li>Support for Start Frames that do not include a Break Field</li> <li>Support for Start Frames that do not include Control Field 0</li> <li>Bit rate measurement function</li> </ul>	<ul style="list-style-type: none"> <li>Ability to detect Break Field low width/detection completion interrupt function</li> <li>Control Field 0 and Control Field 1 data comparison/match interrupt function</li> <li>Ability to select between two data types for comparison (primary and secondary) in Control Field 1</li> <li>Ability to set priority interrupt bit in Control Field 1</li> <li>Support for Start Frames that do not include a Break Field</li> <li>Support for Start Frames that do not include Control Field 0</li> <li>Bit rate measurement function</li> </ul>
Extended serial mode (supported by SCI12 only)	I/O control function	<ul style="list-style-type: none"> <li>Ability to select polarity of TXDX12 and RXDX12 signals</li> <li>Ability to specify digital filter function for RXDX12 signal</li> <li>Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin</li> <li>Ability to select sampling timing for data received on RXDX12</li> </ul>	<ul style="list-style-type: none"> <li>Ability to select polarity of TXDX12 and RXDX12 signals</li> <li>Ability to specify digital filter function for RXDX12 signal</li> <li>Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin</li> <li>Ability to select sampling timing for data received on RXDX12</li> </ul>
	Timer function	Usable as reload timer	Usable as reload timer

Item	RX65N (SCIg, SCli, SCih)	RX671 (SCIk, SCIm, SCih)
Bit rate modulation function	Ability to reduce errors by correcting output from the on-chip baud rate generator	Ability to reduce errors by correcting output from the on-chip baud rate generator
Event link function (supported by SCI5 only)	<ul style="list-style-type: none"> <li>• Error (receive error or error signal detection) event output</li> <li>• Receive data full event output</li> <li>• Transmit data empty event output</li> <li>• Transmit end event output</li> </ul>	<ul style="list-style-type: none"> <li>• Error (receive error or error signal detection) event output</li> <li>• Receive data full event output</li> <li>• Transmit data empty event output</li> <li>• Transmit end event output</li> </ul>

**Table 2.54 Comparative Listing of Serial Communications Interface Channels**

Item	RX65N (SCIg, SCli, SCih)	RX671 (SCIk, SCIm, SCih)
Asynchronous mode	SCI0 to SCI12	SCI0 to SCI12
Clock synchronous mode	SCI0 to SCI12	SCI0 to SCI12
Smart card interface mode	SCI0 to SCI12	SCI0 to SCI12
Simple I <sup>2</sup> C mode	SCI0 to SCI12	SCI0 to SCI12
Simple SPI mode	SCI0 to SCI12	SCI0 to SCI12
FIFO mode	SCI10, SCI11	SCI10, SCI11
Data match detection	SCI10, SCI11	SCI0 to SCI11
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	SCI5	SCI5
Peripheral module clock	PCLKB: SCI0 to SCI9, SCI12 PCLKA: SCI10, SCI11	PCLKB: SCI0 to SCI9, SCI12 PCLKA: SCI10, SCI11

**Table 2.55 Comparison of Serial Communications Interface Registers**

Register	Bit	RX65N (SClg, SCli, SClh)	RX671 (SCIk, SCIm, SCIh)
SEMR	ITE	—	Immediate transmit enable bit
	ABCSE	—	Clock-synchronous basic clock select extended bit
SPTR	RXDMON	RXD line monitoring bit  0: RXDn pin is low-level 1: RXDn pin is high-level	RXD line monitoring bit  When RINV = 0 0: RXDn pin is low-level 1: RXDn pin is high-level <b>When RINV = 1</b> <b>0: RXDn pin is high-level</b> <b>1: RXDn pin is low-level</b>
	SPB2DT SPB2IO	Serial port break data bit Serial port break I/O bit  In clock-synchronous mode, the TXDn pins are controlled by the SCR.TE, SPB2DT, and SPB2IO bits in combination. For details, refer to Table 2.56.	Serial port break data bit Serial port break I/O bit  The TXDn pins are controlled by the SCR.TE, SPB2DT, SPB2IO, and TINV bits in combination. For details, refer to Table 2.56. These settings take effect in clock-synchronous mode only.
	RINV	—	Receive input invert bit
	TINV	—	Transmit output invert bit
	RTADJ	—	Receive data sampling timing adjustment bit
	TTADJ	—	Transmit signal change timing adjustment bit
TMGR	—	—	Transmit/receive timing select register

**Table 2.56 Comparison of TXDn Pin Control Settings**

SCR.TE Bit Setting Value	SPB2IO Bit Setting Value	SPB2DT Bit Setting Value	TXDn Pin State	
			RX65N	RX671
0 (transmit disabled)	0 (input)	Any value	Hi-Z	Hi-Z
	1 (output)	0	Low-level output	When TINV bit = 0 Low-level output <b>When TINV bit = 1</b> <b>High-level output</b>
		1	High-level output	When TINV bit = 0 High-level output <b>When TINV bit = 1</b> <b>Low-level output</b>
1 (transmit enabled)	Any value	Any value	Transmit data output pin	Transmit data output pin

## 2.19 Serial Peripheral Interface

Table 2.57 is a comparative overview of the serial peripheral interfaces, and Table 2.58 is a comparison of serial peripheral interface registers.

**Table 2.57 Comparative Overview of Serial Peripheral Interfaces**

Item	RX65N (RSPIC)	RX671 (RSPID)
Number of channels	3 channels	3 channels
RSPI transfer functions	<ul style="list-style-type: none"> <li>Ability to use MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals to implement serial communication through SPI operation (four-wire method) or clock synchronous operation (three-wire method).</li> <li>Ability to perform transmit-only operation</li> <li>Communication mode: Selectable between full-duplex and transmit-only</li> <li>Ability to switch the polarity of RSPCK</li> <li>Ability to switch the phase of RSPCK</li> </ul>	<ul style="list-style-type: none"> <li>Ability to use MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals to implement serial communication through SPI operation (four-wire method) or clock synchronous operation (three-wire method).</li> <li>Communication mode: Selectable between full-duplex and simplex (transmit-only or receive-only (in slave mode))</li> <li>Ability to switch the polarity of RSPCK</li> <li>Ability to switch the phase of RSPCK</li> </ul>
Data format	<ul style="list-style-type: none"> <li>Selectable between MSB-first and LSB-first</li> <li>Ability to select transfer bit length among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, and 32 bits</li> <li>128-bit transmit/receive buffers</li> <li>Ability to transfer up to four frames in each round of transmission/reception (with up to 32 bits per frame)</li> <li>Ability to swap transmit and receive data in byte units</li> </ul>	<ul style="list-style-type: none"> <li>Selectable between MSB-first and LSB-first</li> <li>Ability to select transfer bit length among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, and 32 bits</li> <li>128-bit transmit/receive buffers</li> <li>Ability to transfer up to four frames in each round of transmission/reception (with up to 32 bits per frame)</li> <li>Ability to swap transmit/receive data in byte units</li> <li>Ability to invert the logic level of transmit/receive data</li> </ul>
Bit rate	<ul style="list-style-type: none"> <li>In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (division ratio: 2 to 4,096).</li> <li>In slave mode, PCLK divided by a minimum of 4 can be input as RSPCK (RSPCK maximum frequency: PCLK divided by 4).                             <ul style="list-style-type: none"> <li>Width at high level: 2 cycles of PCLK; width at low level: 2 cycles of PCLK</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (division ratio: 2 to 4,096).</li> <li>In slave mode, PCLK divided by a minimum of 4 can be input as RSPCK (RSPCK maximum frequency: PCLK divided by 4).                             <ul style="list-style-type: none"> <li>Width at high level: 2 cycles of PCLK; width at low level: 2 cycles of PCLK</li> </ul> </li> </ul>
Buffer configuration	<ul style="list-style-type: none"> <li>Double buffer configuration for both the transmit and receive buffers</li> <li>128 bits for the transmit/receive buffers</li> </ul>	<ul style="list-style-type: none"> <li>Double buffer configuration for both the transmit and receive buffers</li> <li>128 bits for the transmit/receive buffers</li> </ul>

Item	RX65N (RSPic)	RX671 (RSPId)
Error detection	<ul style="list-style-type: none"> <li>• Mode fault error detection</li> <li>• Overrun error detection</li> <li>• Parity error detection</li> <li>• Underrun error detection</li> </ul>	<ul style="list-style-type: none"> <li>• Mode fault error detection</li> <li>• Overrun error detection</li> <li>• Parity error detection</li> <li>• Underrun error detection</li> </ul>
SSL control function	<ul style="list-style-type: none"> <li>• Four SSL pins (SSLx0 to SSLx3) per channel</li> <li>• In single-master mode, SSLx0 to SSLx3 pins are output.</li> <li>• In multi-master mode, the SSLx0 pin is input, and SSLx1 to SSLx3 pins are either output or unused.</li> <li>• In slave mode, the SSLx0 pin is input, and SSLx1 to SSLx3 pins are unused.</li> <li>• Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay)                             <ul style="list-style-type: none"> <li>— Setting range: 1 to 8 RSPCK cycles</li> <li>— Setting unit: One RSPCK cycle</li> </ul> </li> <li>• Controllable delay from RSPCK stop to SSL output negation (SSL negation delay)                             <ul style="list-style-type: none"> <li>— Setting range: 1 to 8 RSPCK cycles</li> <li>— Setting unit: One RSPCK cycle</li> </ul> </li> <li>• Controllable wait until next-access SSL output assertion (next-access delay)                             <ul style="list-style-type: none"> <li>— Setting range: 1 to 8 RSPCK cycles</li> <li>— Setting unit: One RSPCK cycle</li> </ul> </li> <li>• Function for changing SSL polarity</li> </ul>	<ul style="list-style-type: none"> <li>• Four SSL pins (SSLx0 to SSLx3) per channel</li> <li>• In single-master mode, SSLx0 to SSLx3 pins are output.</li> <li>• In multi-master mode, the SSLx0 pin is input, and SSLx1 to SSLx3 pins are either output or unused.</li> <li>• In slave mode, the SSLx0 pin is input, and SSLx1 to SSLx3 pins are unused.</li> <li>• Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay)                             <ul style="list-style-type: none"> <li>— Setting range: 1 to 8 RSPCK cycles</li> <li>— Setting unit: One RSPCK cycle</li> </ul> </li> <li>• Controllable delay from RSPCK stop to SSL output negation (SSL negation delay)                             <ul style="list-style-type: none"> <li>— Setting range: 1 to 8 RSPCK cycles</li> <li>— Setting unit: One RSPCK cycle</li> </ul> </li> <li>• Controllable wait until next-access SSL output assertion (next-access delay)                             <ul style="list-style-type: none"> <li>— Setting range: 1 to 8 RSPCK cycles</li> <li>— Setting unit: One RSPCK cycle</li> </ul> </li> <li>• Function for changing SSL polarity</li> </ul>
Control during master transfer	<ul style="list-style-type: none"> <li>• A transfer of up to eight commands can be executed sequentially in looped execution.</li> <li>• For each command, the following items can be set:                             <ul style="list-style-type: none"> <li>— SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay</li> </ul> </li> <li>• A transfer can be initiated by writing to the transmit buffer.</li> <li>• The MOSI signal value at SSL negation can be specified.</li> <li>• RSPCK auto-stop function</li> </ul>	<ul style="list-style-type: none"> <li>• A transfer of up to eight commands can be executed sequentially in looped execution.</li> <li>• For each command, the following items can be set:                             <ul style="list-style-type: none"> <li>— SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay</li> </ul> </li> <li>• A transfer can be initiated by writing to the transmit buffer.</li> <li>• The MOSI signal value at SSL negation can be specified.</li> <li>• RSPCK auto-stop function</li> <li>• <b>The delay between data bytes can be shortened during burst transfers.</b></li> </ul>
Interrupt sources	Interrupt sources <ul style="list-style-type: none"> <li>• Receive buffer full interrupt</li> <li>• Transmit buffer empty interrupt</li> <li>• RSPi error interrupt (mode fault, overrun, underrun, or parity error)</li> <li>• RSPi idle interrupt (RSPi idle)</li> </ul>	Interrupt sources <ul style="list-style-type: none"> <li>• Receive buffer full interrupt</li> <li>• Transmit buffer empty interrupt</li> <li>• Error interrupt (mode fault, overrun, underrun, or parity error)</li> <li>• Idle interrupt</li> <li>• <b>Communication end interrupt</b></li> </ul>

Item	RX65N (RSPIC)	RX671 (RSPID)
Event link function (output)	The following events can be output to the event link controller (RSPI0): <ul style="list-style-type: none"> <li>• Receive buffer full event signal</li> <li>• Transmit buffer empty event signal</li> <li>• Mode fault, overrun, underrun, or parity error event signal</li> <li>• RSPI idle event signal</li> <li>• Transmission-completed event signal</li> </ul>	The following events can be output to the event link controller (RSPI0): <ul style="list-style-type: none"> <li>• Receive buffer full event signal</li> <li>• Transmit buffer empty event signal</li> <li>• Error events (mode fault, overrun, underrun, parity error)</li> <li>• Idle events</li> <li>• Communication completion events</li> </ul>
Other functions	<ul style="list-style-type: none"> <li>• Function for switching between CMOS and open-drain output</li> <li>• Function for initializing the RSPI</li> <li>• Loopback mode</li> </ul>	<ul style="list-style-type: none"> <li>• Function for initializing the RSPI</li> <li>• Loopback mode</li> </ul>
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

**Table 2.58 Comparison of Serial Peripheral Interface Registers**

Register	Bit	RX65N (RSPIC)	RX671 (RSPID)
SPSR	SPCF	—	Communication completion flag
SPCR2	SPPE	Parity enable bit  0: No transmit data parity bit appended No parity checking is performed on receive data.  1: A transmit data parity bit is appended. Parity checking is performed on receive data.	Parity enable bit  0: No transmit data parity bit appended No parity checking is performed on receive data.  1: A transmit data parity bit is appended, and parity checking is performed on receive data (when SPCR.TXMD = 0). A parity bit is appended to transmit data, but no parity checking is performed on receive data (when SPCR.TXMD = 1).
SPDCR2	DINV	—	Transfer data invert bit
SPCR3	—	—	RSPI control register 3

## 2.20 Quad Serial Peripheral Interface/Quad SPI Memory Interface

Table 2.59 is a comparative overview of the quad serial peripheral interface and quad SPI memory interface, and Table 2.60 is a comparison of quad serial peripheral interface and quad SPI memory interface registers.

**Table 2.59 Comparative Overview of Quad Serial Peripheral Interface and Quad SPI Memory Interface**

Item	RX65N (QSPI)	RX671 (QSPIX)
Channels	1 channel	1 channel
SPI	<ul style="list-style-type: none"> <li>Ability to communicate with serial flash memory using <b>single-</b>, dual-, or quad-SPI operation</li> <li>Ability to configure SPI modes 0 to 4</li> </ul>	<ul style="list-style-type: none"> <li>Support for <b>extended SPI</b>, dual-SPI, and quad-SPI protocols</li> <li>Ability to configure SPI modes 0 and 3</li> <li>Ability to select address width of 8, 16, 24, or 32 bits</li> </ul>
Timing adjustment function	—	Ability to implement configurations supporting a variety of serial flash specifications
Memory mapped mode	—	<ul style="list-style-type: none"> <li>Support for read, fast read, fast read dual output, fast read dual I/O, fast read quad output, and fast read quad I/O instructions</li> <li>Ability to substitute instruction codes</li> <li>Ability to adjust dummy cycle count</li> <li>Prefetch function</li> <li>Polling processing</li> <li>SPI bus cycle extension function</li> </ul>
Indirect access mode	—	Flexible support using software control for various serial flash instructions/functions, including erase, write, ID read, and power down control
Interrupt sources	<ul style="list-style-type: none"> <li>Receive buffer full interrupt</li> <li>Transmit buffer empty interrupt</li> <li>QSSL negate interrupt</li> </ul>	<ul style="list-style-type: none"> <li>Error interrupt</li> </ul>
Module stop function	Ability to transition to module stop state	Ability to reduce power consumption by enabling module stop state

**Table 2.60 Comparison of Quad Serial Peripheral Interface and Quad SPI Memory Interface Registers**

Register	Bit	RX65N (QSPI)	RX671 (QSPIX)
SPCR	—	QSPI control register	—
SSLP	—	QSPI slave select polarity register	—
SPPCR	—	QSPI pin control register	—
SPSR	—	QSPI status register	SPI status register
		SPSR is a 16-bit register.	SPSR is a 32-bit register.
		Initial value after a reset differs.	
	SPSSLF	QSSL negate flag	—
	SPTEF	Transmit buffer empty flag	—
	TREND	Transmit end flag	—
	SPRFF	Receive buffer full flag	—
	BUSY	—	Bus busy flag
ROMAE	—	ROM access error flag	

Register	Bit	RX65N (QSPI)	RX671 (QSPIX)
SPDR	—	QSPI data register  Writing to this register is accomplished by writing to the transmit buffer (SPTXB), and reading from this register is accomplished by reading from the receive buffer (SPRXB). This register can be accessed in <b>byte, word, or</b> longword units.	SPI data register  <b>Reads and writes to this register are converted into SPI bus cycles. When the AMOD bit is set to 1, this register can only be accessed in indirect access mode. In memory mapped mode, accesses to this register are ignored.</b>
SPSCR	—	QSPI sequence control register	—
SPSSR	—	QSPI sequence status register	—
SPBR	—	QSPI bit rate register	—
SPDCR	TXDMY	Dummy data transmit enable bit	—
	DCYC[3:0]	—	Dummy cycle count setting bits
	XIPS	—	XIP status flag
	XIPE	—	XIP enable bit
	MODE[7:0]	—	Mode data bits
SPCKD	—	QSPI clock delay register	—
SSLND	—	QSPI slave select negate delay register	—
SPND	—	QSPI next access delay register	—
SPCMDn	—	QSPI command register n (n = 0 to 3)	—
SPBFCR	—	QSPI buffer control register	—
SPBDCR	—	QSP buffer data count setting register	—
SPBMULn	—	QSPI transfer data length multiple setting register n (n = 0 to 3)	—
SPMR0	—	—	Mode register 0
SPSSCR	—	—	Slave select signal control register
SPOCR	—	—	Operating clock control register
SPPFSR	—	—	Prefetch status register
SPMR1	—	—	Mode register 1
SPSR	—	—	SPI status register
SPRIR	—	—	Independent read instruction setting register
SPAMR	—	—	Address mode register
SPMR2	—	—	Mode register 2
SPPCR	—	—	Port control register
SPUAR	—	—	Upper-bit address register



## 2.21 Boundary Scan

Table 2.61 is a comparative overview of the boundary scan functions, and Table 2.62 is a comparison of boundary scan registers.

**Table 2.61 Comparative Overview of Boundary Scan Functions**

Item	RX65N	RX671
Boundary scan enable/disable	Boundary scan is enabled when the RES# pin and the BSCANP pin are driven high and the EMLE pin is driven low.	Boundary scan is enabled when the RES# pin and the BSCANP pin are driven high and the EMLE pin is driven low.
Dedicated boundary scan pins	The following pins are used exclusively by the JTAG when the boundary scan function is enabled: TDO, TCK, TDI, TMS, and TRST# <b>177-pin TFLGA and 176-pin LFBGA products: PF0, PF1, PF2, PF3, and PF4</b> 145-pin TFLGA and 64-pin TFBGA products: P26, P27, P30, P31, and P34	The following pins are used exclusively by the JTAG when the boundary scan function is enabled: TDO, TCK, TDI, TMS, and TRST#  145-pin TFLGA and 64-pin TFBGA products: P26, P27, P30, P31, and P34
Six test modes	<ul style="list-style-type: none"> <li>• BYPASS mode</li> <li>• EXTEST mode</li> <li>• SAMPLE/PRELOAD mode</li> <li>• CLAMP mode</li> <li>• HIGHZ mode</li> <li>• IDCODE mode</li> </ul>	<ul style="list-style-type: none"> <li>• BYPASS mode</li> <li>• EXTEST mode</li> <li>• SAMPLE/PRELOAD mode</li> <li>• CLAMP mode</li> <li>• HIGHZ mode</li> <li>• IDCODE mode</li> </ul>

**Table 2.62 Comparison of Boundary Scan Registers**

Register	Bit	RX65N	RX671
JTIDR	—	ID code register	ID code register
		<b>Initial value after a reset differs.</b>	

## 2.22 12-Bit A/D Converter

Table 2.63 is a comparative overview of the 12-bit A/D converters, and Table 2.64 is a comparison of 12-bit A/D converter registers.

**Table 2.63 Comparative Overview of 12-Bit A/D Converters**

Item	RX65N (S12ADFa)	RX671 (S12ADFa)
Number of units	2 units (S12AD, S12AD1)	2 units (S12AD, S12AD1)
Input channels	S12AD: 8 channels S12AD1: 21 channels + 1 extension	S12AD: 8 channels S12AD1: <b>12</b> channels + 1 extension
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	0.48 $\mu$ s per channel (12-bit conversion mode) 0.45 $\mu$ s per channel (10-bit conversion mode) 0.42 $\mu$ s per channel (8-bit conversion mode) (When A/D conversion clock (ADCLK) = 60 MHz)	0.48 $\mu$ s per channel (12-bit conversion mode) 0.45 $\mu$ s per channel (10-bit conversion mode) 0.42 $\mu$ s per channel (8-bit conversion mode) (When A/D conversion clock (ADCLK) = 60 MHz)
A/D conversion clock	<ul style="list-style-type: none"> <li>Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 2:1, 4:1, 8:1</li> <li>ADCLK is set using the clock generation circuit.</li> </ul>	<ul style="list-style-type: none"> <li>Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 2:1, 4:1, 8:1</li> <li>ADCLK is set using the clock generation circuit.</li> </ul>
Data registers	<ul style="list-style-type: none"> <li>29 registers for analog input (eight for S12AD and 21 for S12AD1), 1 for A/D-converted data duplication in double trigger mode per unit, and 2 for A/D-converted data duplication during extended operation in double trigger mode per unit.</li> <li>One register for temperature sensor (S12AD1)</li> <li>One register for internal reference (S12AD1)</li> <li>One register for self-diagnosis per unit</li> <li>The results of A/D conversion are stored in 12-bit A/D data registers.</li> <li>Support for output of A/D conversion results at 8-, 10-, or 12-bit accuracy</li> <li>The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode.</li> </ul>	<ul style="list-style-type: none"> <li><b>20</b> registers for analog input (eight for S12AD and <b>12</b> for S12AD1), 1 for A/D-converted data duplication in double trigger mode per unit, and 2 for A/D-converted data duplication during extended operation in double trigger mode per unit.</li> <li>One register for temperature sensor (S12AD1)</li> <li>One register for internal reference (S12AD1)</li> <li>One register for self-diagnosis per unit</li> <li>The results of A/D conversion are stored in 12-bit A/D data registers.</li> <li>Support for output of A/D conversion results at 8-, 10-, or 12-bit accuracy</li> <li>The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode.</li> </ul>

Item	RX65N (S12ADFa)	RX671 (S12ADFa)
Data registers	<ul style="list-style-type: none"> <li>• Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.</li> <li>• Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.</li> </ul>	<ul style="list-style-type: none"> <li>• Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.</li> <li>• Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.</li> </ul>
Operating modes	<p>Operating modes can be set independently for two units.</p> <ul style="list-style-type: none"> <li>• Single scan mode:                             <ul style="list-style-type: none"> <li>— A/D conversion is performed only once on the analog inputs arbitrarily selected.</li> <li>— A/D conversion is performed only once on the temperature sensor output (S12AD1).</li> <li>— A/D conversion is performed only once on the internal reference voltage (S12AD1).</li> <li>— A/D conversion is performed only once on the extended analog input (S12AD1).</li> </ul> </li> <li>• Continuous scan mode:                             <ul style="list-style-type: none"> <li>— A/D conversion is performed repeatedly on the analog input, temperature sensor output (S12AD1), and internal reference voltage (S12AD1) of an arbitrarily selected channel.</li> <li>— A/D conversion is performed repeatedly on the extended analog input (S12AD1).</li> </ul> </li> <li>• Group scan mode:                             <ul style="list-style-type: none"> <li>— Two (groups A and B) or three (groups A, B, and C) can be selected as the number of the groups to be used. (Only the combination of groups A and B can be selected when the number of the groups is two.)</li> <li>— Analog inputs, temperature sensor output (S12AD1), and internal reference voltage (S12AD1) that are arbitrarily selected are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once.</li> </ul> </li> </ul>	<p>Operating modes can be set independently for two units.</p> <ul style="list-style-type: none"> <li>• Single scan mode:                             <ul style="list-style-type: none"> <li>— A/D conversion is performed only once on the analog inputs arbitrarily selected.</li> <li>— A/D conversion is performed only once on the temperature sensor output (S12AD1).</li> <li>— A/D conversion is performed only once on the internal reference voltage (S12AD1).</li> <li>— A/D conversion is performed only once on the extended analog input (S12AD1).</li> </ul> </li> <li>• Continuous scan mode:                             <ul style="list-style-type: none"> <li>— A/D conversion is performed repeatedly on the analog input, temperature sensor output (S12AD1), and internal reference voltage (S12AD1) of an arbitrarily selected channel.</li> <li>— A/D conversion is performed repeatedly on the extended analog input (S12AD1).</li> </ul> </li> <li>• Group scan mode:                             <ul style="list-style-type: none"> <li>— Two (groups A and B) or three (groups A, B, and C) can be selected as the number of the groups to be used. (Only the combination of groups A and B can be selected when the number of the groups is two.)</li> <li>— Analog inputs, temperature sensor output (S12AD1), and internal reference voltage (S12AD1) that are arbitrarily selected are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once.</li> </ul> </li> </ul>

Item	RX65N (S12ADFa)	RX671 (S12ADFa)
Operating modes	<ul style="list-style-type: none"> <li>— The conditions for scanning start of groups A, B, and C (synchronous trigger) can be independently selected, thus allowing A/D conversion of each group to be started independently.</li> <li>• Group scan mode (when group priority control selected):                             <ul style="list-style-type: none"> <li>— If a priority-group trigger is input during scanning of the low-priority group, scan of the low-priority group is stopped and scan of the priority group is started. The priority order is group A (highest) &gt; group B &gt; group C (lowest).</li> <li>— Whether or not to restart scanning of the low-priority group after processing for the high-priority group completes, is selectable. Rescan can also be set to start either from the beginning of the selected channel or the channel on which A/D conversion is not completed.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>— The conditions for scanning start of groups A, B, and C (synchronous trigger) can be independently selected, thus allowing A/D conversion of each group to be started independently.</li> <li>• Group scan mode (when group priority control selected):                             <ul style="list-style-type: none"> <li>— If a priority-group trigger is input during scanning of the low-priority group, scan of the low-priority group is stopped and scan of the priority group is started. The priority order is group A (highest) &gt; group B &gt; group C (lowest).</li> <li>— Whether or not to restart scanning of the low-priority group after processing for the high-priority group completes, is selectable. Rescan can also be set to start either from the beginning of the selected channel or the channel on which A/D conversion is not completed.</li> </ul> </li> </ul>
Conditions for A/D conversion start	<ul style="list-style-type: none"> <li>• Software trigger</li> <li>• Synchronous trigger: Trigger by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), 16-bit timer pulse unit (TPU), or event link controller (ELC).</li> <li>• Asynchronous trigger: A/D conversion can be triggered by the external trigger ADTRG0# (S12AD) or ADTRG1# (S12AD1) pin (independently for two units).</li> </ul>	<ul style="list-style-type: none"> <li>• Software trigger</li> <li>• Synchronous trigger: Trigger by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), 16-bit timer pulse unit (TPU), or event link controller (ELC).</li> <li>• Asynchronous trigger: A/D conversion can be triggered by the external trigger ADTRG0# (S12AD) or ADTRG1# (S12AD1) pin (independently for two units).</li> </ul>
Functions	<ul style="list-style-type: none"> <li>• <b>Channel-dedicated sample-and-hold function (three channels for S12AD only)</b></li> <li>• Variable sampling time (can be set per channel)</li> <li>• Self-diagnosis of 12-bit A/D converter</li> <li>• Selectable A/D-converted value addition mode or average mode</li> <li>• Analog input disconnection detection assist function (discharge function/precharge function)</li> <li>• Double trigger mode (duplication of A/D conversion data)</li> <li>• 12-/10-/8-bit conversion switching</li> <li>• Automatic clear function of A/D data registers</li> <li>• Extended analog input</li> <li>• Comparison function (windows A and B)</li> </ul>	<ul style="list-style-type: none"> <li>• Variable sampling time (can be set per channel)</li> <li>• Self-diagnosis of 12-bit A/D converter</li> <li>• Selectable A/D-converted value addition mode or average mode</li> <li>• Analog input disconnection detection assist function (discharge function/precharge function)</li> <li>• Double trigger mode (duplication of A/D conversion data)</li> <li>• 12-/10-/8-bit conversion switching</li> <li>• Automatic clear function of A/D data registers</li> <li>• Extended analog input</li> <li>• Comparison function (windows A and B)</li> </ul>

Item	RX65N (S12ADFa)	RX671 (S12ADFa)
Interrupt sources	<ul style="list-style-type: none"> <li>• In the modes except double trigger mode and group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of single scan. (Independently for two units).</li> <li>• In double trigger mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of double scan. (Independently for two units).</li> <li>• In group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a group A scan, whereas a group B–exclusive scan end interrupt request (S12GBADI or S12GBADI1) can be generated on completion of a group B scan, and a group C–exclusive scan end interrupt request (S12GCADI or S12GCADI1) can be generated on completion of a group C scan.</li> <li>• When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a double scan of group A, and a scan end interrupt request exclusive to the corresponding group (S12GBADI/S12GCADI or S12GBADI1/S12GCADI1) can be generated on completion of a group B or group C scan.</li> <li>• A compare interrupt request (S12CMPAI, S12CMPAI1, S12CMPBI, or S12CMPBI1) can be generated upon a match with the comparison condition for the digital compare function.</li> <li>• The S12ADI/S12ADI1, S12GBADI/S12GBADI1, and S12GCADI/S12GCADI1 interrupts can trigger the DMA controller (DMAC) and data transfer controller (DTC).</li> </ul>	<ul style="list-style-type: none"> <li>• In the modes except double trigger mode and group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of single scan. (Independently for two units).</li> <li>• In double trigger mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of double scan. (Independently for two units).</li> <li>• In group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a group A scan, whereas a group B–exclusive scan end interrupt request (S12GBADI or S12GBADI1) can be generated on completion of a group B scan, and a group C–exclusive scan end interrupt request (S12GCADI or S12GCADI1) can be generated on completion of a group C scan.</li> <li>• When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a double scan of group A, and a scan end interrupt request exclusive to the corresponding group (S12GBADI/S12GCADI or S12GBADI1/S12GCADI1) can be generated on completion of a group B or group C scan.</li> <li>• A compare interrupt request (S12CMPAI, S12CMPAI1, S12CMPBI, or S12CMPBI1) can be generated upon a match with the comparison condition for the digital compare function.</li> <li>• The S12ADI/S12ADI1, S12GBADI/S12GBADI1, and S12GCADI/S12GCADI1 interrupts can trigger the DMA controller (DMAC) and data transfer controller (DTC).</li> </ul>
Event linking function	<ul style="list-style-type: none"> <li>• The ELC event signal is generated when all scans are finished.</li> <li>• Able to start scanning by a trigger from the ELC.</li> </ul>	<ul style="list-style-type: none"> <li>• The ELC event signal is generated when all scans are finished.</li> <li>• Able to start scanning by a trigger from the ELC.</li> </ul>
Low power consumption function	Module stop state can be set.	Module stop state can be set.

**Table 2.64 Comparison of 12-Bit A/D Converter Registers**

Register	Bit	RX65N (S12ADFa)	RX671 (S12ADFa)
ADDRy	—	A/D data registers y (y = 0 to 7: S12AD, y = 0 to 20: S12AD1)	A/D data registers y (y = 0 to 11)
S12AD1. ADANSA0	ANSA012 to ANSA015	A/D conversion channel select bits	—
ADANSA1	—	A/D channel select register A1	—
S12AD1. ADANSB0	ANSB012 to ANSB015	A/D conversion channel select bits	—
ADANSB1	—	A/D channel select register B1	—
S12AD1. ADANSC0	ANSC012 to ANSC015	A/D conversion channel select bits	—
ADANSC1	—	A/D channel select register C1	—
S12AD1. ADADS0	ADS012 to ADS015	A/D-converted value addition/average channel select bits	—
ADADS1	—	A/D-converted value addition/ average function channel select register 1	—
ADSSTRn	—	A/D sampling state register n (n = 0 to 15, L, T, O)	A/D sampling state register n (n = 0 to 11, T, O)
ADSHCR	—	A/D sample-and-hold circuit control register	—
ADSHMSR	—	A/D sample-and-hold operating mode select register	—
S12AD1. ADCMPANSR0	CMPCHA012 to CMPCHA015	Comparison window A channel select bits	—
ADCMPANSR1	—	A/D comparison function window A channel select register 1	—
S12AD1. ADCMPLR0	CMPLCHA012 to CMPLCHA015	Comparison window A comparison condition select bits	—
ADCMPLR1	—	A/D comparison function window A comparison condition setting register 1	—
S12AD1. ADCMPSR0	CMPSTCHA012 to CMPSTCHA015	Comparison window A flags	—
ADCMPSR1	—	A/D comparison function window A channel status register 1	—

## 2.23 Data Operation Circuit

Table 2.65 is a comparative overview of data operation circuit, and Table 2.66 is a comparison of data operation circuit registers.

**Table 2.65 Comparative Overview of Data Operation Circuit**

Item	RX65N (DOC)	RX671 (DOCA)
Data operation functions	<ul style="list-style-type: none"> <li>16-bit data comparison, addition, and subtraction</li> </ul>	<ul style="list-style-type: none"> <li>Comparison of 16- or 32-bit data (match/mismatch, greater/less, in/out of range)</li> <li>Addition or subtraction of 16- or 32-bit data</li> </ul>
Low power consumption function	Module stop state can be set.	Ability to specify module stop state
Interrupts	<ul style="list-style-type: none"> <li>The compared values either match or mismatch</li> <li>The result of data addition is greater than FFFFh</li> <li>The result of data subtraction is less than 0000h</li> </ul>	<ul style="list-style-type: none"> <li>When data comparison result matches detection condition</li> <li>When data addition result is greater than FFFFh (when DOCR.DOPSZ = 0) or FFFF FFFFh (when DOCR.DOPSZ = 1) (overflow)</li> <li>When data subtraction result is less than 0000h (when DOCR.DOPSZ = 0) or 0000 0000h (when DOCR.DOPSZ = 1) (underflow)</li> </ul>
Event linking function (output)	<ul style="list-style-type: none"> <li>The compared values either match or mismatch</li> <li>The result of data addition is greater than FFFFh</li> <li>The result of data subtraction is less than 0000h</li> </ul>	<ul style="list-style-type: none"> <li>When data comparison result matches detection condition</li> <li>When data addition result is greater than FFFFh (when DOCR.DOPSZ = 0) or FFFF FFFFh (when DOCR.DOPSZ = 1) (overflow)</li> <li>When data subtraction result is less than 0000h (when DOCR.DOPSZ = 0) or 0000 0000h (when DOCR.DOPSZ = 1) (underflow)</li> </ul>

**Table 2.66 Comparison of Data Operation Circuit Registers**

Register	Bit	RX65N (DOC)	RX671 (DOCA)
DOCR	DCSEL (RX65N) DCSEL[2:0] (RX671)	Detection condition select bit (b2)  Data comparison result 0: Detect mismatches 1: Detect matches	Detection condition select bits (b6 to b4)  b6 b4 0 0 0: Mismatch (DODIR ≠ DODSR0) 0 0 1: Match (DODIR = DODSR0) 0 1 0: Less (DODIR < DODSR0) 0 1 1: Greater (DODIR > DODSR0) 1 0 0: In range (DODSR0 < DODIR < DODSR1) 1 0 1: Out of range (DODIR < DODSR0, DODSR1 < DODIR) Other than above: Setting prohibited.
	DOPSZ	—	Data operation size select bit
	DOPCIE	Data operation circuit interrupt enable bit (b4)	Data operation circuit interrupt enable bit (b7)
	DOPCF	Data operation circuit flag	—
	DOPCFCL	DOPCF clear bit	—
DOSR	—	—	DOC status register
DOSCR	—	—	DOC status clear register
DODIR	—	DOC data input register  DODIR is a 16-bit register.	DOC data input register  DODIR is a 32-bit register. Access this register in units equal to the data operation size specified by the DOCR.DOPSZ bit.
DODSR (RX65N) DODSR0/ DODSR1 (RX671)	—	DOC data setting register  DODSR is a 16-bit register.	DOC data setting registers 0 and 1  DODSR0 and DODSR1 are 32-bit registers. Access these registers in units equal to the data operation size specified by the DOCR.DOPSZ bit.



## 2.24 RAM

Table 2.67 is a comparative overview of RAM, and Table 2.68 is a comparison of RAM registers.

**Table 2.67 Comparative Overview of RAM**

Item	RX65N		RX671
	RAM	Expansion RAM* <sup>1</sup>	RAM
Capacity	256 KB	384 KB	384 KB
Address	0000 0000h to 0003 FFFFh	0080 0000h to 0085 FFFFh	0000 0000h to 0005 FFFFh
Memory bus	Memory bus 1	Memory bus 3	Memory bus 1
Access	<ul style="list-style-type: none"> <li>Single-cycle access is possible for both reading and writing.</li> <li>RAM can be enabled or disabled.</li> </ul>		<ul style="list-style-type: none"> <li>Single-cycle access is possible for both reading and writing.</li> <li>RAM can be enabled or disabled.</li> </ul>
Data retention function	Not available in deep software standby mode		Not available in deep software standby mode
Low power consumption function	Transition to module stop state can be enabled separately for RAM and expansion RAM* <sup>1</sup> .		Ability to transition to the module stop state
Error checking	<ul style="list-style-type: none"> <li>Parity checking: 1-bit error detection</li> <li>A non-maskable interrupt or interrupt is generated in response to an error.</li> </ul>		<ul style="list-style-type: none"> <li>Parity checking: 1-bit error detection</li> <li>A non-maskable interrupt or interrupt is generated in response to an error.</li> </ul>

Note: 1. Only on products with a code flash memory capacity of 1.5 MB or more.

**Table 2.68 Comparison of RAM Registers**

Register	Bit	RX65N	RX671
EXRAMMODE	—	Expansion RAM operating mode control register	—
EXRAMSTS	—	Expansion RAM error status register	—
EXRAMECAD	—	Expansion RAM error address capture register	—
EXRAMPRCR	—	Expansion RAM protection register	—

## 2.25 Standby RAM

Table 2.69 is a comparative overview of standby RAM.

**Table 2.69 Comparative Overview of Standby RAM**

Item	RX65N	RX671
RAM capacity	8 KB	4 KB
RAM address	000A 4000h to 000A 5FFFh	000A 4000h to 000A 4FFFh
Access	<ul style="list-style-type: none"> <li>Both read and write operations take 2 or 3 cycles of PCLKB when ICLK ≥ PCLKB; two cycles of ICLK are needed when ICLK &lt; PCLKB.</li> <li>Ability to enable or disable RAM access</li> <li>The endian order conforms to the endian setting of the chip.</li> <li>Non-aligned access is prohibited. Correct operation is not guaranteed if non-aligned access is attempted.</li> </ul>	<ul style="list-style-type: none"> <li>Both read and write operations take 2 or 3 cycles of PCLKB when ICLK ≥ PCLKB; two cycles of ICLK are needed when ICLK &lt; PCLKB.</li> <li>Ability to enable or disable RAM access</li> <li>The endian order conforms to the endian setting of the chip.</li> <li>Non-aligned access is prohibited. Correct operation is not guaranteed if non-aligned access is attempted.</li> </ul>
Data retention function	Data can be retained in deep software standby mode.	Data can be retained in deep software standby mode.
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

## 2.26 Flash Memory

Table 2.70 is a comparative overview of flash memory, and Table 2.71 is a comparison of flash memory registers.

**Table 2.70 Comparative Overview of Flash Memory**

Item	RX65N		RX671 (FLASH)	
	Code Flash Memory	Data Flash Memory	Code Flash Memory	Data Flash Memory
Memory capacity	User area: Up to 2 MB	Data area: 32 KB	User area: Up to 2 MB	Data area: 8 KB
Address	<ul style="list-style-type: none"> <li>When capacity is 2 MB: FFE0 0000h to FFFF FFFFh</li> <li>When capacity is 1.5 MB: FFE8 0000h to FFFF FFFFh</li> <li>When capacity is 1 MB: FFF0 0000h to FFFF FFFFh</li> <li>When capacity is 768 KB: FFF4 0000h to FFFF FFFFh</li> <li>When capacity is 512 KB: FFF8 0000h to FFFF FFFFh</li> </ul>	0010 0000h to 0010 7FFFh	<ul style="list-style-type: none"> <li>When capacity is 2 MB: FFE0 0000h to FFFF FFFFh</li> <li>When capacity is 1.5 MB: FFE8 0000h to FFFF FFFFh</li> <li>When capacity is 1 MB: FFF0 0000h to FFFF FFFFh</li> </ul>	0010 0000h to 0010 1FFFh
ROM cache	<ul style="list-style-type: none"> <li>Capacity: Up to 256 Bytes</li> <li>Mapping method: 8-way set associative</li> <li>Replace method: LRU algorithm</li> <li>Line size: 16 bytes</li> </ul>	—	<ul style="list-style-type: none"> <li>Capacity: 8 KB</li> <li>Mapping method: direct mapping</li> <li>Line size: 16 bytes</li> </ul>	—

Item	RX65N		RX671 (FLASH)	
	Code Flash Memory	Data Flash Memory	Code Flash Memory	Data Flash Memory
Read cycle	<ul style="list-style-type: none"> <li>When the cache is hit: One cycle</li> <li>When the cache is missed while ROM cache operation is enabled, or when ROM cache operation is disabled: <ul style="list-style-type: none"> <li>— ICLK ≤ 50 MHz One cycle</li> <li>— 50 MHz &lt; ICLK ≤ 100 MHz Two cycles</li> <li>— ICLK &gt; 100 MHz Three cycles</li> </ul> </li> </ul>	Reading proceeds in every cycle of FCLK.	<ul style="list-style-type: none"> <li>While ROM cache operation is enabled: <ul style="list-style-type: none"> <li>— When the cache is hit: One cycle</li> <li>— When the cache is missed: <b>One to two cycles when ICLK ≤ 60 MHz; two to three cycles when ICLK &gt; 60 MHz</b></li> </ul> </li> <li>When ROM cache operation is disabled: <ul style="list-style-type: none"> <li>— One cycle <b>when ICLK ≤ 60 MHz</b></li> <li>— Two cycles <b>when ICLK &gt; 60 MHz</b></li> </ul> </li> </ul>	Reading proceeds in every cycle of FCLK.
Value after erasure	FFh	Undefined	FFh	Undefined
Programming/erasing method	<ul style="list-style-type: none"> <li>Programming or erasure of the code flash memory and data flash memory, and programming of the option-setting memory, by means of FACL commands specified in the FACL command issuing area (007E 0000h) (self-programming)</li> <li>Programming or erasure through transfer by a serial-programmer via a serial interface (serial programming)</li> </ul>		<ul style="list-style-type: none"> <li>Programming or erasure of the code flash memory and data flash memory, and programming of the option-setting memory, by means of FACL commands specified in the FACL command issuing area (007E 0000h) (self-programming)</li> <li>Programming or erasure through transfer by a serial-programmer via a serial interface (serial programming)</li> </ul>	
Security function	Protects against illicit tampering or reading of data in flash memory		Protects against illicit tampering or reading of data in flash memory	
Protection function	Protects against erroneous rewriting of the flash memory (software protection, error protection, startup program protection function, area protection, and dual-bank function)		Protects against erroneous rewriting of the flash memory (software protection, error protection, startup program protection function, area protection, and dual-bank function)	
Dual bank function	<p>The dual-bank configuration enables safe updating in cases where programming is suspended.</p> <ul style="list-style-type: none"> <li>Linear mode: the code flash memory is used as one area.</li> <li>Dual mode: the code flash memory is divided into two areas.</li> </ul>	—	<p>The dual-bank configuration enables safe updating in cases where programming is suspended.</p> <ul style="list-style-type: none"> <li>Linear mode: the code flash memory is used as one area.</li> <li>Dual mode: the code flash memory is divided into two areas.</li> </ul>	—

Item	RX65N		RX671 (FLASH)	
	Code Flash Memory	Data Flash Memory	Code Flash Memory	Data Flash Memory
Trusted memory (TM) function	Protects against unauthorized reading of the code flash memory. <ul style="list-style-type: none"> <li>Linear mode: blocks 8 and 9</li> <li>Dual mode: blocks 8, 9, 46, and 47</li> </ul>	—	Protects against unauthorized reading of the code flash memory. <ul style="list-style-type: none"> <li>Linear mode: blocks 8 and 9</li> <li>Dual mode: blocks 8, 9, 46, and 47</li> </ul>	—
Background operation (BGO)	<ul style="list-style-type: none"> <li>The code flash memory can be read while the code flash memory is being programmed or erased.</li> <li>The data flash memory can be read while the code flash memory is being programmed or erased.</li> <li>The code flash memory can be read while the data flash memory is being programmed or erased.</li> </ul>		<ul style="list-style-type: none"> <li>The code flash memory can be read while the code flash memory is being programmed or erased.</li> <li>The data flash memory can be read while the code flash memory is being programmed or erased.</li> <li>The code flash memory can be read while the data flash memory is being programmed or erased.</li> </ul>	
Units of programming and erasure	<ul style="list-style-type: none"> <li>Unit of programming for the user area: 128 bytes</li> <li>Unit of erasure for the user area: Block</li> </ul>	<ul style="list-style-type: none"> <li>Unit of programming for data area: 4 bytes</li> <li>Unit of erasure for data area: 64, 128, or 256 bytes</li> </ul>	<ul style="list-style-type: none"> <li>Unit of programming for the user area: 128 bytes</li> <li>Unit of erasure for the user area: Block</li> </ul>	<ul style="list-style-type: none"> <li>Unit of programming for data area: 4 bytes</li> <li>Unit of erasure for data area: 64, 128, or 256 bytes</li> </ul>
Other functions	<ul style="list-style-type: none"> <li>Interrupts can be accepted during self-programming.</li> <li>The initial settings of the MCU can be specified in the option-setting memory.</li> </ul>		<ul style="list-style-type: none"> <li>Interrupts can be accepted during self-programming.</li> <li>The initial settings of the MCU can be specified in the option-setting memory.</li> </ul>	
On-board programming (serial programming/self-programming)	<ul style="list-style-type: none"> <li>Programming/erasure in boot mode (SCI interface)                             <ul style="list-style-type: none"> <li>The asynchronous serial interface (SCI1) is used.</li> <li>The transfer rate is adjusted automatically.</li> </ul> </li> <li>Programming/erasure in boot mode (USB interface)                             <ul style="list-style-type: none"> <li>USBb is used.</li> <li>Dedicated hardware is not required, so direct connection to a PC is possible.</li> </ul> </li> <li>Programming/erasure in boot mode (FINE interface)                             <ul style="list-style-type: none"> <li>FINE is used.</li> </ul> </li> <li>Programming or erasure by self-programming                             <ul style="list-style-type: none"> <li>Programming and erasure can be performed without resetting the system, and it is possible to read data from the code flash memory while erasure is in progress.</li> </ul> </li> </ul>		<ul style="list-style-type: none"> <li>Programming/erasure in boot mode (SCI interface)                             <ul style="list-style-type: none"> <li>The asynchronous serial interface (SCI1) is used.</li> <li>The transfer rate is adjusted automatically.</li> </ul> </li> <li>Programming/erasure in boot mode (USB interface)                             <ul style="list-style-type: none"> <li>USB is used.</li> <li>Dedicated hardware is not required, so direct connection to a PC is possible.</li> </ul> </li> <li>Programming/erasure in boot mode (FINE interface)                             <ul style="list-style-type: none"> <li>FINE is used.</li> </ul> </li> <li>Programming and erasure in single-chip mode                             <ul style="list-style-type: none"> <li>Programming and erasure can be performed by a code flash memory or data flash memory programming routine in a user program.</li> </ul> </li> </ul>	
Off-board programming	Programming or erasure of the code flash memory or option-setting memory are possible by using a parallel programmer.*1	Programming or erasure of the data flash memory by using a parallel programmer is not possible.*1	Programming or erasure of the code flash memory or option-setting memory are possible by using a parallel programmer.	Programming or erasure of the data flash memory by using a parallel programmer is not possible.
Unique ID	A 16-byte ID code is provided for each MCU.		A 16-byte ID code is provided for each MCU.	

Note: 1. Not supported on 64-pin products.

**Table 2.71 Comparison of Flash Memory Registers**

Register	Bit	RX65N	RX671
NCRGn	—	—	Non-cacheable area n address register (n = 0 or 1)
NCRCn	—	—	Non-cacheable area n setting register (n = 0 or 1)
FWEPROR	FLWE[1:0]	<p>Flash programming and erasure enable bits</p> <p>Products with 1.5 MB or more of code flash memory:</p> <p>b1 b0</p> <p>0 0: Disables programming and erasure, and blank checking.</p> <p>0 1: Enables programming and erasure, and blank checking.</p> <p>1 0: Disables programming and erasure, and blank checking.</p> <p>1 1: Disables programming and erasure, and blank checking.</p> <p>Products with 1 MB or less of code flash memory:</p> <p>b1 b0</p> <p>0 0: Disables programming and erasure.</p> <p>0 1: Enables programming and erasure.</p> <p>1 0: Disables programming and erasure.</p> <p>1 1: Disables programming and erasure.</p>	<p>Flash programming and erasure enable bits</p> <p>b1 b0</p> <p>0 0: Disables programming and erasure, and blank checking.</p> <p>0 1: Enables programming and erasure, and blank checking.</p> <p>1 0: Disables programming and erasure, and blank checking.</p> <p>1 1: Disables programming and erasure, and blank checking.</p>

## 2.27 Packages

As indicated in Table 2.72, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

**Table 2.72 Comparison of Packages**

Package Type	Renesas Code	
	RX65N	RX671
177-pin TFLGA	○	×
176-pin LFBGA	○	×
176-pin LFQFP	○	×
145-pin TFLGA	PTLG0145KA-A	PTLG0145 <b>J</b> C-A, PTLG0145 <b>K</b> B-A
100-pin TFLGA	PTLG0100JA-A	PTLG0100 <b>J</b> B-A
48-pin HWQFN	×	○

○: Package available (Renesas code omitted); ×: Package not available

### 3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exist on both groups with different specifications are indicated by **red text**. **Black text** indicates there is no differences in the item's specifications between groups.

#### 3.1 144-Pin LFQFP Package

Table 3.1 is a comparative listing of the pin functions of 144-pin LFQFP package products.

**Table 3.1 Comparative Listing of 144-Pin LFQFP Package Pin Functions**

144-Pin LFQFP	RX65N	RX671
1	AVSS0	AVSS0
2	P05/IRQ13/DA1	P05/IRQ13
3	AVCC1	AVCC1
4	P03/IRQ11/DA0	P03/IRQ11
5	AVSS1	AVSS1
6	P02/TMC11/SCK6/IRQ10/AN120	P02/TMC11/SCK6/IRQ10/AN109
7	P01/TMC10/RXD6/SMISO6/SSCL6/IRQ9/AN119	P01/TMC10/RXD6/SMISO6/SSCL6/IRQ9/AN110
8	P00/TMR10/TXD6/SMOSI6/SSDA6/IRQ8/AN118	P00/TMR10/TXD6/SMOSI6/SSDA6/IRQ8/AN111
9	PF5/IRQ4	PF5/IRQ4
10	EMLE	EMLE
11	PJ5/POE8#/CTS2#/RTS2#/SS2#	PJ5/POE8#/CTS2#/RTS2#/SS2#/IRQ13
12	VSS	VSS
13	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#	EXCIN/PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#/IRQ11
14	VCL	VCL
15	VBATT	VBATT
16	MD/FINED	MD/FINED
17	XCIN	XCIN
18	XCOUT	XCOUT
19	RES#	RES#
20	XTAL/P37	XTAL/P37
21	VSS	VSS
22	EXTAL/P36	EXTAL/P36
23	VCC	VCC
24	UPSEL/P35/NMI	UPSEL/P35/NMI
25	TRST#/P34/MTIOC0A/TMC13/PO12/POE10#/ET0_LINKSTA/SCK6/SCK0/IRQ4	TRST#/P34/MTIOC0A/TMC13/PO12/POE10#/SCK6/SCK0/IRQ4/TS0
26	P33/EDREQ1/MTIOC0D/TIOCD0/TMR13/PO11/POE4#/POE11#/RXD6/SMISO6/SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMR13/PO11/POE4#/POE11#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/IRQ3-DS/TS1
27	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCIC2/RTCOUT/POE0#/POE10#/TXD6/SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/POE0#/POE10#/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/USB0_VBUSEN/IRQ2-DS/TAMPI2
28	TMS/P31/MTIOC4D/TMC12/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS	TMS/P31/MTIOC4D/TMC12/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS/TAMPI1



144-Pin LQFP	RX65N	RX671
29	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS/ <a href="#">TAMPIO</a>
30	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A/ <a href="#">IRQ7/TS2</a>
31	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB-A/ <a href="#">IRQ6/TS3</a>
32	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/SDHI_CD*1/ <a href="#">HSYNC/ADTRG0#</a>	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/SDHI_CD/ <a href="#">IRQ5/ADTRG0#/TS4/CLKOUT</a>
33	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/SDHI_WP*1/ <a href="#">PIXCLK</a>	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/SDHI_WP/ <a href="#">IRQ12/TS5</a>
34	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/SS0#/SDHI_D1-C*1/ <a href="#">PIXD7</a>	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3/ <a href="#">SSIBCK0/SDHI_D1-C/IRQ3/TS6</a>
35	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB/SDHI_D0-C*1/ <a href="#">PIXD6</a>	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB/ <a href="#">AUDIO_CLK/SDHI_D0-C/IRQ15/TS7</a>
36	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/SCL1*1/USB0_EXICEN/SDHI_CLK-C*1/ <a href="#">PIXD5/IRQ9</a>	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/SCL1/USB0_EXICEN/ <a href="#">SSILRCK0/SDHI_CLK-C/IRQ9/TS8</a>
37	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/SDA1*1/USB0_ID/SDHI_CMD-C*1/ <a href="#">PIXD4/IRQ8</a>	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/SDA1/USB0_ID/ <a href="#">SSIRXD0/SDHI_CMDC/IRQ8/TS9</a>
38	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/SDHI_D3-C*1/ <a href="#">PIXD3/IRQ7/ADTRG1#</a>	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/ <a href="#">SSITXD0/SDHI_D3-C/IRQ7/ADTRG1#</a>
39	P87/MTIOC4C/TIOCA2/SMOSI10/SSDA10/TXD10/SDHI_D2-C*1/ <a href="#">PIXD2</a>	P87/MTIOC4C/TIOCA2/SMOSI10/SSDA10/TXD10/ <a href="#">SMOSI10/SSDA10/TXD010/SDHI_D2-C/IRQ15</a>
40	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOU/TXD1/SMOSI1/SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/USB0_VBUSEN/USB0_VBUS/USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOU/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#
41	P86/MTIOC4D/TIOCA0/SMISO10/SSCL10/RXD10/ <a href="#">PIXD1</a>	P86/MTIOC4D/TIOCA0/SMISO10/SSCL10/RXD10/ <a href="#">SMISO10/SSCL10/RXD010/IRQ14</a>
42	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SMISO1/SSCL1/SCK3/CRX1-DS/ <a href="#">PIXD0/IRQ5</a>	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/IRQ5/ <a href="#">TS10</a>
43	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4/ <a href="#">TS11</a>
44	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/ <a href="#">SDAHS0[FM+/HS]/IRQ3/ADTRG1#</a>
45	P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2	P12/ <a href="#">MTIC5U</a> /TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/ <a href="#">SCLHS0[FM+/HS]/IRQ2</a>
46	VCC_USB	VCC_USB
47	USB0_DM	<a href="#">PH2/TMRI0/USB0_DM/IRQ1</a>

144-Pin LQFP	RX65N	RX671
48	USB0_DP	PH1/TMO0/USB0_DP/IRQ0
49	VSS_USB	VSS_USB
50	P56/EDACK1/MTIOC3C/TIOCA1/SCK7*1	P56/EDACK1/MTIOC3C/TIOCA1/SCK7/ RSPCKC-B/IRQ6
51	TRDATA3/P55/D0[A0/D0]*1/WAIT#/ EDREQ0/MTIOC4D/TMO3/ET0_EXOUT/ TXD7*1/SMOSI7*1/SSDA7*1/CRX1/ IRQ10	TRDATA3/P55/D0[A0/D0]/WAIT#/EDREQ0/ MTIOC4D/TMO3/TXD7/SMOSI7/SSDA7/ CRX1/MISOC-B/IRQ10
52	TRDATA2/P54/ALE/D1[A1/D1]*1/EDACK0/ MTIOC4B/TMC11/ET0_LINKSTA/CTS2#/ RTS2#/SS2#/CTX1	TRDATA2/P54/ALE/D1[A1/D1]/EDACK0/ MTIOC4B/TMC11/CTS2#/RTS2#/SS2#/ CTX1/MOSIC-B/IRQ4
53	P53*2/BCLK	P53*2/BCLK/SSIRXD0/PMC0-DS/IRQ3/ TS12
54	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A/ IRQ2
55	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A/ IRQ1
56	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A/IRQ0
57	VSS	VSS
58	TRCLK/P83/EDACK1/MTIOC4C/ET0_CRS/ RMII0_CRS_DV/SCK10/SS10#/CTS10#	TRCLK/P83/EDACK1/MTIOC4C/SS10#/ CTS10#/SCK10/SS010#/CTS010#/SCK010/ IRQ3
59	VCC	VCC
60	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/ET0_COL/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/MMC_D7-A/IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/ SSITXD0/SMOSI010/SSDA010/TXD010/ MISO0-A/IRQ14
61	PC6/D2[A2/D2]*1/A22/CS1#/MTIOC3C/ MTCLKA/TMC12/PO30/TIC0/ET0_ETXD3/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/MMC_D6-A/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMC12/TIC0/PO30/RXD8/SMISO8/ SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ SSILRCK0/SMISO010/SSCL010/RXD010/ MOSI0-A/IRQ13/TS13
62	PC5/D3[A3/D3]*1/A21/CS2#/WAIT#/ MTIOC3B/MTCLKD/TMR12/PO29/ ET0_ETXD2/SCK8/SCK10/RSPCKA-A/ MMC_D5-A	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMR12/PO29/SCK8/SCK10/ RSPCKA-A/SSIBCK0/SCK010/RSPCK0-A/ IRQ5/TS14
63	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ ET0_ETXD1/RMII0_TXD1/SMOSI10/ SSDA10/TXD10/MMC_D4-A	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ SMOSI10/SSDA10/TXD10/SMOSI010/ SSDA010/TXD010/IRQ2
64	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ ET0_ETXD0/RMII0_TXD0/SMISO10/ SSCL10/RXD10/QIO3-A/SDHI_CD/ MMC_D3-A	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ SMISO10/SSCL10/RXD10/SMISO010/ SSCL010/RXD010/SDHI_CD/QIO3-A/IRQ9
65	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ ET0_TX_EN/RMII0_TXD_EN/SCK10/ RTS10#/QIO2-A/SDHI_WP/MMC_D2-A	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10/RTS10#/SCK010/RTS010#/DE010/ SDHI_WP/QIO2-A/IRQ8
66	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMC11/ PO25/POE0#/ET0_TX_CLK/SCK5/CTS8#/ RTS8#/SS8#/SS10#/CTS10#/RTS10#/ SSLA0-A/QMI-A/QIO1-A/SDHI_D1-A/ SDSI_D1-A/MMC_D1-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMC11/ PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/ SS10#/CTS10#/RTS10#/SSLA0-A/ AUDIO_CLK/SS010#/CTS010#/RTS010#/ DE010/SSL00-A/SDHI_D1-A/QIO1-A/IRQ12/ TSCAP

144-Pin LQFP	RX65N	RX671
67	PC3/A19/MTIOC4D/TCLKB/PO24/ ET0_TX_ER/TXD5/SMOSI5/SSDA5/QMO-A/ QIO0-A/SDHI_D0-A/SDSI_D0-A/MMC_D0-A	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/ SMOSI5/SSDA5/PMC0-DS/SDHI_D0-A/ QIO0-A/IRQ11
68	TRDATA7/P77/CS7#/PO23/ET0_RX_ER/ RMII0_RX_ER/SMOSI11/SSDA11/TXD11/ QSPCLK-A/SDHI_CLK-A/SDSI_CLK-A/ MMC_CLK-A	TRDATA7/P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/SMOSI011/SSDA011/ TXD011/SDHI_CLK-A/QSPCLK-A/IRQ7
69	TRDATA6/P76/CS6#/PO22/ET0_RX_CLK/ REF50CK0/SMISO11/SSCL11/RXD11/ QSSL-A/SDHI_CMD-A/SDSI_CMD-A/ MMC_CMD-A	TRDATA6/P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/SMISO011/SSCL011/ RXD011/SDHI_CMD-A/QSSL-A/IRQ14
70	PC2/A18/MTIOC4B/TCLKA/PO21/ ET0_RX_DV/RXD5/SMISO5/SSCL5/ SSLA3-A/SDHI_D3-A/SDSI_D3-A/ MMC_CD-A	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/ SMISO5/SSCL5/SSLA3-A/TXDB011/ SSL03-A/SDHI_D3-A/IRQ10
71	TRSYNC1/P75/CS5#/PO20/ET0_ERXD0/ RMII0_RXD0/SCK11/RTS11#/SDHI_D2-A/ SDSI_D2-A/MMC_RES#-A	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/ SCK011/RTS011#/DE011/SDHI_D2-A/ IRQ13
72	TRDATA5/P74/A20/CS4#/PO19/ ET0_ERXD1/RMII0_RXD1/SS11#/CTS11#	TRDATA5/P74/A20/CS4#/PO19/SS11#/ CTS11#/SS011#/CTS011#/IRQ12
73	PC1/A17/MTIOC3A/TCLKD/PO18/ ET0_ERXD2/SCK5/SSLA2-A/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/TXD011/SMOSI011/ SSDA011/TXDA011/SSL02-A/IRQ12/TS15
74	VCC	VCC
75	PC0/A16/MTIOC3C/TCLKC/PO17/ ET0_ERXD3/CTS5#/RTS5#/SS5#/ SSLA1-A/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/RXD011/ SMISO011/SSCL011/SSL01-A/IRQ14/TS16
76	VSS	VSS
77	TRDATA4/P73/CS3#/PO16/ET0_WOL	TRDATA4/P73/CS3#/PO16/IRQ8
78	PB7/A15/MTIOC3B/TIOCB5/PO31/ ET0_CRS/RMII0_CRS_DV/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/TXD11/ SDSI_D1-B	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ SMOSI011/SSDA011/TXD011/IRQ15
79	PB6/A14/MTIOC3D/TIOCA5/PO30/ ET0_ETXD1/RMII0_TXD1/RXD9/SMISO9/ SSCL9/SMISO11/SSCL11/RXD11/ SDSI_D0-B	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ SMISO011/SSCL011/RXD011/IRQ6
80	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/ET0_ETXD0/ RMII0_TXD0/SCK9/SCK11/SDSI_CLK-B/ LCD_CLK-B*1	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/SCK11/SCK011/ IRQ13
81	PB4/A12/TIOCA4/PO28/ET0_TX_EN/ RMII0_TXD_EN/CTS9#/RTS9#/SS9#/ SS11#/CTS11#/RTS11#/SDSI_CMD-B/ LCD_TCON0-B*1	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/ SS9#/SS11#/CTS11#/RTS11#/ SS011#/CTS011#/RTS011#/DE011/IRQ4
82	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/ET0_RX_ER/ RMII0_RX_ER/SCK4/SCK6/SDSI_D3-B/ LCD_TCON1-B*1	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ PMC0-DS/IRQ3
83	PB2/A10/TIOCC3/TCLKC/PO26/ ET0_RX_CLK/REF50CK0/CTS4#/RTS4#/ SS4#/CTS6#/RTS6#/SS6#/SDSI_D2-B/ LCD_TCON2-B*1	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS 4#/CTS6#/RTS6#/SS4#/SS6#/IRQ2

144-Pin LFQFP	RX65N	RX671
84	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/ET0_ERXD0/RMII0_RXD0/TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/LCD_TCON3-B*1/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/SSDA4/SSDA6/IRQ4-DS
85	P72/A19/CS2#/ET0_MDC	P72/A19/CS2#/IRQ10
86	P71/A18/CS1#/ET0_MDIO	P71/A18/CS1#/IRQ1
87	PB0/A8/MTIC5W/TIOCA3/PO24/ET0_ERXD1/RMII0_RXD1/RXD4/SMISO4/SSCL4/RXD6/SMISO6/SSCL6/LCD_DATA0-B*1/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/RXD6/SMISO4/SMISO6/SSCL4/SSCL6/IRQ12
88	PA7/A7/TIOCB2/PO23/ET0_WOL/MISOA-B/LCD_DATA1-B*1	PA7/A7/TIOCB2/PO23/MISOA-B/MISO0-B/IRQ7
89	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#/ET0_EXOUT/CTS5#/RTS5#/SS5#/MOSIA-B/LCD_DATA2-B*1	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#/CTS5#/RTS5#/SS5#/MOSIA-B/MOSI0-B/CTS12#/RTS12#/SS12#/IRQ14
90	PA5/A5/MTIOC6B/TIOCB1/PO21/ET0_LINKSTA/RSPCKA-B/LCD_DATA3-B*1	PA5/A5/MTIOC6B/TIOCB1/PO21/RSPCKA-B/RSPCK0-B/IRQ5
91	VCC	VCC
92	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/ET0_MDC/TXD5/SMOSI5/SSDA5/SSLA0-B/LCD_DATA4-B*1/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/SSL00-B/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ5-DS
93	VSS	VSS
94	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/ET0_MDIO/RXD5/SMISO5/SSCL5/LCD_DATA5-B*1/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/IRQ6-DS
95	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B*1	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/SSCL5/SSLA3-B/SSL03-B/RXD12/SMISO12/SSCL12/RDX12/SDHI_WP/IRQ10
96	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17/ET0_WOL/SCK5/SSLA2-B/LCD_DATA7-B*1/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17/SCK5/SSLA2-B/SSL02-B/SCK12/SDHI_CD/IRQ11
97	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/PO16/CACREF/ET0_TX_EN/RMII0_TXD_EN/SSLA1-B/LCD_DATA8-B*1	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/CACREF/PO16/SSLA1-B/SSL01-B/IRQ0
98	P67/DQM1/CS7#/MTIOC7C/IRQ15	P67/CS7#/DQM1/MTIOC7C/IRQ15
99	P66/DQM0/CS6#/MTIOC7D	P66/CS6#/DQM0/MTIOC7D/IRQ14
100	P65/CKE/CS5#	P65/CS5#/CKE/IRQ13
101	PE7/D15[A15/D15]/D7[A7/D7]*1/MTIOC6A/TOC1/MISOB-B/SDHI_WP/MMC_RES#-B/LCD_DATA9-B*1/IRQ7/AN105	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/TOC1/MISOB-B/SDHI_WP/SDHI_D1-B/QIO1-B/IRQ7
102	PE6/D14[A14/D14]/D6[A6/D6]*1/MTIOC6C/TIC1/MOSIB-B/SDHI_CD/MMC_CD-B/LCD_DATA10-B*1/IRQ6/AN104	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/TIC1/MOSIB-B/SDHI_CD/SDHI_D0-B/QIO0-B/IRQ6
103	VCC	VCC
104	P70/SDCLK	P70/SDCLK/IRQ0
105	VSS	VSS
106	PE5/D13[A13/D13]/D5[A5/D5]*1/MTIOC4C/MTIOC2B/ET0_RX_CLK/REF50CK0/RSPCKB-B/LCD_DATA11-B*1/IRQ5/AN103	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/MTIOC2B/RSPCKB-B/IRQ5

144-Pin LQFP	RX65N	RX671
107	PE4/D12[A12/D12]/D4[A4/D4]*1/MTIOC4D/MTIOC1A/PO28/ <a href="#">ET0_ERXD2</a> /SSLB0-B/ <a href="#">LCD_DATA12-B</a> *1/ <a href="#">AN102</a>	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/MTIOC1A/PO28/SSLB0-B/ <a href="#">IRQ12</a>
108	PE3/D11[A11/D11]/D3[A3/D3]*1/MTIOC4B/PO26/TOC3/POE8#/ <a href="#">ET0_ERXD3</a> /CTS12#/ <a href="#">RTS12</a> #/ <a href="#">SS12</a> #/ <a href="#">MMC_D7-B</a> / <a href="#">LCD_DATA13-B</a> *1/ <a href="#">AN101</a>	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/PO26/POE8#/TOC3/CTS12#/ <a href="#">RTS12</a> #/ <a href="#">SS12</a> #/ <a href="#">IRQ11</a>
109	PE2/D10[A10/D10]/D2[A2/D2]*1/MTIOC4A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/ <a href="#">MMC_D6-B</a> / <a href="#">LCD_DATA14-B</a> *1/ <a href="#">IRQ7-DS</a> / <a href="#">AN100</a>	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/ <a href="#">IRQ7-DS</a>
110	PE1/D9[A9/D9]/D1[A1/D1]*1/MTIOC4C/MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/ <a href="#">MMC_D5-B</a> / <a href="#">LCD_DATA15-B</a> *1/ <a href="#">ANEX1</a>	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/ <a href="#">IRQ9</a> / <a href="#">ANEX1</a>
111	PE0/D8[A8/D8]/D0[A0/D0]*1/MTIOC3D/SCK12/SSLB1-B/ <a href="#">MMC_D4-B</a> / <a href="#">LCD_DATA16-B</a> *1/ <a href="#">ANEX0</a>	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/SCK12/SSLB1-B/ <a href="#">IRQ8</a> / <a href="#">ANEX0</a>
112	P64/WE#/D3[A3/D3]*1/CS4#	P64/CS4#/WE#/D3[A3/D3]/ <a href="#">IRQ4</a>
113	P63/CAS#/D2[A2/D2]*1/CS3#	P63/CS3#/CAS#/D2[A2/D2]/ <a href="#">IRQ3</a>
114	P62/RAS#/D1[A1/D1]*1/CS2#	P62/CS2#/RAS#/D1[A1/D1]/ <a href="#">IRQ2</a>
115	P61/SDCS#/D0[A0/D0]*1/CS1#	P61/CS1#/SDCS#/D0[A0/D0]/ <a href="#">IRQ1</a>
116	VSS	VSS
117	P60/CS0#	P60/CS0#/ <a href="#">IRQ0</a>
118	VCC	VCC
119	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ <a href="#">QMI-B</a> / <a href="#">QIO1-B</a> / <a href="#">SDHI_D1-B</a> / <a href="#">MMC_D1-B</a> / <a href="#">LCD_DATA17-B</a> *1/ <a href="#">IRQ7</a> / <a href="#">AN107</a>	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ <a href="#">SDHI_D1-B</a> / <a href="#">QIO1-B</a> / <a href="#">IRQ7</a> / <a href="#">AN100</a>
120	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2-A/ <a href="#">QMO-B</a> / <a href="#">QIO0-B</a> / <a href="#">SDHI_D0-B</a> / <a href="#">MMC_D0-B</a> / <a href="#">LCD_DATA18-B</a> *1/ <a href="#">IRQ6</a> / <a href="#">AN106</a>	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2-A/ <a href="#">SDHI_D0-B</a> / <a href="#">QIO0-B</a> / <a href="#">IRQ6</a> / <a href="#">AN101</a>
121	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1-A/ <a href="#">QSPCLK-B</a> / <a href="#">SDHI_CLK-B</a> / <a href="#">MMC_CLK-B</a> / <a href="#">LCD_DATA19-B</a> *1/ <a href="#">IRQ5</a> / <a href="#">AN113</a>	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1-A/ <a href="#">SDHI_CLK-B</a> / <a href="#">QSPCLK-B</a> / <a href="#">IRQ5</a> / <a href="#">AN102</a>
122	PD4/D4[A4/D4]/MTIOC8B/POE11#/ <a href="#">SSLC0-A</a> / <a href="#">QSSL-B</a> / <a href="#">SDHI_CMD-B</a> / <a href="#">MMC_CMD-B</a> / <a href="#">LCD_DATA20-B</a> *1/ <a href="#">IRQ4</a> / <a href="#">AN112</a>	PD4/D4[A4/D4]/MTIOC8B/POE11#/ <a href="#">SSLC0-A</a> / <a href="#">SDHI_CMD-B</a> / <a href="#">QSSL-B</a> / <a href="#">IRQ4</a> / <a href="#">AN103</a>
123	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ <a href="#">RSPCKC-A</a> / <a href="#">QIO3-B</a> / <a href="#">SDHI_D3-B</a> / <a href="#">MMC_D3-B</a> / <a href="#">LCD_DATA21-B</a> *1/ <a href="#">IRQ3</a> / <a href="#">AN111</a>	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/ <a href="#">RSPCKC-A</a> / <a href="#">SDHI_D3-B</a> / <a href="#">QIO3-B</a> / <a href="#">IRQ3</a> / <a href="#">AN104</a>
124	PD2/D2[A2/D2]/MTIOC4D/TIC2/MISOC-A/ <a href="#">CRX0</a> / <a href="#">QIO2-B</a> / <a href="#">SDHI_D2-B</a> / <a href="#">MMC_D2-B</a> / <a href="#">LCD_DATA22-B</a> *1/ <a href="#">IRQ2</a> / <a href="#">AN110</a>	PD2/D2[A2/D2]/MTIOC4D/TIC2/ <a href="#">CRX0</a> /MISOC-A/ <a href="#">SDHI_D2-B</a> / <a href="#">QIO2-B</a> / <a href="#">IRQ2</a> / <a href="#">AN105</a>
125	PD1/D1[A1/D1]/MTIOC4B/POE0#/MOSIC-A/ <a href="#">CTX0</a> / <a href="#">LCD_DATA23-B</a> *1/ <a href="#">IRQ1</a> / <a href="#">AN109</a>	PD1/D1[A1/D1]/MTIOC4B/POE0#/ <a href="#">CTX0</a> /MOSIC-A/ <a href="#">IRQ1</a> / <a href="#">AN106</a>
126	PD0/D0[A0/D0]/POE4#/ <a href="#">LCD_EXTCLK-B</a> *1/ <a href="#">IRQ0</a> / <a href="#">AN108</a>	PD0/D0[A0/D0]/POE4#/ <a href="#">IRQ0</a> / <a href="#">AN107</a>
127	P93/A19/POE0#/CTS7#/ <a href="#">RTS7</a> #/ <a href="#">SS7</a> #/ <a href="#">AN117</a>	P93/A19/POE0#/CTS7#/ <a href="#">RTS7</a> #/ <a href="#">SS7</a> #/ <a href="#">IRQ11</a>
128	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ <a href="#">AN116</a>	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ <a href="#">IRQ10</a>

144-Pin LFQFP	RX65N	RX671
129	P91/A17/SCK7/AN115	P91/A17/SCK7/IRQ9
130	VSS	VSS
131	P90/A16/TXD7/SMOSI7/SSDA7/AN114	P90/A16/TXD7/SMOSI7/SSDA7/IRQ0/ AN108
132	VCC	VCC
133	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
134	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
135	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
136	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
137	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
138	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
139	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
140	VREFL0	VREFL0
141	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
142	VREFH0	VREFH0
143	AVCC0	AVCC0
144	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#

- Notes: 1. Valid only on products with a code flash memory capacity of 2 MB or 1.5 MB.  
 2. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.

### 3.2 100-Pin TFLGA Package

Table 3.2 is a comparative listing of the pin functions of 100-pin TFLGA package products.

**Table 3.2 Comparative Listing of 100-Pin TFLGA Package Pin Functions**

100-Pin TFLGA	RX65N	RX671
A1	P05/IRQ13/DA1	P05/IRQ13
A2	AVCC1	AVCC1
A3	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
A4	VREFL0	VREFL0
A5	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
A6	PD0/D0[A0/D0]/POE4#/LCD_EXTCLK-B*1/ IRQ0/AN108	PD0/D0[A0/D0]/POE4#/IRQ0/AN107
A7	PD4/D4[A4/D4]/MTIIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B*1/IRQ4/ AN112	PD4/D4[A4/D4]/MTIIOC8B/POE11#/ SSLC0-A/SDHI_CMD-B/QSSL-B/IRQ4/ AN103
A8	PE0/D8[A8/D8]/D0[A0/D0]*1/ MTIIOC3D/SCK12/SSLB1-B/MMC_D4-B/ LCD_DATA16-B*1/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIIOC3D/SCK12/ SSLB1-B/IRQ8/ANEX0
A9	PE1/D9[A9/D9]/D1[A1/D1]*1/ MTIIOC4C/MTIIOC3B/PO18/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/LCD_DATA15-B*1/ ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIIOC4C/ MTIIOC3B/PO18/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/IRQ9/ANEX1
A10	PE2/D10[A10/D10]/D2[A2/D2]*1/MTIIOC4A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B*1/IRQ7-DS/AN100	PE2/D10[A10/D10]/D2[A2/D2]/MTIIOC4A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/IRQ7-DS
B1	EMLE	EMLE
B2	AVSS0	AVSS0
B3	AVCC0	AVCC0
B4	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
B5	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
B6	PD1/D1[A1/D1]/MTIIOC4B/POE0#/ MOSIC-A/CTX0/LCD_DATA23-B*1/IRQ1/ AN109	PD1/D1[A1/D1]/MTIIOC4B/POE0#/CTX0/ MOSIC-A/IRQ1/AN106
B7	PD3/D3[A3/D3]/MTIIOC8D/TOC2/POE8#/ RSPCKC-A/QIO3-B/SDHI_D3-B/MMC_D3-B/ LCD_DATA21-B*1/IRQ3/AN111	PD3/D3[A3/D3]/MTIIOC8D/POE8#/TOC2/ RSPCKC-A/SDHI_D3-B/QIO3-B/IRQ3/ AN104
B8	PD6/D6[A6/D6]/MTIC5V/MTIIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B*1/IRQ6/ AN106	PD6/D6[A6/D6]/MTIC5V/MTIIOC8A/POE4#/ SSLC2-A/SDHI_D0-B/QIO0-B/IRQ6/AN101
B9	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B*1/IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ SDHI_D1-B/QIO1-B/IRQ7/AN100
B10	PE3/D11[A11/D11]/D3[A3/D3]*1/MTIIOC4B/ PO26/TOC3/POE8#/ETO_ERXD3/CTS12#/ RTS12#/SS12#/MMC_D7-B/ LCD_DATA13-B*1/AN101	PE3/D11[A11/D11]/D3[A3/D3]/MTIIOC4B/ PO26/POE8#/TOC3/CTS12#/RTS12#/ SS12#/IRQ11
C1	VCL	VCL
C2	AVSS1	AVSS1

100-Pin TFLGA	RX65N	RX671
C3	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/ CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#	EXCIN/PJ3/EDACK1/MTIOC3C/CTS6#/ RTS6#/CTS0#/RTS0#/SS6#/SS0#/IRQ11
C4	VREFH0	VREFH0
C5	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
C6	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
C7	PD2/D2[A2/D2]/MTIOC4D/TIC2/MISOC-A/ CRX0/QIO2-B/SDHI_D2-B/MMC_D2-B/ LCD_DATA22-B*1/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/ MISOC-A/SDHI_D2-B/QIO2-B/IRQ2/AN105
C8	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/ SSLC1-A/QSPCLK-B/SDHI_CLK-B/ MMC_CLK-B/LCD_DATA19-B*1/IRQ5/ AN113	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/ SSLC1-A/SDHI_CLK-B/QSPCLK-B/IRQ5/ AN102
C9	PE5/D13[A13/D13]/D5[A5/D5]*1/MTIOC4C/ MTIOC2B/ET0_RX_CLK/REF50CK0/ RSPCKB-B/LCD_DATA11-B*1/IRQ5/AN103	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/RSPCKB-B/IRQ5
C10	PE4/D12[A12/D12]/D4[A4/D4]*1/MTIOC4D/ MTIOC1A/PO28/ET0_ERXD2/SSLB0-B/ LCD_DATA12-B*1/AN102	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/SSLB0-B/IRQ12
D1	XCIN	XCIN
D2	XCOU	XCOU
D3	MD/FINED	MD/FINED
D4	VBATT	VBATT
D5	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
D6	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
D7	PE6/D14[A14/D14]/D6[A6/D6]*1/MTIOC6C/ TIC1/MOSIB-B/SDHI_CD/MMC_CD-B/ LCD_DATA10-B*1/IRQ6/AN104	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/MOSIB-B/SDHI_CD/SDHI_D0-B/ QIO0-B/IRQ6
D8	PE7/D15[A15/D15]/D7[A7/D7]*1/MTIOC6A/ TOC1/MISOB-B/SDHI_WP/MMC_RES#-B/ LCD_DATA9-B*1/IRQ7/AN105	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/MISOB-B/SDHI_WP/SDHI_D1-B/ QIO1-B/IRQ7
D9	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/ET0_WOL/SCK5/SSLA2-B/ LCD_DATA7-B*1/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/SCK5/SSLA2-B/SSL02-B/ SCK12/SDHI_CD/IRQ11
D10	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/ PO16/CACREF/ET0_TX_EN/ RMII0_TXD_EN/SSLA1-B/LCD_DATA8-B*1	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/ CACREF/PO16/SSLA1-B/SSL01-B/IRQ0
E1	XTAL/P37	XTAL/P37
E2	VSS	VSS
E3	RES#	RES#
E4	TRST#/P34/MTIOC0A/TMC13/PO12/ POE10#/ET0_LINKSTA/SCK6/SCK0/IRQ4	TRST#/P34/MTIOC0A/TMC13/PO12/ POE10#/SCK6/SCK0/IRQ4/TS0
E5	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
E6	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/LCD_DATA6-B*1	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/SSL03-B/RXD12/ SMISO12/SSCL12/RDX12/SDHI_WP/ IRQ10
E7	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMC13/ PO22/POE10#/ET0_EXOUT/CTS5#/RTS5#/ SS5#/MOSIA-B/LCD_DATA2-B*1	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMC13/ PO22/POE10#/CTS5#/RTS5#/SS5#/ MOSIA-B/MOSI0-B/CTS12#/RTS12#/SS12#/ IRQ14



100-Pin TFLGA	RX65N	RX671
E8	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/ET0_MDC/TXD5/SMOSI5/SSDA5/ SSLA0-B/LCD_DATA4-B*1/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ SSL00-B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/IRQ5-DS
E9	PA5/A5/MTIOC6B/TIOCB1/PO21/ ET0_LINKSTA/RSPCKA-B/ LCD_DATA3-B*1	PA5/A5/MTIOC6B/TIOCB1/PO21/ RSPCKA-B/RSPCK0-B/IRQ5
E10	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/ET0_MDIO/RXD5/SMISO5/ SSCL5/LCD_DATA5-B*1/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ IRQ6-DS
F1	EXTAL/P36	EXTAL/P36
F2	VCC	VCC
F3	UPSEL/P35/NMI	UPSEL/P35/NMI
F4	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOU/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOU/RTCIC2/POE0#/POE10#/TXD6/ TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/IRQ2-DS/TAMPI2
F5	P12/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/SCLHS0[FM+]/HS/IRQ2
F6	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/ET0_RX_ER/ RMII0_RX_ER/SCK6/SDSI_D3-B/ LCD_TCON1-B*1	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK6/ PMC0-DS/IRQ3
F7	PB2/A10/TIOCC3/TCLKC/PO26/ ET0_RX_CLK/REF50CK0/CTS6#/RTS6#/ SS6#/SDSI_D2-B/LCD_TCON2-B*1	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/ RTS6#/SS6#/IRQ2
F8	PB0/A8/MTIC5W/TIOCA3/PO24/ ET0_ERXD1/RMII0_RXD1/RXD6/SMISO6/ SSCL6/LCD_DATA0-B*1/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/ SMISO6/SSCL6/IRQ12
F9	PA7/A7/TIOCB2/PO23/ET0_WOL/ MISOA-B/LCD_DATA1-B*1	PA7/A7/TIOCB2/PO23/MISOA-B/ MISO0-B/IRQ7
F10	VSS	VSS
G1	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/ IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/RXD0/ SMISO6/SMISO0/SSCL6/SSCL0/CRX0/ IRQ3-DS/TS1
G2	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS/ TAMPI1
G3	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS/TAMPI0
G4	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/ SCK1/RSPCKB-A	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/ SCK1/RSPCKB-A/IRQ7/TS2
G5	P53*2/BCLK	P53*2/BCLK/SSIRXD0/PMC0-DS/IRQ3/ TS12
G6	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A/ IRQ2
G7	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/ET0_ETXD0/ RMII0_TXD0/SCK9/SCK11/SDSI_CLK-B/ LCD_CLK-B*1	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/SCK11/SCK011/ IRQ13

100-Pin TFLGA	RX65N	RX671
G8	PB4/A12/TIOCA4/PO28/ET0_TX_EN/ RMII0_TXD_EN/CTS9#/RTS9#/SS9#/ SS11#/CTS11#/RTS11#/SDSI_CMD-B/ LCD_TCON0-B*1	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/ SS9#/SS11#/CTS11#/RTS11#/SS011#/ CTS011#/RTS011#/DE011/IRQ4
G9	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCIO/PO25/ET0_ERXD0/RMII0_RXD0/ TXD6/SMOSI6/SSDA6/LCD_TCON3-B*1/ IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCIO/PO25/TXD6/SMOSI6/SSDA6/ IRQ4-DS
G10	VCC	VCC
H1	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ MOSIB-A/IRQ6/TS3
H2	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ ADTRG0#	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SDHI_CD/IRQ5/ADTRG0#/TS4/CLKOUT
H3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOU/TXD1/SMOSI1/ SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOU/TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/SCL2-DS/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#
H4	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCIO2/PO13/RXD1/SMISO1/SSCL1/SCK3/ CRX1-DS/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCIO2/PO13/RXD1/SCK3/SMISO1/SSCL1/ CRX1-DS/IRQ5/TS10
H5	P55/D0[A0/D0]*1/WAIT#/EDREQ0/ MTIOC4D/TMO3/ET0_EXOUT/CRX1/IRQ10	P55/D0[A0/D0]/WAIT#/EDREQ0/MTIOC4D/ TMO3/CRX1/MISOC-B/IRQ10
H6	P54/ALE/D1[A1/D1]*1/EDACK0/MTIOC4B/ TMCIO1/ET0_LINKSTA/CTS2#/RTS2#/SS2#/ CTX1	P54/ALE/D1[A1/D1]/EDACK0/MTIOC4B/ TMCIO1/CTS2#/RTS2#/SS2#/CTX1/ MOSIC-B/IRQ4
H7	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/ET0_COL/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/ SSITXD0/SMOSI010/SSDA010/TXD010/ MISO0-A/IRQ14
H8	PC6/D2[A2/D2]*1/A22/CS1#/MTIOC3C/ MTCLKA/TMCIO2/PO30/TIC0/ET0_ETXD3/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCIO2/PO30/RXD8/SMISO8/ SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ SSILRCK0/SMISO010/SSCL010/RXD010/ MOSI0-A/IRQ13/TS13
H9	PB6/A14/MTIOC3D/TIOCA5/PO30/ ET0_ETXD1/RMII0_TXD1/RXD9/SMISO9/ SSCL9/SMISO11/SSCL11/RXD11/ SDSI_D0-B	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ SMISO011/SSCL011/RXD011/IRQ6
H10	PB7/A15/MTIOC3B/TIOCB5/PO31/ ET0_CRS/RMII0_CRS_DV/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/TXD11/ SDSI_D1-B	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ SMOSI011/SSDA011/TXD011/IRQ15
J1	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SDHI_WP/IRQ12/TS5
J2	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCIO/ PO1/RXD0/SMISO0/SSCL0/SCL1*1/ USB0_EXICEN/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCIO/ PO1/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ IRQ9/TS8

100-Pin TFLGA	RX65N	RX671
J3	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/SSITXD0/SDHI_D3-C/IRQ7/ADTRG1#
J4	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/SDAHS0[FM+/HS]/IRQ3/ADTRG1#
J5	VSS_USB	VSS_USB
J6	VCC_USB	VCC_USB
J7	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A/IRQ0
J8	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMC11/PO25/POE0#/ET0_TX_CLK/SCK5/CTS8#/RTS8#/SS8#/SS10#/CTS10#/RTS10#/SSLA0-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMC11/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/AUDIO_CLK/SS010#/CTS010#/RTS010#/DE010/SSL00-A/SDHI_D1-A/QIO1-A/IRQ12/TSCAP
J9	PC0/A16/MTIOC3C/TCLKC/PO17/ET0_ERXD3/CTS5#/RTS5#/SS5#/SSLA1-A/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/RXD011/SMISO011/SSCL011/SSL01-A/IRQ14/TS16
J10	PC1/A17/MTIOC3A/TCLKD/PO18/ET0_ERXD2/SCK5/SSLA2-A/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2-A/TXD011/SMOSI011/SSDA011/TXDA011/SSL02-A/IRQ12/TS15
K1	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/SS0#	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3/SSIBCK0/SDHI_D1-C/IRQ3/TS6
K2	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB/AUDIO_CLK/SDHI_D0-C/IRQ15/TS7
K3	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/SDA1*1/USB0_ID/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/SDHI_CMDC/IRQ8/TS9
K4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4/TS11
K5	USB0_DM	PH2/TMRI0/USB0_DM/IRQ1
K6	USB0_DP	PH1/TMO0/USB0_DP/IRQ0
K7	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A/IRQ1
K8	PC5/D3[A3/D3]*1/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/ET0_ETXD2/SCK8/SCK10/RSPCKA-A	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/SCK8/SCK10/RSPCKA-A/SSIBCK0/SCK010/RSPCK0-A/IRQ5/TS14
K9	PC3/A19/MTIOC4D/TCLKB/PO24/ET0_TX_ER/TXD5/SMOSI5/SSDA5	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/PMC0-DS/SDHI_D0-A/QIO0-A/IRQ11
K10	PC2/A18/MTIOC4B/TCLKA/PO21/ET0_RX_DV/RXD5/SMISO5/SSCL5/SLA3-A	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3-A/TXDB011/SSL03-A/SDHI_D3-A/IRQ10

- Notes: 1. Valid only on products with a code flash memory capacity of 2 MB or 1.5 MB.  
 2. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.

### 3.3 100-Pin LFQFP Package

Table 3.3 is a comparative listing of the pin functions of 100-pin LFQFP package products.

**Table 3.3 Comparative Listing of 100-Pin LFQFP Package Pin Functions**

100-Pin LFQFP	RX65N	RX671
1	AVCC1	AVCC1
2	EMLE	EMLE
3	AVSS1	AVSS1
4	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/ CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#	EXCIN/PJ3/EDACK1/MTIOC3C/CTS6#/ RTS6#/CTS0#/RTS0#/SS6#/SS0#/IRQ11
5	VCL	VCL
6	VBATT	VBATT
7	MD/FINED	MD/FINED
8	XCIN	XCIN
9	XCOU	XCOU
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	UPSEL/P35/NMI	UPSEL/P35/NMI
16	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/ET0_LINKSTA/SCK6/SCK0/IRQ4	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/IRQ4/TS0
17	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/ IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/RXD0/ SMISO6/SMISO0/SSCL6/SSCL0/CRX0/ IRQ3-DS/TS1
18	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/POE0#/POE10#/TXD6/ TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/IRQ2-DS/TAMPI2
19	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS/ TAMPI1
20	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS/TAMPI0
21	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/ SCK1/RSPCKB-A	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A/IRQ7/TS2
22	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ MOSIB-A/IRQ6/TS3
23	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ ADTRG0#	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SDHI_CD/IRQ5/ADTRG0#/TS4/CLKOUT
24	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SDHI_WP/IRQ12/TS5
25	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/ SS0#	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/ SSDA3/SSIBCK0/SDHI_D1-C/IRQ3/TS6

100-Pin LQFP	RX65N	RX671
26	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB/AUDIO_CLK/SDHI_D0-C/IRQ15/TS7
27	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/SCL1*1/USB0_EXICEN/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/SCL1/USB0_EXICEN/SSILRCK0/SDHI_CLK-C/IRQ9/TS8
28	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/SDA1*1/USB0_ID/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/SDHI_CMDC/IRQ8/TS9
29	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/SSITXD0/SDHI_D3-C/IRQ7/ADTRG1#
30	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOU/TXD1/SMOSI1/SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/USB0_VBUSEN/USB0_VBUS/USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOU/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#
31	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SMISO1/SSCL1/SCK3/CRX1-DS/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/IRQ5/TS10
32	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4/TS11
33	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/SDAHS0[FM+/HS]/IRQ3/ADTRG1#
34	P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/SCLHS0[FM+/HS]/IRQ2
35	VCC_USB	VCC_USB
36	USB0_DM	PH2/TMRI0/USB0_DM/IRQ1
37	USB0_DP	PH1/TMO0/USB0_DP/IRQ0
38	VSS_USB	VSS_USB
39	P55/D0[A0/D0]*1/WAIT#/EDREQ0/MTIOC4D/TMO3/ET0_EXOUT/CRX1/IRQ10	P55/D0[A0/D0]/WAIT#/EDREQ0/MTIOC4D/TMO3/CRX1/MISOC-B/IRQ10
40	P54/ALE/D1[A1/D1]*1/EDACK0/MTIOC4B/TMCI1/ET0_LINKSTA/CTS2#/RTS2#/SS2#/CTX1	P54/D1[A1/D1]/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1/MOSIC-B/IRQ4
41	P53*2/BCLK	P53*2/BCLK/SSIRXD0/PMC0-DS/IRQ3/TS12
42	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A/IRQ2
43	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A/IRQ1
44	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A/IRQ0
45	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/PO31/TOC0/CACREF/ET0_COL/TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/SSITXD0/SMOSI010/SSDA010/TXD010/MISO0-A/IRQ14

100-Pin LQFP	RX65N	RX671
46	PC6/D2[A2/D2]*1/A22/CS1#/MTIOC3C/MTCLKA/TMC12/PO30/TIC0/ET0_ETXD3/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/MTCLKA/TMC12/TIC0/PO30/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/SSILRCK0/SMISO010/SSCL010/RXD010/MOSI0-A/IRQ13/TS13
47	PC5/D3[A3/D3]*1/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMR12/PO29/ET0_ETXD2/SCK8/SCK10/RSPCKA-A	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMR12/PO29/SCK8/SCK10/RSPCKA-A/SSIBCK0/SCK010/RSPCK0-A/IRQ5/TS14
48	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMC11/PO25/POE0#/ET0_TX_CLK/SCK5/CTS8#/RTS8#/SS8#/SS10#/CTS10#/RTS10#/SSLA0-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMC11/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/AUDIO_CLK/SS010#/CTS010#/RTS010#/DE010/SSL00-A/SDHI_D1-A/QIO1-A/IRQ12/TSCAP
49	PC3/A19/MTIOC4D/TCLKB/PO24/ET0_TX_ER/TXD5/SMOSI5/SSDA5	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/PMC0-DS/SDHI_D0-A/QIO0-A/IRQ11
50	PC2/A18/MTIOC4B/TCLKA/PO21/ET0_RX_DV/RXD5/SMISO5/SSCL5/SSLA3-A	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3-A/TXDB011/SSL03-A/SDHI_D3-A/IRQ10
51	PC1/A17/MTIOC3A/TCLKD/PO18/ET0_ERXD2/SCK5/SSLA2-A/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2-A/TXD011/SMOSI011/SSDA011/TXDA011/SSL02-A/IRQ12/TS15
52	PC0/A16/MTIOC3C/TCLKC/PO17/ET0_ERXD3/CTS5#/RTS5#/SS5#/SSLA1-A/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/RXD011/SMISO011/SSCL011/SSL01-A/IRQ14/TS16
53	PB7/A15/MTIOC3B/TIOCB5/PO31/ET0_CRS/RMII0_CRS_DV/TXD9/SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/SDSI_D1-B	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/SMOSI011/SSDA011/TXD011/IRQ15
54	PB6/A14/MTIOC3D/TIOCA5/PO30/ET0_ETXD1/RMII0_TXD1/RXD9/SMISO9/SSCL9/SMISO11/SSCL11/RXD11/SDSI_D0-B	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/SMISO11/SSCL11/RXD11/SMISO011/SSCL011/RXD011/IRQ6
55	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMR11/PO29/POE4#/ET0_ETXD0/RMII0_TXD0/SCK9/SCK11/SDSI_CLK-B/LCD_CLK-B*1	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMR11/PO29/POE4#/SCK9/SCK11/SCK011/IRQ13
56	PB4/A12/TIOCA4/PO28/ET0_TX_EN/RMII0_TXD_EN/CTS9#/RTS9#/SS9#/SS11#/CTS11#/RTS11#/SDSI_CMD-B/LCD_TCON0-B*1	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#/SS11#/CTS11#/RTS11#/SS011#/CTS011#/RTS011#/DE011/IRQ4
57	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/ET0_RX_ER/RMII0_RX_ER/SCK6/SDSI_D3-B/LCD_TCON1-B*1	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/SCK6/PMC0-DS/IRQ3
58	PB2/A10/TIOCC3/TCLKC/PO26/ET0_RX_CLK/REF50CK0/CTS6#/RTS6#/SS6#/SDSI_D2-B/LCD_TCON2-B*1	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/RTS6#/SS6#/IRQ2
59	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMC10/PO25/ET0_ERXD0/RMII0_RXD0/TXD6/SMOSI6/SSDA6/LCD_TCON3-B*1/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMC10/PO25/TXD6/SMOSI6/SSDA6/IRQ4-DS

100-Pin LQFP	RX65N	RX671
60	VCC	VCC
61	PB0/A8/MTIC5W/TIOCA3/PO24/ ET0_ERXD1/RMII0_RXD1/RXD6/SMISO6/ SSCL6/LCD_DATA0-B*1/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/ SMISO6/SSCL6/IRQ12
62	VSS	VSS
63	PA7/A7/TIOCB2/PO23/ET0_WOL/MISOA-B/ LCD_DATA1-B*1	PA7/A7/TIOCB2/PO23/MISOA-B/MISO0-B/ IRQ7
64	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/ET0_EXOUT/CTS5#/RTS5#/ SS5#/MOSIA-B/LCD_DATA2-B*1	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/CTS5#/RTS5#/SS5#/ MOSIA-B/MOSI0-B/CTS12#/RTS12#/ SS12#/IRQ14
65	PA5/A5/MTIOC6B/TIOCB1/PO21/ ET0_LINKSTA/RSPCKA-B/ LCD_DATA3-B*1	PA5/A5/MTIOC6B/TIOCB1/PO21/ RSPCKA-B/RSPCK0-B/IRQ5
66	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/ET0_MDC/TXD5/SMOSI5/SSDA5/ SSLA0-B/LCD_DATA4-B*1/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ SSL00-B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/IRQ5-DS
67	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/ET0_MDIO/RXD5/SMISO5/ SSCL5/LCD_DATA5-B*1/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ IRQ6-DS
68	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/LCD_DATA6-B*1	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/SSL03-B/RXD12/ SMISO12/SSCL12/RXDX12/SDHI_WP/ IRQ10
69	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/ET0_WOL/SCK5/SSLA2-B/ LCD_DATA7-B*1/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/SCK5/SSLA2-B/SSL02-B/ SCK12/SDHI_CD/IRQ11
70	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/ PO16/CACREF/ET0_TX_EN/ RMII0_TXD_EN/SSLA1-B/LCD_DATA8-B*1	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/ CACREF/PO16/SSLA1-B/SSL01-B/IRQ0
71	PE7/D15[A15/D15]/D7[A7/D7]*1/MTIOC6A/ TOC1/MISOB-B/SDHI_WP/MMC_RES#-B/ LCD_DATA9-B*1/IRQ7/AN105	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/MISOB-B/SDHI_WP/SDHI_D1-B/ QIO1-B/IRQ7
72	PE6/D14[A14/D14]/D6[A6/D6]*1/MTIOC6C/ TIC1/MOSIB-B/SDHI_CD/MMC_CD-B/ LCD_DATA10-B*1/IRQ6/AN104	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/MOSIB-B/SDHI_CD/SDHI_D0-B/ QIO0-B/IRQ6
73	PE5/D13[A13/D13]/D5[A5/D5]*1/MTIOC4C/ MTIOC2B/ET0_RX_CLK/REF50CK0/ RSPCKB-B/LCD_DATA11-B*1/IRQ5/AN103	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/RSPCKB-B/IRQ5
74	PE4/D12[A12/D12]/D4[A4/D4]*1/MTIOC4D/ MTIOC1A/PO28/ET0_ERXD2/SSLB0-B/ LCD_DATA12-B*1/AN102	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/SSLB0-B/IRQ12
75	PE3/D11[A11/D11]/D3[A3/D3]*1/MTIOC4B/ PO26/TOC3/POE8#/ET0_ERXD3/CTS12#/ RTS12#/SS12#/MMC_D7-B/ LCD_DATA13-B*1/AN101	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/POE8#/TOC3/CTS12#/RTS12#/ SS12#/IRQ11
76	PE2/D10[A10/D10]/D2[A2/D2]*1/MTIOC4A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B*1/IRQ7-DS/AN100	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/IRQ7-DS

100-Pin LQFP	RX65N	RX671
77	PE1/D9[A9/D9]/D1[A1/D1]*1/MTIOC4C/MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/MMC_D5-B/LCD_DATA15-B*1/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/IRQ9/ANEX1
78	PE0/D8[A8/D8]/D0[A0/D0]*1/MTIOC3D/SCK12/SSLB1-B/MMC_D4-B/LCD_DATA16-B*1/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/SCK12/SSLB1-B/IRQ8/ANEX0
79	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/LCD_DATA17-B*1/IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/SDHI_D1-B/QIO1-B/IRQ7/AN100
80	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/MMC_D0-B/LCD_DATA18-B*1/IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2-A/SDHI_D0-B/QIO0-B/IRQ6/AN101
81	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1-A/QSPCLK-B/SDHI_CLK-B/MMC_CLK-B/LCD_DATA19-B*1/IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1-A/SDHI_CLK-B/QSPCLK-B/IRQ5/AN102
82	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0-A/QSSL-B/SDHI_CMD-B/MMC_CMD-B/LCD_DATA20-B*1/IRQ4/AN112	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0-A/SDHI_CMD-B/QSSL-B/IRQ4/AN103
83	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/RSPCKC-A/QIO3-B/SDHI_D3-B/MMC_D3-B/LCD_DATA21-B*1/IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/RSPCKC-A/SDHI_D3-B/QIO3-B/IRQ3/AN104
84	PD2/D2[A2/D2]/MTIOC4D/TIC2/MISOC-A/CRX0/QIO2-B/SDHI_D2-B/MMC_D2-B/LCD_DATA22-B*1/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/MISOC-A/SDHI_D2-B/QIO2-B/IRQ2/AN105
85	PD1/D1[A1/D1]/MTIOC4B/POE0#/MOSIC-A/CTX0/LCD_DATA23-B*1/IRQ1/AN109	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/MOSIC-A/IRQ1/AN106
86	PD0/D0[A0/D0]/POE4#/LCD_EXTCLK-B*1/IRQ0/AN108	PD0/D0[A0/D0]/POE4#/IRQ0/AN107
87	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
88	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
89	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
90	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
91	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
92	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
93	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
94	VREFL0	VREFL0
95	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
96	VREFH0	VREFH0
97	AVCC0	AVCC0
98	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
99	AVSS0	AVSS0
100	P05/IRQ13/DA1	P05/IRQ13

Notes: 1. Valid only on products with a code flash memory capacity of 2 MB or 1.5 MB.

2. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.



### 3.4 64-Pin TFBGA Package

Table 3.4 is a comparative listing of the pin functions of 64-pin TFBGA package products.

**Table 3.4 Comparative Listing of 64-Pin TFBGA Package Pin Functions**

64-Pin TFBGA	RX65N	RX671
A1	AVCC1	AVCC1
A2	AVSS0	AVSS0
A3	VREFH0	VREFH0
A4	VREFL0	VREFL0
A5	PD2/MTIOC4D/TIC2/QIO2-B/SDHI_D2-B/IRQ2/ <b>AN110</b>	PD2/MTIOC4D/TIC2/SDHI_D2-B/QIO2-B/IRQ2/ <b>AN105</b>
A6	PD7/MTIC5U/POE0#/ <b>QMI-B</b> /QIO1-B/SDHI_D1-B/IRQ7/ <b>AN107</b>	PD7/MTIC5U/POE0#/SDHI_D1-B/QIO1-B/IRQ7/ <b>AN100</b>
A7	PE0/MTIOC3D/SCK12/ANEX0	PE0/MTIOC3D/SCK12/ <b>SSLB1-B</b> /IRQ8/ANEX0
A8	PE2/MTIOC4A/TIC3/RXD12/SSCL12/RXDX12/IRQ7-DS	PE2/MTIOC4A/TIC3/RXD12/ <b>SMISO12</b> /SSCL12/RXDX12/ <b>SSLB3-B</b> /IRQ7-DS
B1	EMLE	EMLE
B2	AVSS1	AVSS1
B3	AVCC0	AVCC0
B4	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
B5	PD3/MTIOC8D/TOC2/POE8#/ <b>QIO3-B</b> /SDHI_D3-B/IRQ3/ <b>AN111</b>	PD3/MTIOC8D/POE8#/TOC2/SDHI_D3-B/QIO3-B/IRQ3/ <b>AN104</b>
B6	PD6/MTIC5V/MTIOC8A/POE4#/ <b>QMO-B</b> /QIO0-B/SDHI_D0-B/IRQ6/ <b>AN106</b>	PD6/MTIC5V/MTIOC8A/POE4#/ <b>SDHI_D0-B</b> /QIO0-B/IRQ6/ <b>AN101</b>
B7	PE1/MTIOC4C/MTIOC3B/TXD12/SSDA12/TXDX12/SIOX12/ANEX1	PE1/MTIOC4C/MTIOC3B/TXD12/ <b>SMOSI12</b> /SSDA12/TXDX12/SIOX12/ <b>SSLB2-B</b> /IRQ9/ANEX1
B8	PE6/MTIOC6C/TIC1/SDHI_CD/IRQ6	PE6/MTIOC6C/TIC1/ <b>MOSIB-B</b> /SDHI_CD/ <b>SDHI_D0-B</b> /QIO0-B/IRQ6
C1	VCL	VCL
C2	VBATT	VBATT
C3	MD/FINED	MD/FINED
C4	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
C5	PD4/MTIOC8B/POE11#/ <b>QSSL-B</b> /SDHI_CMD-B/IRQ4/ <b>AN112</b>	PD4/MTIOC8B/POE11#/ <b>SDHI_CMD-B</b> /QSSL-B/IRQ4/ <b>AN103</b>
C6	PD5/MTIC5W/MTIOC8C/POE10#/ <b>QSPCLK-B</b> /SDHI_CLK-B/IRQ5/ <b>AN113</b>	PD5/MTIC5W/MTIOC8C/POE10#/ <b>SDHI_CLK-B</b> /QSPCLK-B/IRQ5/ <b>AN102</b>
C7	PA1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/SCK5/IRQ11	PA1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/SCK5/ <b>SSLA2-B</b> / <b>SSL02-B</b> /SCK12/ <b>SDHI_CD</b> /IRQ11
C8	PE7/MTIOC6A/TOC1/SDHI_WP/IRQ7	PE7/MTIOC6A/TOC1/ <b>MISOB-B</b> /SDHI_WP/ <b>SDHI_D1-B</b> /QIO1-B/IRQ7
D1	XCIN	XCIN
D2	XCOUT	XCOUT
D3	RES#	RES#
D4	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
D5	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
D6	PA6/MTIC5V/MTCLKB/TIOCA2/TMCI3/POE10#/CTS5#/RTS5#/SS5#	PA6/MTIC5V/MTCLKB/TIOCA2/TMCI3/POE10#/CTS5#/RTS5#/SS5#/ <b>MOSIA-B</b> / <b>MOSIO-B</b> /CTS12#/ <b>RTS12#</b> / <b>SS12#</b> /IRQ14

64-Pin TFBGA	RX65N	RX671
D7	PA2/MTIOC7A/RXD5/SMISO5/SSCL5	PA2/MTIOC7A/RXD5/SMISO5/SSCL5/ SSLA3-B/SSL03-B/RXD12/SMISO12/ SSCL12/RDX12/SDHI_WP/IRQ10
D8	PA4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ TXD5/SMOSI5/SSDA5/IRQ5-DS	PA4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ TXD5/SMOSI5/SSDA5/SSLA0-B/SSL00-B/ TXD12/SMOSI12/SSDA12/TXD12/SIOX12/ IRQ5-DS
E1	XTAL/P37	XTAL/P37
E2	VSS	VSS
E3	TRST#/P34/MTIOC0A/TMCI3/POE10#/IRQ4	TRST#/P34/MTIOC0A/TMCI3/POE10#/IRQ4/ TS0
E4	P13/MTIOC0B/TIOCA5/TMO3/TXD2/SSDA2/ SDA0[FM+]/IRQ3/ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/ SDAHS0[FM+/HS]/IRQ3/ADTRG1#
E5	BSCANP	BSCANP
E6	PA7/TIOCB2	PA7/TIOCB2/MISOA-B/MISO0-B/IRQ7
E7	VCC	VCC
E8	VSS	VSS
F1	EXTAL/P36	EXTAL/P36
F2	VCC	VCC
F3	UPSEL/P35/NMI	UPSEL/P35/NMI
F4	P12/TMCI1/RXD2/SSCL2/SCL0[FM+]/IRQ2	P12/TMCI1/MTIC5U/RXD2/SMISO2/SSCL2/ SCL0[FM+]/SCLHS0[FM+/HS]/IRQ2
F5	P53	P53/SSIRXD0/PMC0-DS/IRQ3/TS12
F6	PB7/MTIOC3B/TIOCB5/TXD9/SSDA9/ SSDA11/TXD11	PB7/MTIOC3B/TIOCB5/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/TXD11/ SMOSI011/SSDA011/TXD011/IRQ15
F7	PB6/MTIOC3D/TIOCA5/RXD9/SSCL9/ SSCL11/RXD11	PB6/MTIOC3D/TIOCA5/RXD9/SMISO9/ SSCL9/SMISO11/SSCL11/RXD11/ SMISO011/SSCL011/RXD011/IRQ6
F8	PB5/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/ POE4#/SCK9/SCK11	PB5/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/ POE4#/SCK9/SCK11/SCK011/IRQ13
G1	TCK/P27/MTIOC2B/TMCI3/SCK1/ RSPCKB-A	TCK/P27/MTIOC2B/TMCI3/SCK1/ RSPCKB-A/IRQ7/TS2
G2	TMS/P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/ RTS1#/SS1#/SSLB0-A/IRQ1-DS	TMS/P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/ RTS1#/SS1#/SSLB0-A/IRQ1-DS/TAMPI1
G3	TDI/P30/MTIOC4B/TMRI3/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS/ TAMPI0
G4	VCC_USB	VCC_USB
G5	VSS_USB	VSS_USB
G6	UB/PC7/MTIOC3A/MTCLKB/TMO2/TOC0/ CACREF/TXD8/SMOSI8/SSDA8/SMOSI10/ SSDA10/TXD10/MISOA-A/IRQ14	UB/PC7/MTIOC3A/MTCLKB/TMO2/TOC0/ CACREF/TXD8/SMOSI8/SSDA8/SMOSI10/ SSDA10/TXD10/MISOA-A/SSITXD0/ SMOSI010/SSDA010/TXD010/MISO0-A/ IRQ14
G7	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/ SCK10/RSPCKA-A	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/ SCK10/RSPCKA-A/SSIBCK0/SCK010/ RSPCK0-A/IRQ5/TS14
G8	PC0/MTIOC3C/TCLKC/SSLA1-A/IRQ14	PC0/MTIOC3C/TCLKC/CTS5#/RTS5#/SS5#/ SSLA1-A/RXD011/SMISO011/SSCL011/ SSL01-A/IRQ14/TS16

64-Pin TFBGA	RX65N	RX671
H1	TDO/P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/MOSIB-A	TDO/P26/MTIOC2A/TMO1/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB-A/IRQ6/TS3
H2	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/POE8#/SCK1/TXD3/SSDA3/SDA2-DS/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/SSITXD0/SDHI_D3-C/IRQ7/ADTRG1#
H3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/SSCL3/SCL2-DS/USB0_VBUS/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/USB0_VBUS/IRQ6/ADTRG0#
H4	USB0_DM	PH2/TMRI0/USB0_DM/IRQ1
H5	USB0_DP	PH1/TMO0/USB0_DP/IRQ0
H6	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/IRQ13	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/SMISO010/SSCL010/RXD010/MOSI0-A/SSILRCK0/IRQ13/TS13
H7	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/CTS8#/RTS8#/SS8#/SS10#/CTS10#/RTS10#/SSLA0-A	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/CTS8#/RTS8#/SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/AUDIO_CLK/SS010#/CTS010#/RTS010#/DE010/SSL00-A/SDHI_D1-A/QIO1-A/IRQ12/TSCAP
H8	PC1/MTIOC3A/TCLKD/SSLA2-A/IRQ12	PC1/MTIOC3A/TCLKD/SCK5/SSLA2-A/TXD011/SMOSI011/SSDA011/TXDA011/SSL02-A/IRQ12/TS15

### 3.5 64-Pin LFQFP Package

Table 3.5 is a comparative listing of the pin functions of 64-pin LFQFP package products.

**Table 3.5 Comparative Listing of 64-Pin LFQFP Package Pin Functions**

64-Pin LFQFP	RX65N	RX671
1	AVCC1	AVCC1
2	EMLE	EMLE
3	AVSS1	AVSS1
4	VCL	VCL
5	VBATT	VBATT
6	MD/FINED	MD/FINED
7	XCIN	XCIN
8	XCOU	XCOU
9	RES#	RES#
10	XTAL/P37	XTAL/P37
11	VSS	VSS
12	EXTAL/P36	EXTAL/P36
13	VCC	VCC
14	UPSEL/P35/NMI	UPSEL/P35/NMI
15	TRST#/P34/MTIOC0A/TMCI3/POE10#/IRQ4	TRST#/P34/MTIOC0A/TMCI3/POE10#/IRQ4/ TS0
16	TDI/P30/MTIOC4B/TMRI3/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS/ TAMPI0
17	TMS/P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/ RTS1#/SS1#/SSLB0-A/IRQ1-DS	TMS/P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/ RTS1#/SS1#/SSLB0-A/IRQ1-DS/TAMPI1
18	TDO/P26/MTIOC2A/TMO1/TXD1/SMOSI1/ SSDA1/CTS3#/RTS3#/MOSIB-A	TDO/P26/MTIOC2A/TMO1/TXD1/CTS3#/ RTS3#/SMOSI1/SS3#/SSDA1/MOSIB-A/ IRQ6/TS3
19	TCK/P27/MTIOC2B/TMCI3/SCK1/ RSPCKB-A	TCK/P27/MTIOC2B/TMCI3/SCK1/ RSPCKB-A/IRQ7/TS2
20	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/POE8#/SCK1/TXD3/SSDA3/ SDA2-DS/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/POE8#/SCK1/TXD3/SMOSI3/ SSDA3/SDA2-DS/SSITXD0/SDHI_D3-C/ IRQ7/ADTRG1#
21	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/RTCOU/TXD1/SMOSI1/SSDA1/ RXD3/SSCL3/SCL2-DS/ USB0_VBUS/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/RTCOU/TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/SCL2-DS/ USB0_VBUS/IRQ6/ADTRG0#
22	P13/MTIOC0B/TIOCA5/TMO3/TXD2/SSDA2/ SDA0[FM+]/IRQ3/ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/ SDAHS0[FM+/HS]/IRQ3/ADTRG1#
23	P12/TMCI1/RXD2/SSCL2/SCL0[FM+]/IRQ2	P12/TMCI1/MTIC5U/RXD2/SMISO2/SSCL2/ SCL0[FM+]/SCLHS0[FM+/HS]/IRQ2
24	VCC_USB	VCC_USB
25	USB0_DM	PH2/TMRI0/USB0_DM/IRQ1
26	USB0_DP	PH1/TMO0/USB0_DP/IRQ0
27	VSS_USB	VSS_USB
28	P53	P53/SSIRXD0/PMC0-DS/IRQ3/TS12

64-Pin LQFP	RX65N	RX671
29	UB/PC7/MTIOC3A/MTCLKB/TMO2/TOC0/CACREF/TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/IRQ14	UB/PC7/MTIOC3A/MTCLKB/TMO2/TOC0/CACREF/TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/SSITXD0/SMOSI010/SSDA010/TXD010/MISO0-A/IRQ14
30	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/IRQ13	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/SMISO010/SSCL010/RXD010/MOSI0-A/SSILRCK0/IRQ13/TS13
31	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/SCK10/RSPCKA-A	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/SCK10/RSPCKA-A/SSIBCK0/SCK010/RSPCK0-A/IRQ5/TS14
32	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/CTS8#/RTS8#/SS8#/SS10#/CTS10#/RTS10#/SSLA0-A	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/CTS8#/RTS8#/SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/AUDIO_CLK/SS010#/CTS010#/RTS010#/DE010/SSL00-A/SDHI_D1-A/QIO1-A/IRQ12/TSCAP
33	PC1/MTIOC3A/TCLKD/SSLA2-A/IRQ12	PC1/MTIOC3A/TCLKD/SCK5/SSLA2-A/TXD011/SMOSI011/SSDA011/TXDA011/SSL02-A/IRQ12/TS15
34	PC0/MTIOC3C/TCLKC/SSLA1-A/IRQ14	PC0/MTIOC3C/TCLKC/CTS5#/RTS5#/SS5#/SSLA1-A/RXD011/SMISO011/SSCL011/SSL01-A/IRQ14/TS16
35	PB7/MTIOC3B/TIOCB5/TXD9/SSDA9/SSDA11/TXD11	PB7/MTIOC3B/TIOCB5/TXD9/SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/SMOSI011/SSDA011/TXD011/IRQ15
36	PB6/MTIOC3D/TIOCA5/RXD9/SSCL9/SSCL11/RXD11	PB6/MTIOC3D/TIOCA5/RXD9/SMISO9/SSCL9/SMISO11/SSCL11/RXD11/SMISO011/SSCL011/RXD011/IRQ6
37	PB5/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/POE4#/SCK9/SCK11	PB5/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/POE4#/SCK9/SCK11/SCK011/IRQ13
38	VCC	VCC
39	VSS	VSS
40	PA7/TIOCB2	PA7/TIOCB2/MISOA-B/MISO0-B/IRQ7
41	PA6/MTIC5V/MTCLKB/TIOCA2/TMCI3/POE10#/CTS5#/RTS5#/SS5#	PA6/MTIC5V/MTCLKB/TIOCA2/TMCI3/POE10#/CTS5#/RTS5#/SS5#/MOSIA-B/MOSI0-B/CTS12#/RTS12#/SS12#/IRQ14
42	PA4/MTIC5U/MTCLKA/TIOCA1/TMRI0/TXD5/SMOSI5/SSDA5/IRQ5-DS	PA4/MTIC5U/MTCLKA/TIOCA1/TMRI0/TXD5/SMOSI5/SSDA5/SSLA0-B/SSL00-B/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ5-DS
43	PA2/MTIOC7A/RXD5/SMISO5/SSCL5	PA2/MTIOC7A/RXD5/SMISO5/SSCL5/SSLA3-B/SSL03-B/RXD12/SMISO12/SSCL12/RDX12/SDHI_WP/IRQ10
44	PA1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/SCK5/IRQ11	PA1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/SCK5/SSLA2-B/SSL02-B/SCK12/SDHI_CD/IRQ11
45	PE7/MTIOC6A/TOC1/SDHI_WP/IRQ7	PE7/MTIOC6A/TOC1/MISOB-B/SDHI_WP/SDHI_D1-B/QIO1-B/IRQ7
46	PE6/MTIOC6C/TIC1/SDHI_CD/IRQ6	PE6/MTIOC6C/TIC1/MOSIB-B/SDHI_CD/SDHI_D0-B/QIO0-B/IRQ6
47	PE2/MTIOC4A/TIC3/RXD12/SSCL12/RXDX12/IRQ7-DS	PE2/MTIOC4A/TIC3/RXD12/SMISO12/SSCL12/RDX12/SSLB3-B/IRQ7-DS

64-Pin LQFP	RX65N	RX671
48	PE1/MTIOC4C/MTIOC3B/TXD12/SSDA12/TXDX12/SIOX12/ANEX1	PE1/MTIOC4C/MTIOC3B/TXD12/ <b>SMOS12</b> /SSDA12/TXDX12/SIOX12/ <b>SSLB2-B/IRQ9</b> /ANEX1
49	PE0/MTIOC3D/SCK12/ANEX0	PE0/MTIOC3D/SCK12/ <b>SSLB1-B/IRQ8</b> /ANEX0
50	PD7/MTIC5U/POE0#/ <b>QMI-B</b> /QIO1-B/SDHI_D1-B/IRQ7/ <b>AN107</b>	PD7/MTIC5U/POE0#/SDHI_D1-B/QIO1-B/IRQ7/ <b>AN100</b>
51	PD6/MTIC5V/MTIOC8A/POE4#/ <b>QMO-B</b> /QIO0-B/SDHI_D0-B/IRQ6/ <b>AN106</b>	PD6/MTIC5V/MTIOC8A/POE4#/SDHI_D0-B/QIO0-B/IRQ6/ <b>AN101</b>
52	PD5/MTIC5W/MTIOC8C/POE10#/QSPCLK-B/SDHI_CLK-B/IRQ5/ <b>AN113</b>	PD5/MTIC5W/MTIOC8C/POE10#/SDHI_CLK-B/QSPCLK-B/IRQ5/ <b>AN102</b>
53	PD4/MTIOC8B/POE11#/QSSL-B/SDHI_CMD-B/IRQ4/ <b>AN112</b>	PD4/MTIOC8B/POE11#/SDHI_CMD-B/QSSL-B/IRQ4/ <b>AN103</b>
54	PD3/MTIOC8D/TOC2/POE8#/QIO3-B/SDHI_D3-B/IRQ3/ <b>AN111</b>	PD3/MTIOC8D/POE8#/TOC2/SDHI_D3-B/QIO3-B/IRQ3/ <b>AN104</b>
55	PD2/MTIOC4D/TIC2/QIO2-B/SDHI_D2-B/IRQ2/ <b>AN110</b>	PD2/MTIOC4D/TIC2/SDHI_D2-B/QIO2-B/IRQ2/ <b>AN105</b>
56	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
57	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
58	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
59	VREFL0	VREFL0
60	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
61	VREFH0	VREFH0
62	AVCC0	AVCC0
63	AVSS0	AVSS0
64	P05/IRQ13/ <b>DA1</b>	P05/IRQ13

## 4. Notes on Migration

This section presents important information regarding differences between the RX671 Group and RX65N Group.

4.1, Notes on Functional Design, presents information regarding the software.

### 4.1 Notes on Functional Design

Some software that runs on the RX65N Group is compatible with the RX671 Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

Software-related considerations regarding function settings that differ between the RX671 Group and RX65N Group are as follows:

For differences between modules and functions, refer to 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware of each MCU group, listed in 5, Reference Documents.

#### 4.1.1 Running RAM Self-Diagnostics on Register Save Banks

On the RX671 Group the register save banks are configured in the RAM. The register save banks are buffered, so writing to a bank with the SAVE instruction and then reading from the same bank with the RSTR instruction immediately afterwards may result in data being read from the buffer rather than from the RAM memory cells. When running RAM self-diagnostics on a register save bank, follow the steps below to ensure that the previously written data is read from the RAM rather than from the buffer.

- (1) Use the SAVE instruction to write data to the bank on which self-diagnostics will be run.
- (2) Use the SAVE instruction to write data to a bank other than that written to in step (1).
- (3) Use the RSTR instruction to read data from the bank written to in step (1).

#### 4.1.2 Setting Number of Flash Memory Access Wait States

On the RX65N Group it is necessary to modify the ROMWT register in order to set the MCU's system clock (ICLK) to a frequency higher than 50 MHz, but on the RX671 Group modification of the ROMWT register is needed only when setting ICLK to a frequency higher than 60 MHz.

#### 4.1.3 Note on RX671 Group 48-Pin Package Products

On the RX671 Group the sub-clock and RTC cannot be used on 48-pin package products. After a cold start the state of the sub-clock control circuit is unstable, so do not fail to set these bits following a cold start. For details, refer to RX671 Group User's Manual: Hardware, listed in 5, Reference Documents.

#### 4.1.4 Current Flow to VBATT Pin

On the RX671 Group, when the VCC voltage rises to  $V_{BATT} + 0.6$  V or higher while operating in battery backup mode, a current flows from the VCC pin, via a parasitic diode in the power switch on the VCC side, to the VBATT pin. If this presents a problem, insert a low-dropout diode between the backup power supply and the VBATT pin.

#### 4.1.5 Port Direction Register (PDR) Initialization

The method for initializing the PDR register differs even on products with the same pin count.

#### 4.1.6 Quad Serial Peripheral Interface/Quad SPI Memory Interface

The quad SPI memory interface registers on the RX671 Group incorporate significant changes compared to the quad serial peripheral interface registers on the RX65N Group. This results in a reduction in software compatibility.

## 5. Reference Documents

### User's Manual: Hardware

RX65N Group, RX651 Group User's Manual: Hardware, Rev. 2.30 (R01UH0590EJ0230)  
(The latest version can be downloaded from the Renesas Electronics website.)

RX65N Group, RX651 Group Flash Memory User's Manual: Hardware Interface,  
Rev. 2.10 (R01UH0602EJ0210)  
(The latest version can be downloaded from the Renesas Electronics website.)

RX671 Group User's Manual: Hardware, Rev. 1.10 (R01UH0899EJ0110)  
(The latest version can be downloaded from the Renesas Electronics website.)

### Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)



## Related Technical Updates

This application note reflects the content of the following technical updates:

- TN-RX\*-A0215A/E
- TN-RX\*-A0223A/E
- TN-RX\*-A0224B/E
- TN-RX\*-A0227A/E
- TN-RX\*-A0233A/E
- TN-RX\*-A0235B/E
- TN-RX\*-A0236B/E
- TN-RX\*-A0248A/E
- TN-RX\*-A0250A/E
- TN-RX\*-A0257A/E

### Revision History

Rev.	Date	Description	
		Page	Summary
1.00	May 17, 2021	—	First edition issued
1.10	May 20, 2022	15	<i>Revised:</i> Table 2.5 Comparison of Clock Generation Circuit Registers
		119	<i>Revised:</i> Table 2.72 Comparison of Packages

## General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

### 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

### 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

### 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

### 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

### 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

### 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

### 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

### 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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