RENESAS

FemtoClock 2 – Generating Synchronous Ethernet (SyncE) Clocks

This document describes how a high-performance FemtoClock®2 clock generator with jitter attenuating capabilities can be configured to comply with Synchronous Ethernet (SyncE) Clock requirements.

Contents

1.	Introduction1
2.	Renesas IC Toolbox (RICBox) Software for FemtoClock 2 Configuration2
3.	Revision History

1. Introduction

FemtoClock 2 is a high-performance clock generator with jitter attenuating capabilities that can be configured to comply with Synchronous Ethernet Clock requirements. ITU-T G.8262/Y.1362 outlines requirements for timing devices used in synchronizing network equipment that support synchronous Ethernet or SyncE. SyncE is used to distribute the primary references clock (PRC) for network synchronization.

G.8262 requirements include clock accuracy, noise transfer, holdover performance and noise generation. It contains two options for SyncE:

- 1. EEC-Option 1 applies to synchronous Ethernet equipment that is designed to work with networks optimized for the 2048Kbps hierarchy.
- 2. EEC-Option 2 applies to synchronous Ethernet equipment that is designed to work with networks optimized for the 1544Kbps hierarchy.

FemtoClock 2 configurations can be created with the Renesas IC Toolbox (RICBox[™]) software. The RICBox software is aware of the above two options and the jitter attenuator can be properly and fully configured, simply by selecting "G.8262 Option 1" or "G.8262 Option 2" in a drop-down menu. The RICBox software also has a third selection for G.8262.1 eEEC "enhanced SyncE".

The recommended FemtoClock 2 device for use with SyncE is the RC32504A. Instead of using a quartz crystal, a TCXO or other stable frequency reference is required to drive the XIN pin on the RC32504A. Consult application note <u>AN-807</u> for acceptable frequency reference devices.

Compliance of FemtoClock 2 with the synchronous Ethernet requirements has been thoroughly tested. For more details, see the <u>RC32504A ITU-T G.8262 and G.8262.1 Compliance Test Report</u> and the following test setup diagram.





2. Renesas IC Toolbox (RICBox) Software for FemtoClock 2 Configuration

The FemtoClock 2 Renesas IC Toolbox (RICBox) software can be downloaded from the <u>RC32504A</u> webpage. The software consists of a main "Toolbox Installer" and the "GUI Installer" that is specific for the FemtoClock 2 products.

Title	Туре	Format	File Size	Date
Software				
FemtoClock2 Renesas IC Toolbox GUI Installer v2.0.0	Software & Tools - Software	ZIP	5.47 MB	Apr 23, 2021
Renesas IC Toolbox Installer v3.3.0	Software & Tools - Software	ZIP	191.06 MB	Apr 23, 2021

Figure 2. FemtoClock 2 Webpage Downloads

When Toolbox Installer software is already installed for use with a different product family, only the GUI Installer for FemtoClock 2 needs to be installed. After installing both packages, run the software and the opening screen should be similar what is shown in Figure 3:

FemtoClock 2 – Generating Synchronous Ethernet (SyncE) Clocks Application Note

RICBox			_	×
<u>F</u> ile <u>H</u> elp				
	New	Browse		
Recent Files				
hello.rbs C:\Users\evkeulen\Desktop				
Online Documentation				
Renesas Website				
Sales Support				
Technical Support				

Figure 3. RICBox Opening Screen

Click *New* to start a new configuration, *Browse* to find a ".rbs" file with a previously saved configuration, or double-click on one of the most recently saved configurations (e.g., like the "hello.rbs" in above Figure 3).

For this application note, we will continue creating a new configuration. After clicking *New*, the following screen appears:

RICBox	_		×
1. Select Product Family			
FemtoClock2	The FemtoClock2 series of Clock Generators and Jitter Attenuators is an excellent cho generating and/or cleaning up noisy clock signals right near the device being clocked use'. The combination of small size (4x4mm), low power and excellent noise performs family in a class by itself. RC22504: Clock Generation RC22514: Clock Generation with internal crystal RC32504: Jitter Attenuation RC32514: Jitter Attenuation with internal crystal	ice for I – the 'J nce set	point-of- s this
2. Select Product			
RC22504A RC22514A			
RC32504A			
RC32514A			
	Back		OK



First, select a Product Family. When this is a new RICBox installation and only the FemtoClock 2 GUI is installed, the screen should look exactly like Figure 4 with only the FemtoClock 2 Family showing at item 1.

Next, select the specific product. We want to use Jitter Attenuator features, so select the RC32504A. The RC32514A is not recommended because it has an internal crystal. A plain crystal is not stable enough for SyncE.

The RICBox software starts a configuration with a Wizard for entering the most important information needed for the configuration. Selection of the SyncE options is part of the Wizard (see the first Wizard screen as shown in Figure 5).

RICBox						\times
<u>F</u> ile <u>T</u> ools <u>H</u> elp						
Configuring RC32504A		1 of 3 Inp	uts			v
Operation Mode Jitter Attenuator Crystal Frequency 60MHz Load Capacitance (pF) 4.1 Clock Mode LVDS Frequency CLKIN Clock Mode LVDS Clock Mode LVDS Clock Mode Concel Cancel		Previous	Operation Ma Synthesizer - configured to clock source a the analog PL APLL then us source to ger outputs. The source is sele the APLL Refe can come fro CLKIN. Jitter Attenua is configured reference for the input to t clock source a	ode: The c o use as the as the LL (AP es tha merate refere cted l erence m eith tor - to us the X he AF at the	device is a single input to PLL). The at clock the ence by using e mux a her XIN The device the CIN pin a PLL and CLKIN Fin	and or rice pin ~
	0 Errors	0 Warnings	RC32504A	No	ot Conn	ected

Figure 5. RICBox – First Wizard Screen

First, select the Operating Mode to be "Jitter Attenuator". Then select a crystal frequency. Note that in this case it will be the frequency of a TCXO or other stable frequency reference. Select "Overdrive" to indicate that the Crystal Oscillator Input pin (XIN) will be overdriven with an external clock. When selecting "Overdrive", the Load Capacitance value is reduced to the smallest value to minimize loading of the external clock (consult the RC32504A datasheet for circuit recommendations when overdriving the crystal interface).

Finally, on this wizard screen you can also enter the reference clock input properties. You can enter the reference clock frequency and the Clock Mode. The "LVDS" clock mode is the most versatile selection where the input can essentially handle any differential clock that is AC coupled. For more details of the reference clock settings, see the RC32504A datasheet.

The second Wizard screen (see Figure 6) sets up the Jitter Attenuator features and this is where the SyncE settings are found.

593										
III RICBox							_		Ц	×
File Tools Help					_					
Configuring RC32504A					2 of 3	DPLL				~
DPLL Profile jitter atte jitter atte jitter atte G.8262 o Normal Ba G.8262 o Actual: ~2 G.8262.1 Acquire Bandwidth G Actual: ~222.3227H Decimator Decimator Decimator Bandwidt Actual: ~1.9428kHz Gain Peaking Normal Gain Peaking Actual: ~0.1804 (-9. Acquire Gain Peaking Actual: ~0.192 (-3.9 Phase Slope Limit Phase Slope Limit Ge Actual: maximum	nuator mode nuator mode otion 1 otion 2 oal 250 c (-11.0709% fro Goal 2.51 (-22.2876% fro Goal 0.2 7888% from goal Goal 0.2 756% from goal al None	i 25Hz) iOHz irom goal of 25DH: 5kHz pm goal of 2.5kHz pm goal of 0.2) 2 al of 0.2)	①	0 Error	Previou	The allo of t for clock Selection (Construction) and the main term in the main term is a dot of the main term is the main term is a dot of the main term is the main term is a dot of the main term is a dot	e DPLL prof ws for quiche Renesa specific ITI ck recomme ecting a sp ifigure the y Renesas the ipment clo pur labs. M configurat de, but car make sure broken. more com ase contac litional sup er Attenuat ====== s profile co vice for jitte input clock requireme PLL Loop F tz (accepta Hz ~ 12kH PLL Phase imited PII Damni Next	ile droc ck con s timir J-T eq endat ecific p device ests fc ock coo odifica compl plex c t Rene port. tor ==== nnfigur ents: iilter B ble ra z) Slope	op-down figuration g device juipment ions. profile we the san or ITU-T mpliance ations to an be t be take iance is clock tree isas for clock tree clock tree isas for clock tree clock tree isas for clock tree clock	in in in in in in in in
				o chois	o warm		1032304A		it conne	cicu

Figure 6. RICBox – Second Wizard Screen

The SyncE option can be selected at the top of the screen with the "DPLL Profile" setting. With this setting, all the other fields will be populated with the appropriate values so the DPLL Profile setting is the only setting needed.

The top selection of "jitter attenuator mode" from the pull-down list allows you to edit each of the parameters. After selecting a SyncE option, you can still modify settings but the software will warn that the configuration may no longer comply with the selected SyncE option.

II RICBox	– 🗆 ×
<u>F</u> ile <u>T</u> ools <u>H</u> elp	
Configuring RC32504A	2 of 3 DPLL Y
DPLL Profile G.8262 option 1	The DPLL profile drop-down allows for quick configuration of the Renesas timing device for specific ITU-T equipment clock recommendations. Selecting a specific profile will configure the device the same way Renesas tests for ITU-T equipment clock compliance
Decimator Decimator Bandwidth Goal 130Hz Actual: ~121.4256Hz (-6.5957% from goal of 130Hz)	in our labs. Modifications to the configuration can be made, but care must be taken to make sure compliance is not broken. For more complex clock trees, please contact Renesas for
Gain PeakingNormal Gain Peaking Goal0.2Actual: ~0.1886 (-5.7137% from goal of 0.2)Acquire Gain Peaking Goal0.2Actual: ~0.1804 (-9.7888% from goal of 0.2)	additional support. • Jitter Attenuator ================= This profile configures the device for jitter attenuation of an input clock.
Phase Slope Limit Phase Slope Limit Goal 7500 of ns/sec Actual: ~7499.9924	Key requirements: * DPLL Loop Filter Bandwidth: 25Hz (acceptable range is 0.1Hz ~ 12kHz) * DPLL Phase Slope Limit: Unlimited * DPLL Damping Goal: < 0.2dB
Cancel 0 Errors	Previous Next Finish 0 Warnings RC32504A Not Connected

Select G.8262 option 1 as shown in Figure 7. This screen shows the values when selecting G.8262 option 1.

Figure 7. RICBox – Select G.8282 Option 1

RICBox	– 🗆 X
<u>F</u> ile <u>T</u> ools <u>H</u> elp	
Configuring RC32504A 2 of 3	DPLL ~
DPLL Profile G.8262 option 2	The DPLL profile drop-down allows for quick configuration of the Renesas timing device for specific ITU-T equipment clock recommendations. Selecting a specific profile will configure the device the same way Renesas tests for ITU-T equipment clock compliance in our labs. Modifications to the configuration can be made, but care must be taken to make sure compliance is not broken.
Actual: ~121.4256Hz (-6.5957% from goal of 130Hz) Gain Peaking Normal Gain Peaking Goal 0.2 Actual: ~0.1804 (-9.7888% from goal of 0.2) Acquire Gain Peaking Goal 0.2 Actual: ~0.1702 (-14.9222% from goal of 0.2)	For more complex clock trees, please contact Renesas for additional support. • Jitter Attenuator ====================================
Phase Slope Limit Phase Slope Limit Goal 885 Actual: ~884.9828 Cancel Previo	Key requirements: * DPLL Loop Filter Bandwidth: 25Hz (acceptable range is 0.1Hz ~ 12kHz) * DPLL Phase Slope Limit: Unlimited * DPLL Damping Goal: < 0.2dB ous Next Finish
0 Errors 0 Warr	nings RC32504A Not Connected

Select G.8262 option 2 as shown in Figure 8. This screen shows the values when selecting G.8262 option 2.

Figure 8. RICBox – Select G.8282 Option 2

The third and last screen of the Wizard allows you to set up the clock outputs of FemtoClock 2. Consult the <u>FemtoClock 2 GUI User Guide</u> for more details about using the RICBox software. The GUI User Guide can also be downloaded from the RC32504A webpage.

3. Revision History

Revision	Date	Description
1.00	Sep 20, 2021	Initial release.

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