FemtoClock®3 (FC3) and FemtoClock 3 Wireless (FC3W) Frequency Planning

This document describes how to configure the FemtoClock®3 (FC3) and FemtoClock 3 Wireless (FC3W) devices to achieve the best performance in terms of phase noise with the lowest crosstalk. Included is an example using the GUI in Synthesizer Mode.

Contents

1. Introduction

FemtoClock 3 (FC3) and FemtoClock 3 Wireless (FC3W) devices are a family of telecom integrated circuits that are low-phase noise jitter attenuators. These include the RC32312 and RC32308 (FC3) or the RC38108, RC38208, RC38112 and RC38312 (FC3W). There are also FC3 devices that are only frequency clock synthesizers, such as the RC22308 and RC22312 (FC3).

The jitter attenuators (JA) consist of inputs, a DPLL to perform the filtering, an APLL, and outputs. The synthesizers (Synth) do not have any inputs or DPLLs; only an APLL and outputs. The parameters for optimizing for low-phase noise will be slightly different for JA mode versus Synth mode. Some commonalities also exist during the optimization process. This document focuses on the commonalities of the devices.

Figure 1 shows a block diagram of an FC3 device (RC32312A) in JA mode.

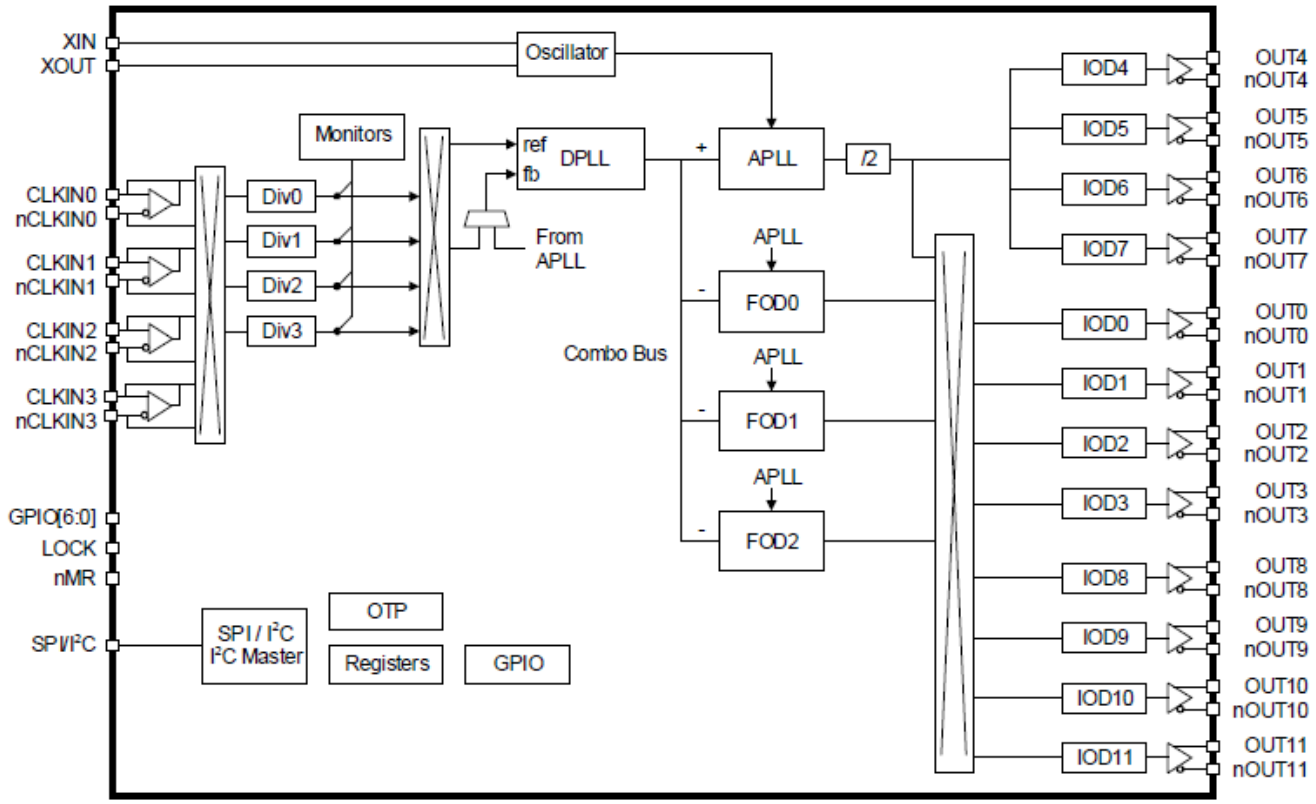

Figure 1. Block Diagram of an FC3 Device

Figure 2 shows a block diagram of an FC3W device (RC38312A) in JA mode.

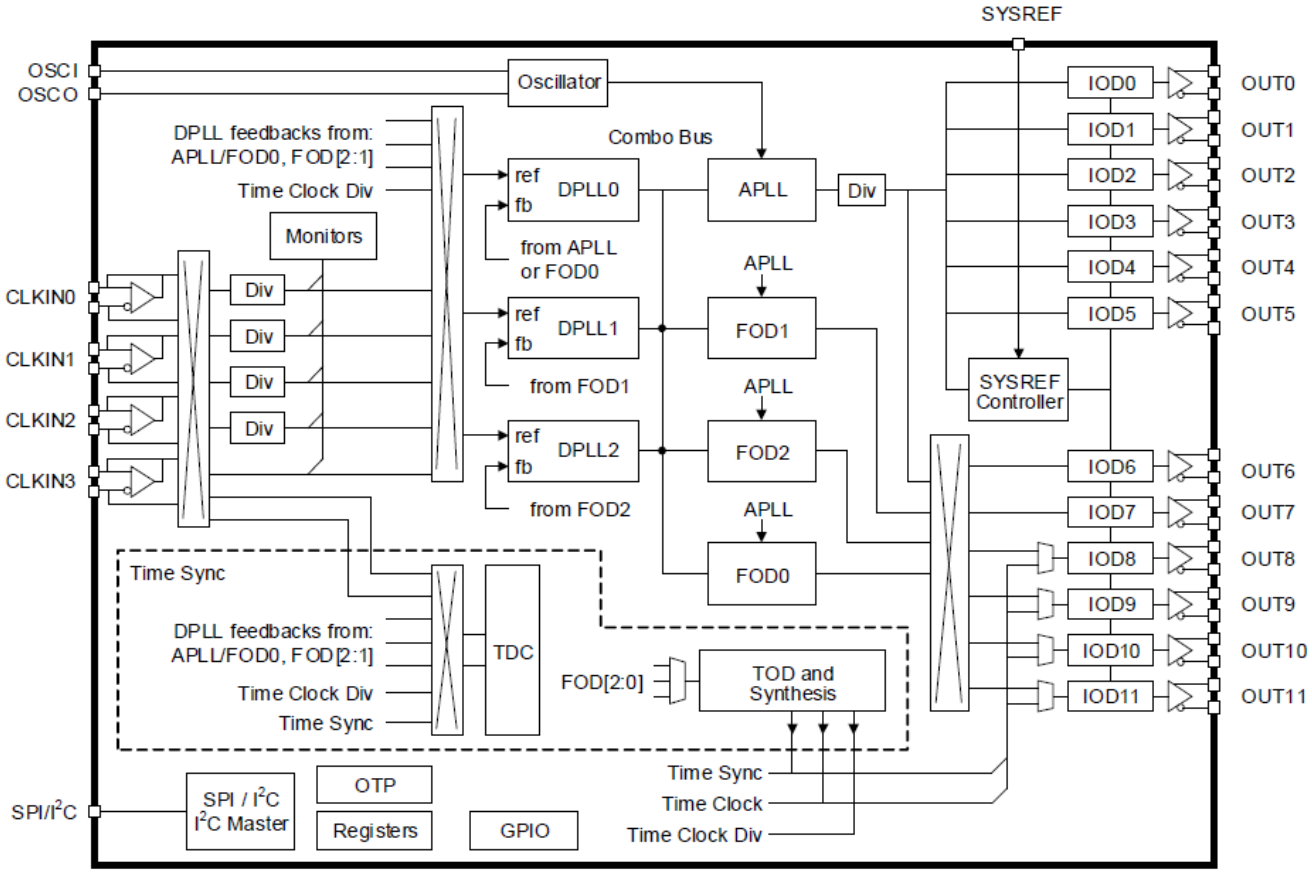

Figure 2. Block Diagram of an FC3W Device

2. XTAL Frequency Selection

Use the following guidelines for choosing the correct XTAL when optimizing for phase noise:

1. Selection to be based upon the device datasheet specifications for Frequency, CL, ESR, and Drivel Level.
2. The higher the XTAL frequency, the better the phase noise. This also helps in filtering out reference feedthrough (a specific type of spur).
3. Choose an appropriate frequency based on the mode, the output frequency plan, and the VCO frequency.
   a. For Synth mode applications, choose a XTAL that **is** an integer multiple of the VCO frequency. For example, VCO = 10GHz, XTAL = 62.5MHz and 50MHz are valid values (62.5MHz is the better value).
   b. For JA mode applications, choose a XTAL that **is not** an integer of the VCO or the output frequency. Also calculate the harmonics to ensure they are outside the integration range of interest. For example, VCO = 10GHz, XTAL = 68MHz.

3. Output Selection

FC3 has Integer Output Dividers (IOD) and Fractional Output Dividers (FOD) as shown in Figure 3. Outputs 4 to 7 are divided by a fixed divide by 2 directly from the APLL followed by the IOD. Outputs 0, 1, 2, 3, 8, 9, 10, and 11 have the option of being divided by 2 from the APLL or to be divided by an FOD, followed by the IOD. These latter outputs also go through a mux before the IOD.

For best phase noise, use Outputs 4 to 7 as they go through the path of least circuitry. If more outputs are necessary, they can be used simultaneously with Outputs 4 to 7 but will have more noise compared to Outputs 4 to 7.

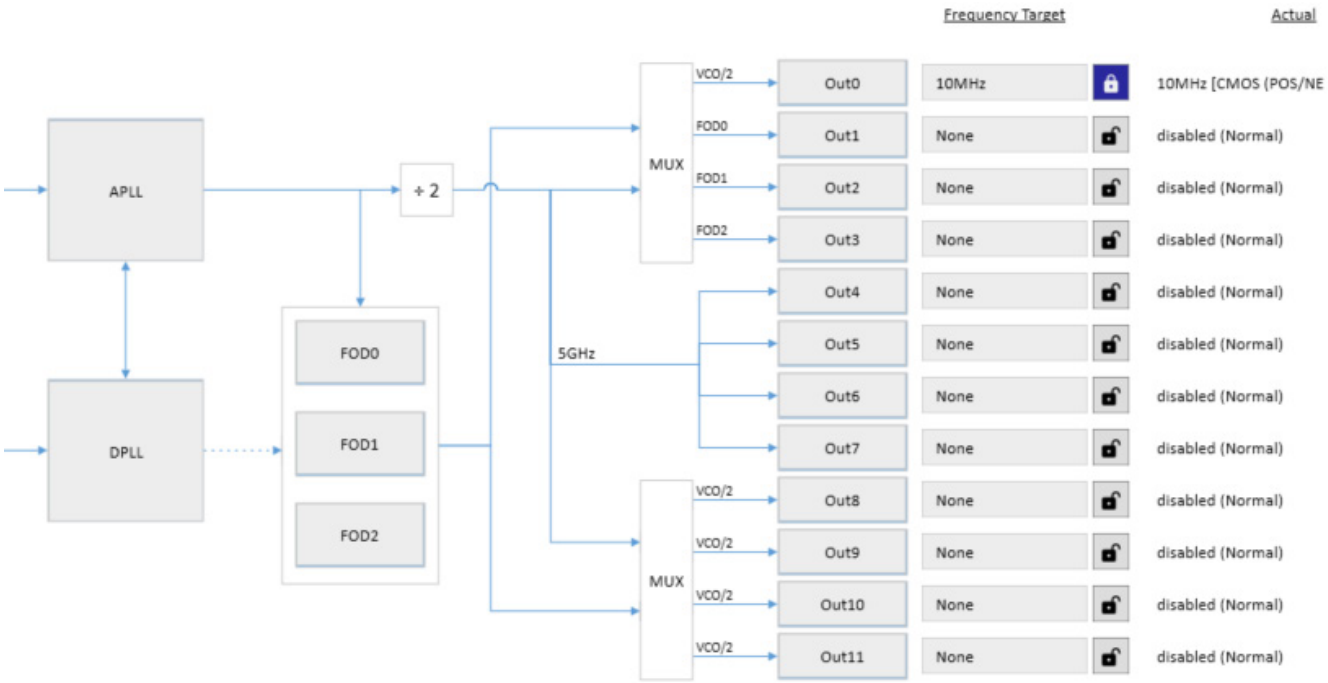

Figure 3. GUI Diagram Showing the Various FC3 Outputs

FC3W also has IODs and FODs (see Figure 4). Outputs 0 to 5 are divided by a fixed divide by 4 directly from the APLL followed by the IOD. Outputs 6 to 11 have the option of being divided by 4 from the APLL or to be divided by an FOD, followed by the IOD. These latter outputs also go through a mux before the IOD.

For best phase noise, use Outputs 0 to 5 as they go through the path of least circuitry. If more outputs are necessary, they can be used simultaneously with Outputs 0 to 5 but will have more noise compared to Output 0 to 5.

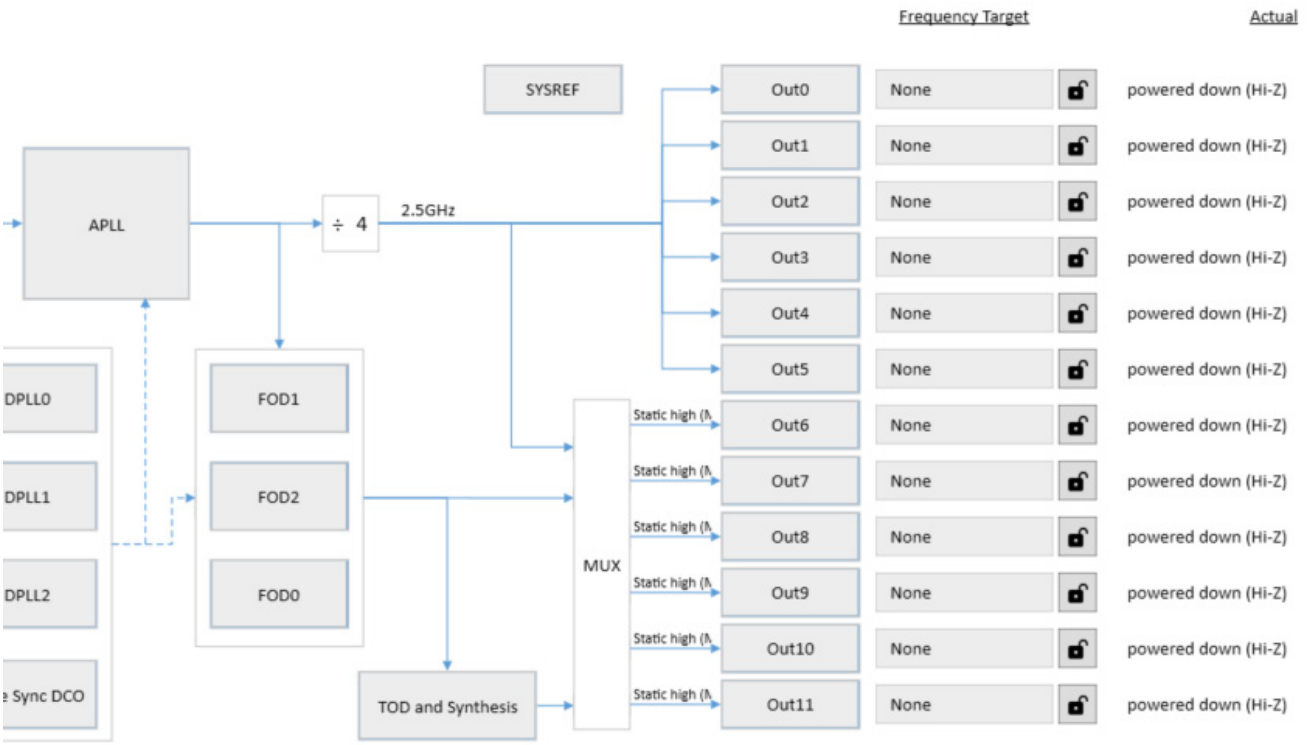

Figure 4. GUI Diagram Showing the Various FC3W Outputs

4. Fractional Output Dividers (FOD)

Fractional output frequencies are sometimes necessary. There are three FODs in FC3/FC3W. To avoid integer boundary spurs using the FODs, the fractional portion of the divide ratio should be between 0.2 and 0.8 as shown in Figure 5. This applies to both FC3 and FC3W. Depending on the configuration, a divide ratio between 0.2 and 0.8 is not guaranteed.

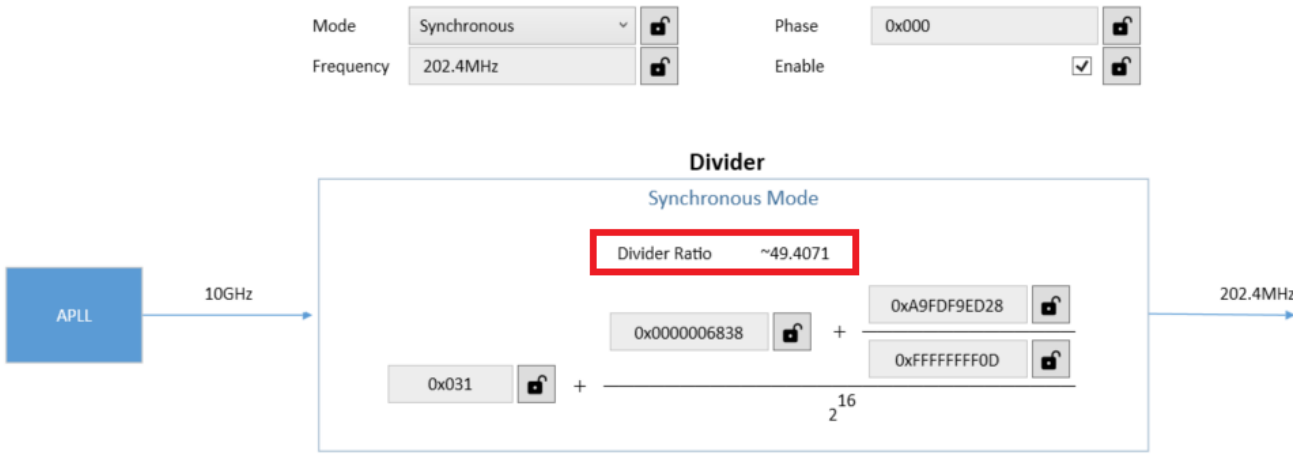

Figure 5. GUI Diagram of the FOD Block Showing the Divider Ratio

5. Shared Power Rails (FC3 only)

Certain outputs and FODs share the same power rail (see Figure 6).

- **Out1** shares power with **FOD0**
- **Out8** shares power with **FOD1**
- **Out10** shares power with **FOD2**

To avoid spurs coupling to other outputs, it is best to associate FOD0 with Out1, FOD1 with Out8, and FOD2 with Out10 whenever possible.

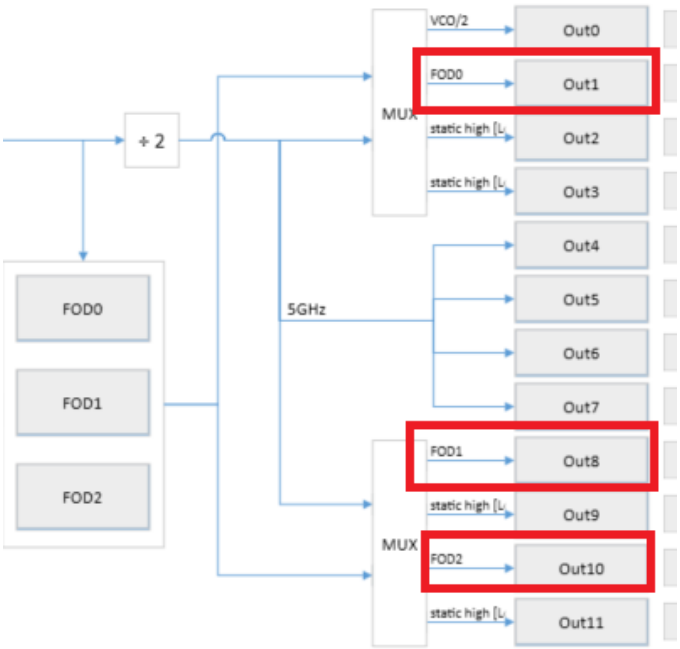

Figure 6. GUI Diagram of the Outputs Associated with the Correct FOD

6. XTAL Coupling to Out0/1 (FC3 only)

FC3 devices have a QFN package, whereas FC3W devices have a BGA package. Due to the XTAL (XIN/XOUT) pad location relative to the Out0/1 pad locations, there is coupling from the XTAL to Out0 and Out1 (see Figure 7). Therefore, unless output/XTAL is an integer relationship and in Synth mode, Out0 and Out1 cannot have sensitive clock outputs.

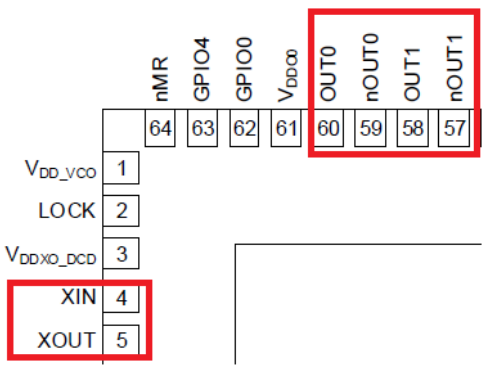

Figure 7. Die Pad Locations for XIN/XOUT, OUT0/nOUT0 and OUT1/nOUT1

7. Output-to-Output Coupling

The outputs of an FC3 QFN package start at the top of the package and then increment serially in clockwise rotation as shown in Figure 8. The location of the outputs gives an indication of where to place certain frequencies to avoid coupling of the fundamental frequency or even the harmonics of adjacent outputs.

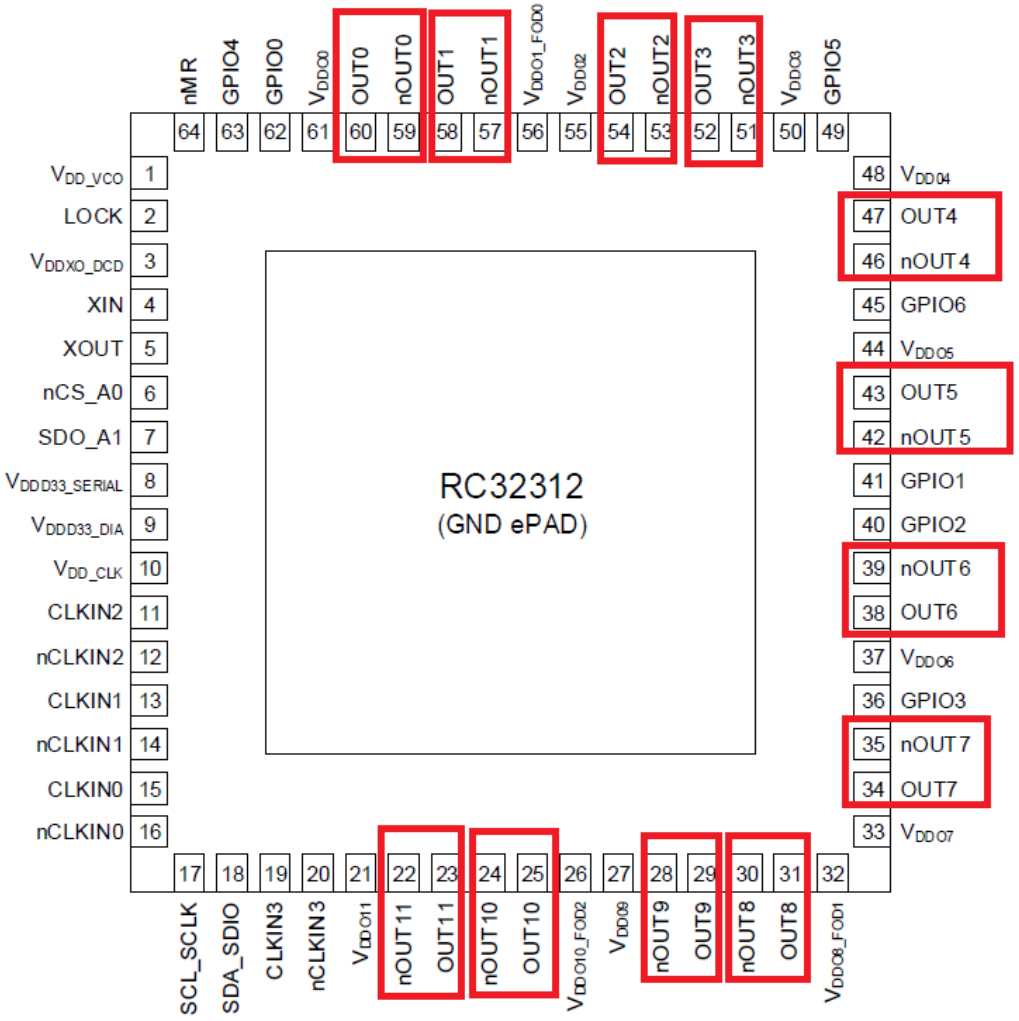

Figure 8. FC3 Die Pad Locations for the Outputs

The outputs of the FC3W BGA package are shown in Figure 9. The outputs start at the top of the package and then increment serially in counter-clockwise rotation. Similarly to FC3, the location of the outputs gives an indication of where to place certain frequencies to avoid coupling of the fundamental frequency or even the harmonics of adjacent outputs.

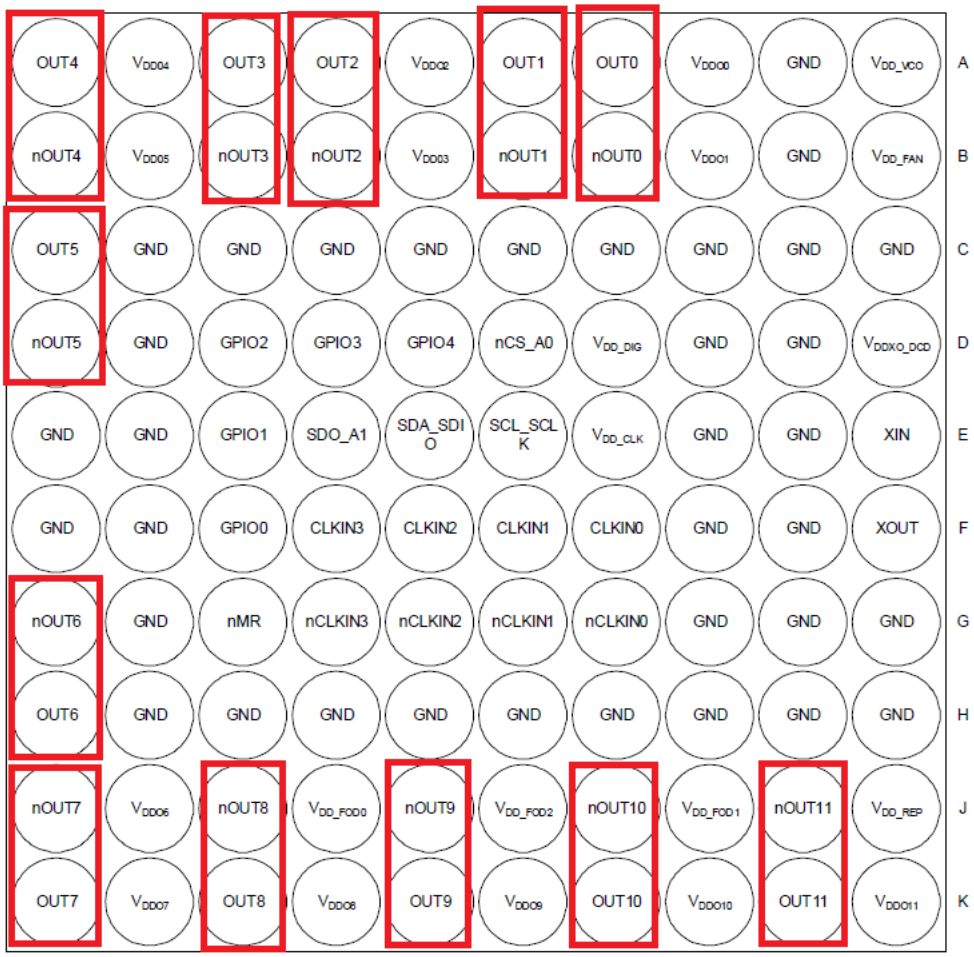

Figure 9. FC3W Die Pad Locations for the Outputs

8. FC3 Synthesizer Configuration Example

Due to the similarities between FC3 and FC3W, only an FC3 example is shown below.

The GUI configuration was created with the following details:

- XTAL = 62.5MHz
- 2x 25MHz LVCMOS
- 2x 50MHz LVDS
- 4x 312.5MHz HCSL
- 2x 156.25MHz HCSL
- 2x 100MHz HCSL

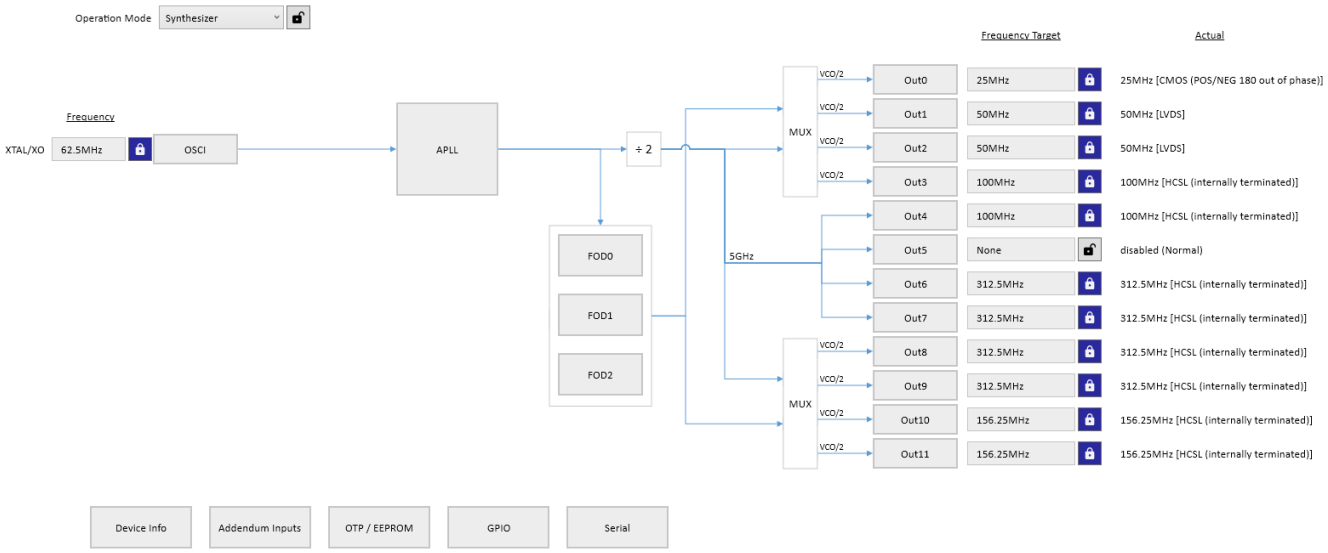

Figure 10. GUI Diagram of the Synthesizer Configuration Example

As shown in Figure 10, an APLL VCO frequency of 10GHz was auto-calculated because it is a multiple of 62.5MHz. In Synthesizer mode, the best phase noise is achieved when the VCO frequency is a multiple of the XTAL frequency.

All the outputs are common factors of 10GHz and use a divide-by-2 followed by an IOD. If they were not common factors of 10GHz, the FODs would need to be used. FODs give higher jitter and can cause additional spurs. Outputs 0 to 3 and Outputs 8 to 11 go through an additional mux that Outputs 4 to 7 do not see, so higher jitter is expected.

Outputs 0 and 1 are not multiples of the XTAL frequency, therefore, coupling occurs due to the fact that the input pads are close to each other.

Also notice how 25MHz, 50MHz, and 100MHz are grouped in the top half of the outputs, whereas 156.25MHz and 312.5MHz are grouped in the bottom half of the outputs. This is to separate groups of multiples to avoid crosstalk. For example, 156.25MHz - 3 × 50MHz = 6.25MHz. This produces a 6.25MHz spur on the 156.25MHz and 312.5MHz outputs due to harmonic coupling.

For the phase noise plots, see Figure 11 (25MHz output), Figure 12 (100MHz output), Figure 13 (156.25MHz output) and Figure 14 (312.5MHz output)

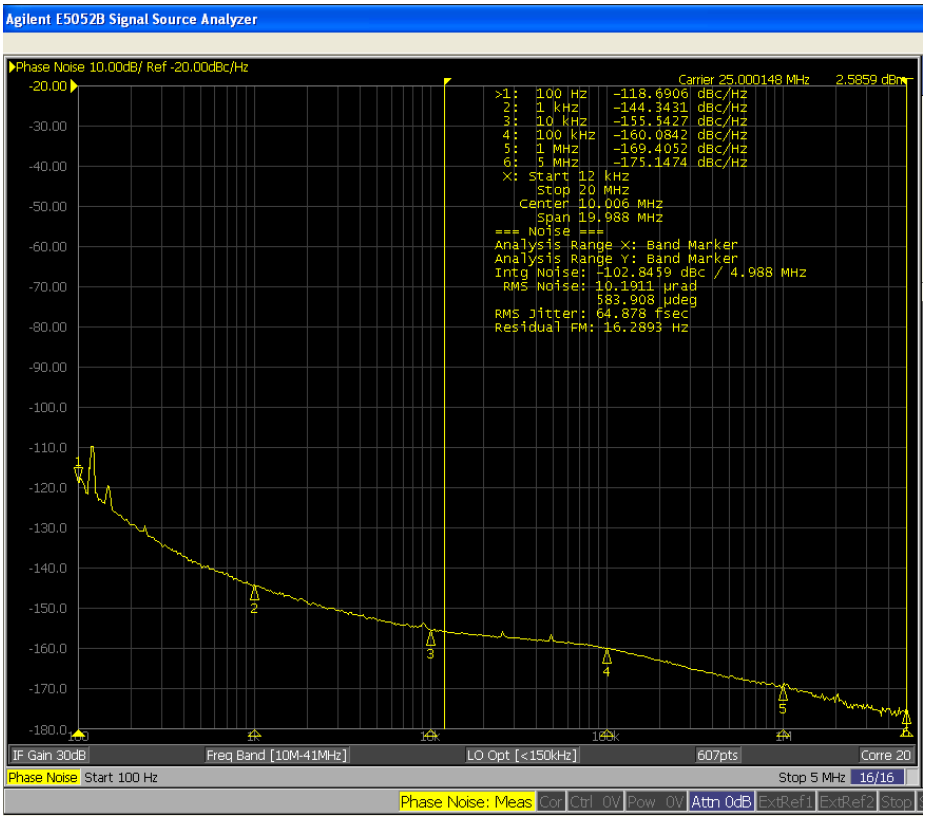

Figure 11. Phase Noise Plot of 25MHz Output

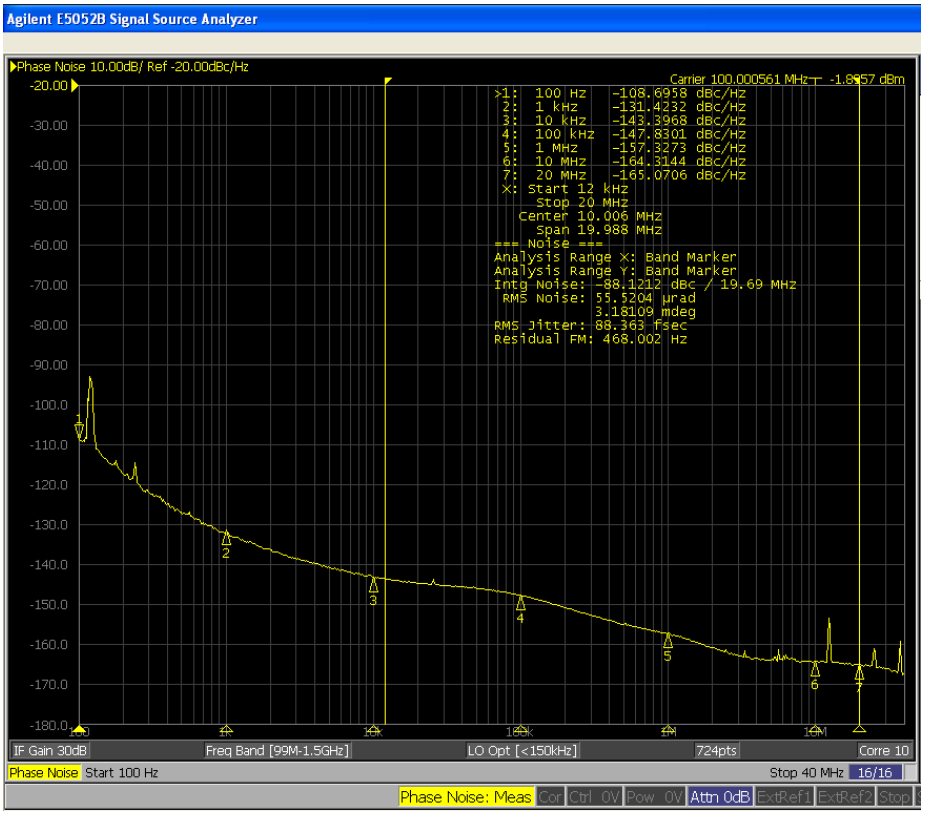

Figure 12. Phase Noise Plot of 100MHz Output

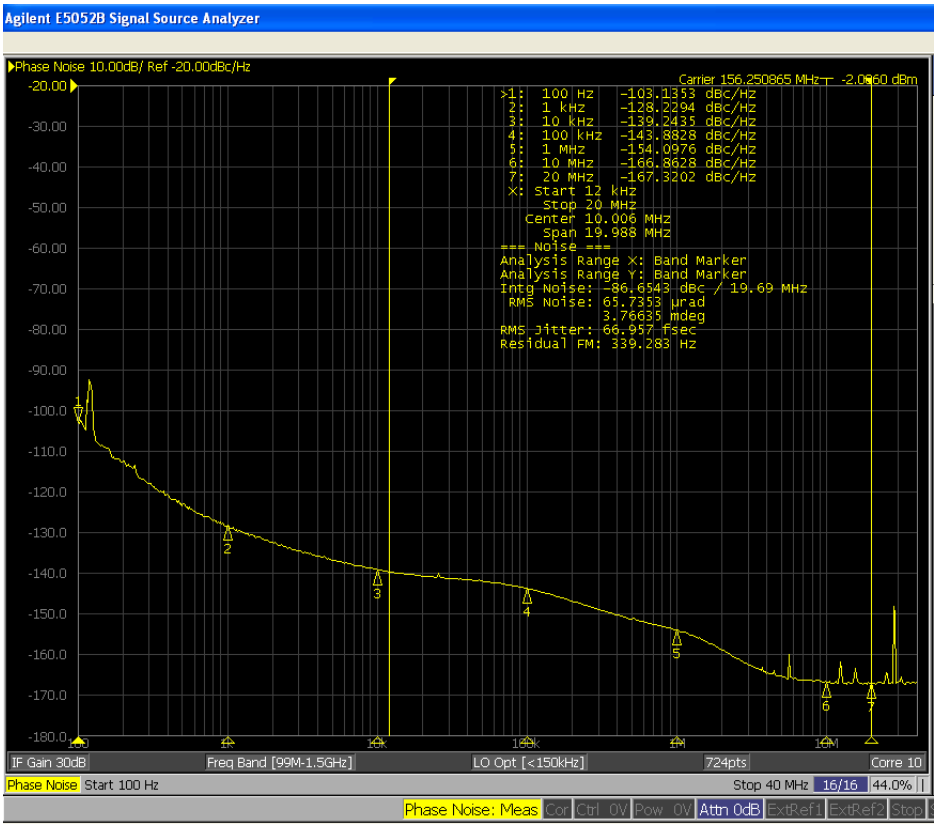

Figure 13. Phase Noise Plot of 156.25MHz Output

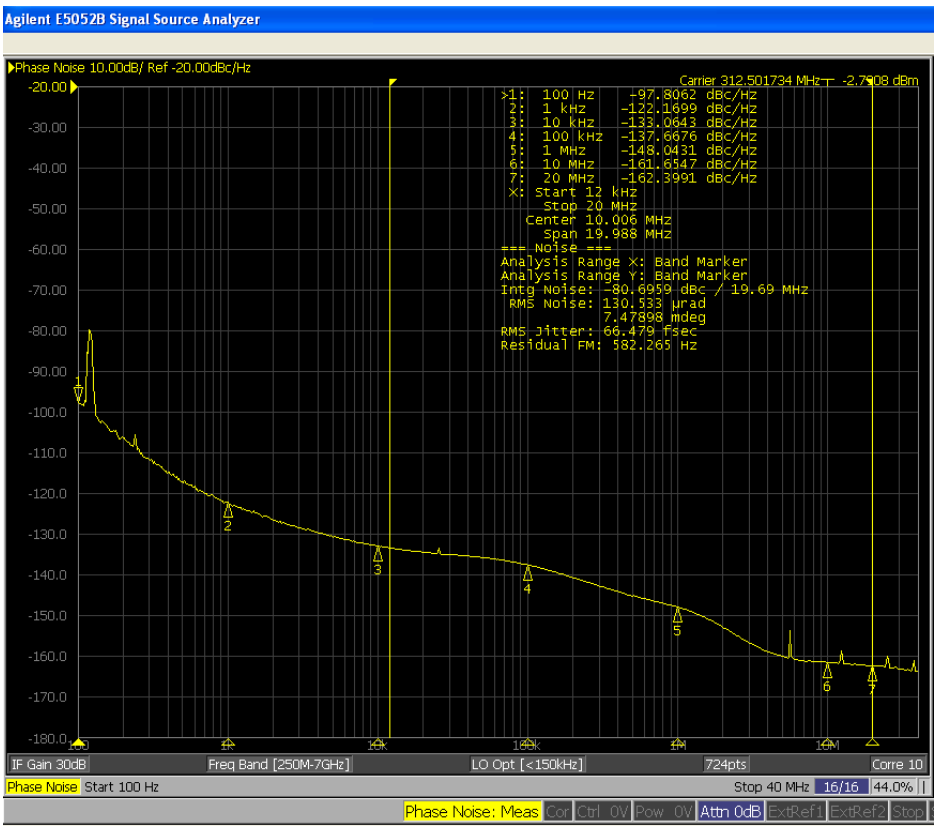

Figure 14. Phase Noise Plot of 312.5MHz Output

9. Revision History

Revision	Date	Description
1.00	Jun 3, 2024	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.