Clock Behavior on Startup and Power Up/Down
SLG47910

Abstract

This application shows how to behave OSC, PLL, and Logic-As-Clock under initial startup, power-up, power-down conditions and at different registers configurations. This application note comes complete with designs files which can be found in the References section.

Contents

1. Terms and Definitions

FPGA	Field Programmable Gate Array
FPGA Editor	Main FPGA design and simulation window
Go Configure Software Hub	Main window for device selection
ForgeFPGA Window	Main FPGA project window for debug and IO programming
OSC	Oscillator
PLL	Phase Locked Loops
LaC	Logic-As-Clock

2. References

For related documents and software, please visit: ForgeFPGA Low-density FPGAs | Renesas.

Download our free ForgeFPGA™ Designer software [1] to open the .ffpga designs files [2] and view the proposed circuit design.

[1] Go Configure Software Hub | Renesas

[2] AN-FG-019 Clock behaviour on startup and power updown.ffpga, Designs file

[3] SLG47910 Datasheet, Renesas Electronics

Author: Oleg Horodechnyi: Application Engineering Team Lead, Renesas Electronics

3. Introduction

The SLG47910 has 3 types of clocks sources: Oscillator Clock, PLL Clock and Logic-As-Clock 0/1. This application note focuses on how the clock outputs behave at different conditions and register configurations.

We will be using examples of a simple Frequency Divider to showcase each block frequency output behavior. In the first example design, we are using the OSC and PLL blocks Figure 1 and in the second example design, we are using the LaC0 and LaC1 blocks Figure 2.

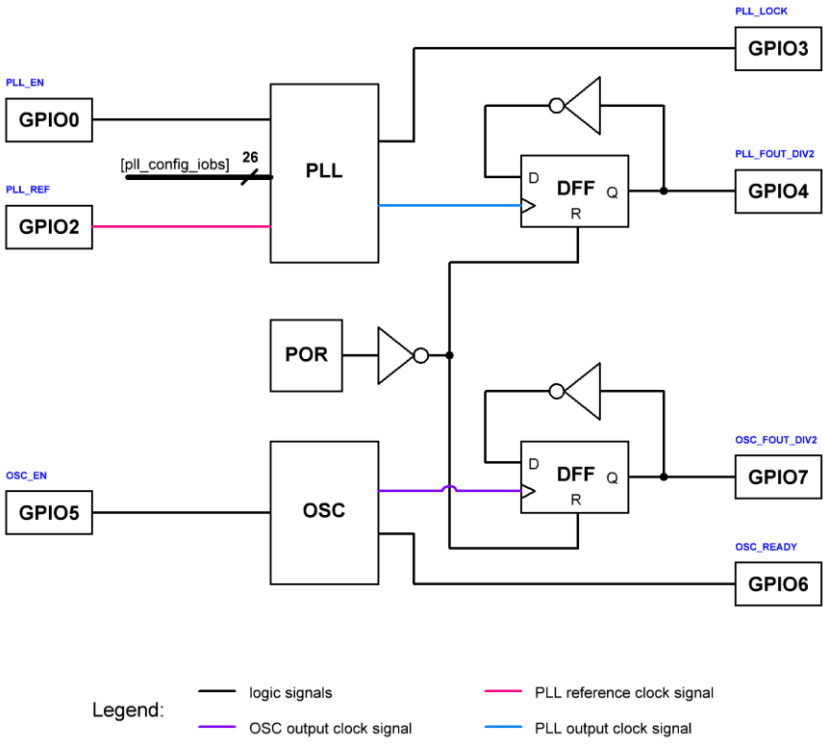


Figure 1: OSC and PLL design block diagram

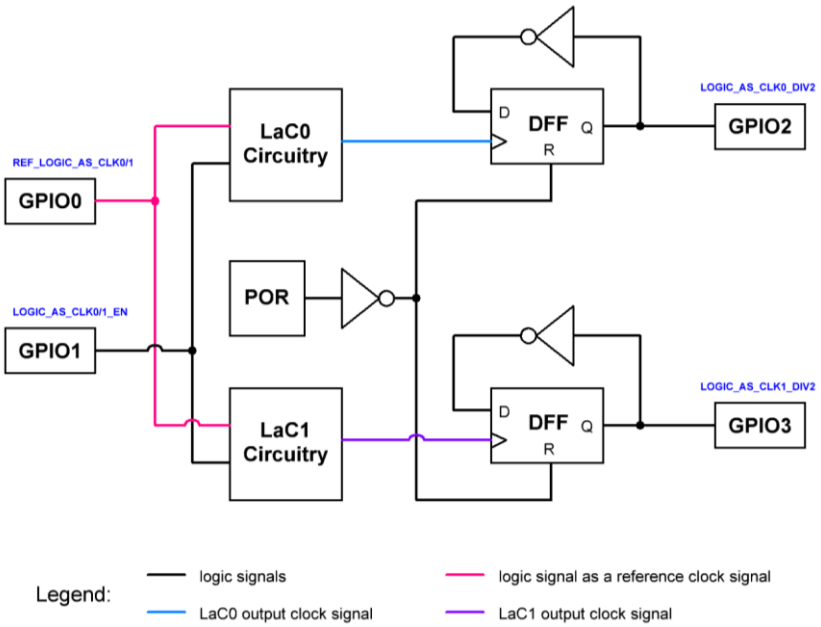


Figure 2: LaC design block diagram

Both designs are using power control signals (OSC_EN, PLL_EN, LOGIC_AS_CLK0/1_EN), reference clock signals for PLL block (PLL_REF) and LaC0/1 blocks (REF_LOGIC_AS_CLK0/1) and frequency output signals that

are divided by two (OSC_FOUT_DIV2, PLL_FOUT_DIV2, LOGIC_AS_CLK0_DIV2 and LOGIC_AS_CLK1_DIV2). The first design also uses status signals (PLL_LOCK, OSC_READY).

4. Ingredients

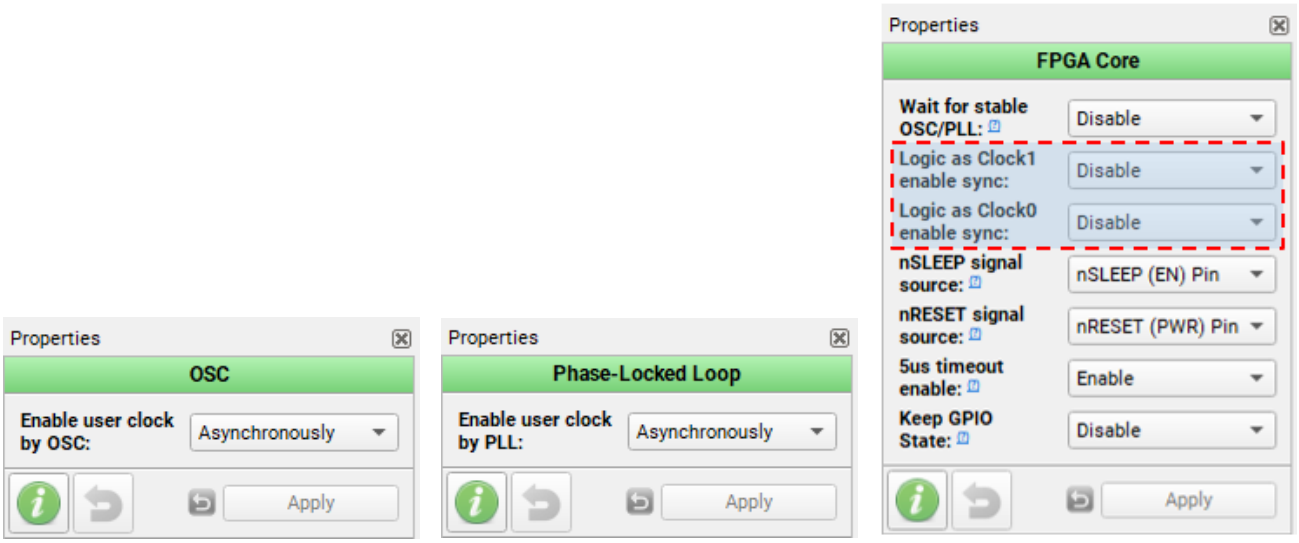
- ForgeFPGA Device SLG47910V
- Latest Revision of ForgeFPGA Workshop software
- SLG47910 Development Board and Adaptor Board

5. Functionality Overview

In the clock signal blocks properties (See Figure 3), you have options (See Figure 4) called "Enable user clock by OSC/PLL" which has two values: Asynchronously and Synchronously and the option called “LaC0/LaC1 enable sync” which has two values: Disable and Enable. Both options have the same behavior Disable is the same as Asynchronously and Enable the same as Synchronously.

The primary purpose of this setting is to turn off the clock source blocks properly. Those blocks should be turned off synchronously, an asynchronous turning off is not recommended because it may cause metastability on the clock line.

There are two ways to turn off clock blocks synchronously. The first way is to disable a block from the same clock domain. In this case, we use the asynchronous/disable option in the block settings (Figure 4 a) and c) images). The second way is to disable a block from another clock domain or by combinatorial logic or externally by GPIO, we should use the synchronous/enable option in the block settings (Figure 4 b) and d) images).



a) b) c)

Figure 3: Blocks Properties panels,

a) OSC properties, b) OSC properties, c) LaCs properties (in a filled rectangle)

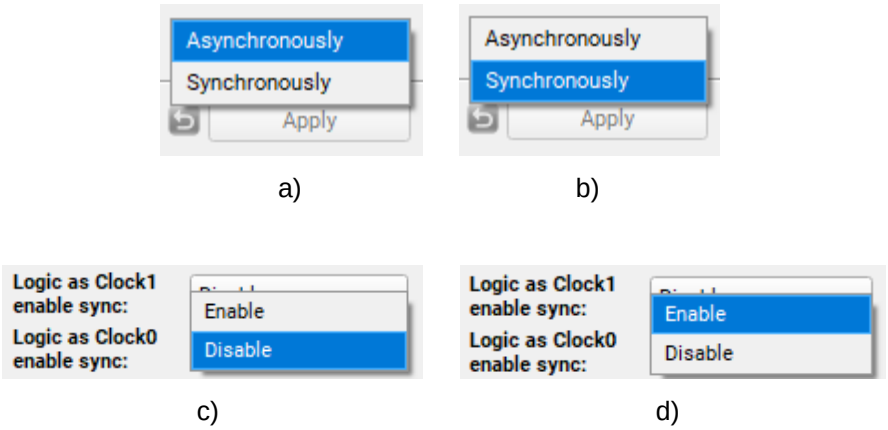


Figure 4: Blocks Properties panels,

a) OSC properties, b) OSC properties, c) LaCs properties (in a filled rectangle), d) LaCs properties

Figure 5, Figure 6, Figure 7 and Figure 8 show the behavior of the blocks under different conditions, namely when the FPGA first loads, when it enters the sleep mode, and when the chip is reconfigured after reset mode.

The main point to pay attention to is that when the blocks are first turned on at the ‘Asynchronously’ option or the ‘Disable’ option, after the first start of the FPGA or after a reset, the frequency at their outputs will appear after an additional two clock cycles on the reference. When all the following blocks turn on, the output frequency appears immediately. When the blocks are turned off, the clock signal at the outputs stops immediately after the falling edge clock signal, and this happens under any conditions. At the ‘Synchronously’ option or the ‘Enable’ option, the output frequency of the blocks will appear after an additional two clock cycles on the reference under any conditions and blocks power cycles.

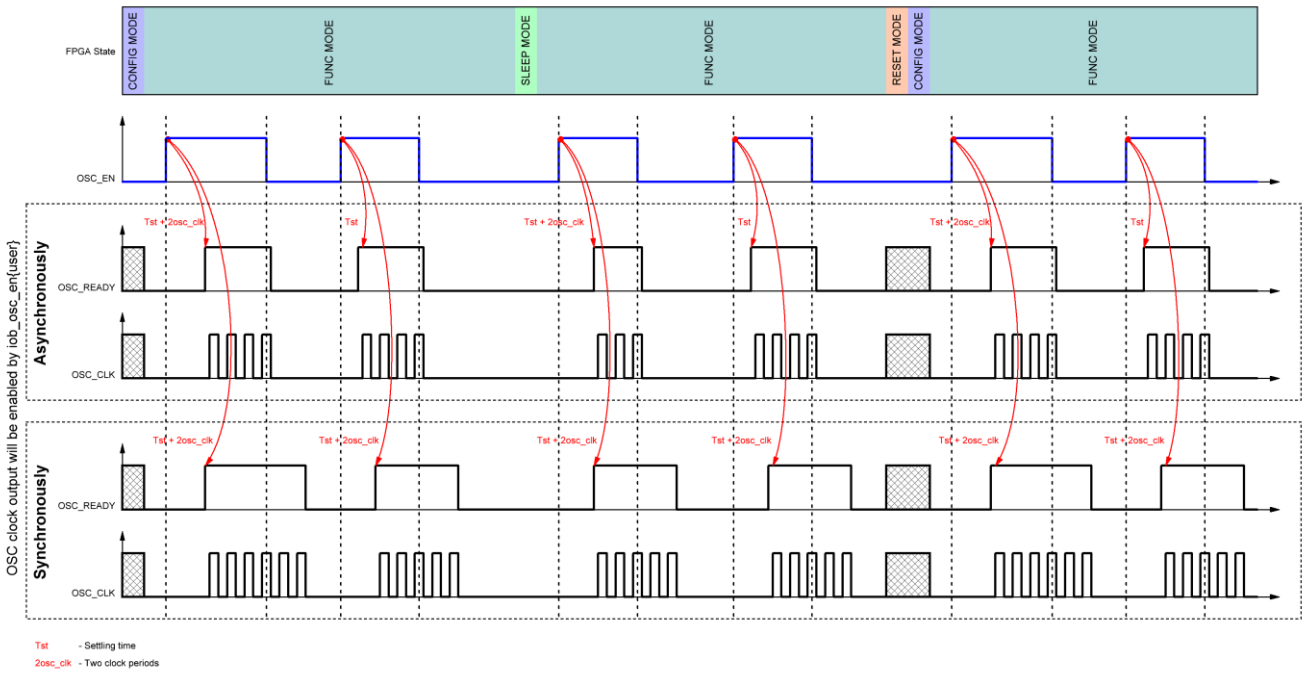


Figure 5: OSC behavior

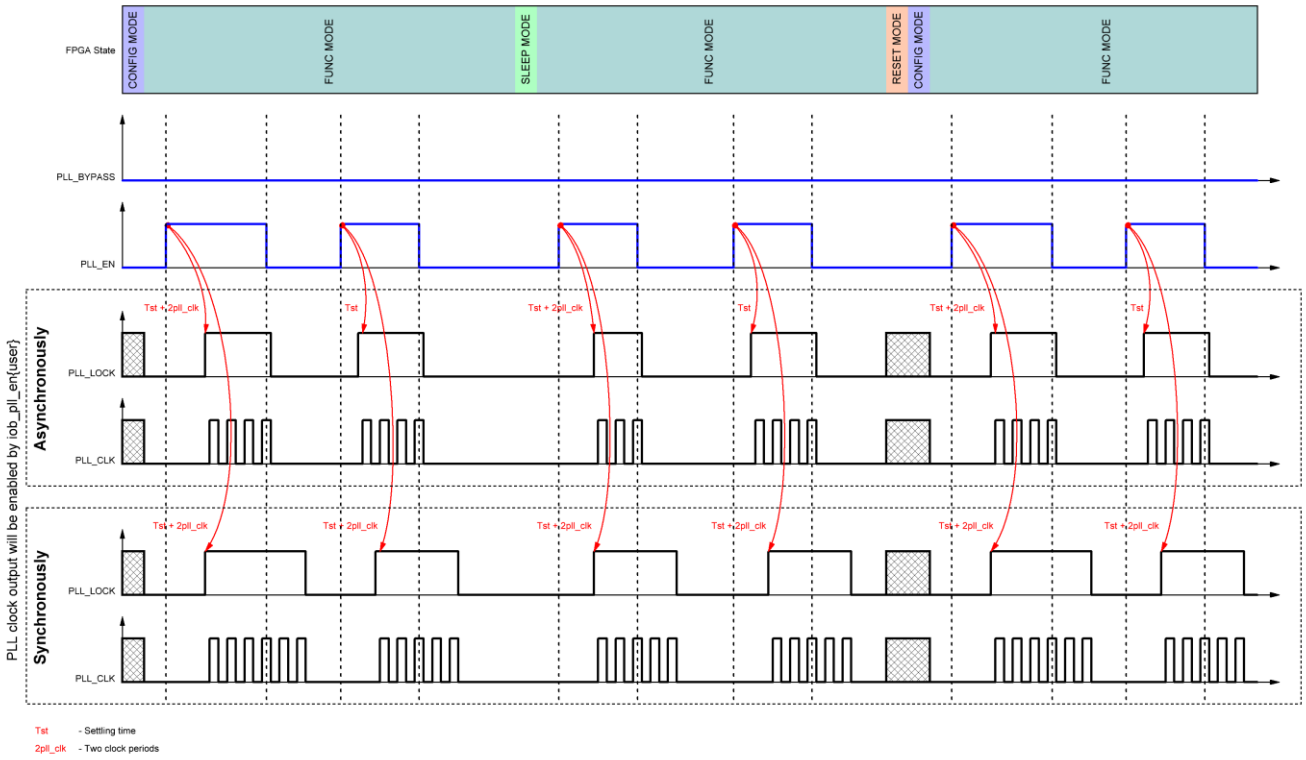


Figure 6: PLL behavior in VCO mode

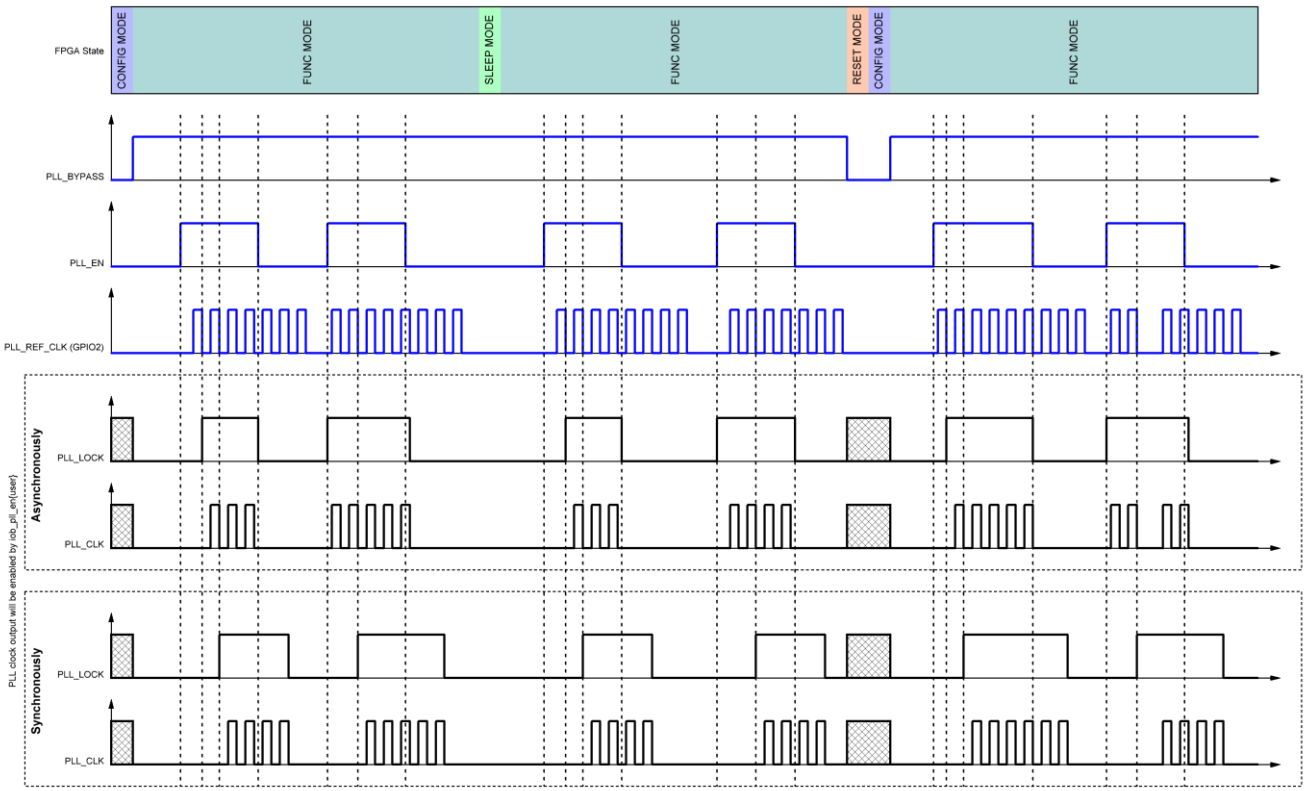


Figure 7: PLL behavior in bypass mode

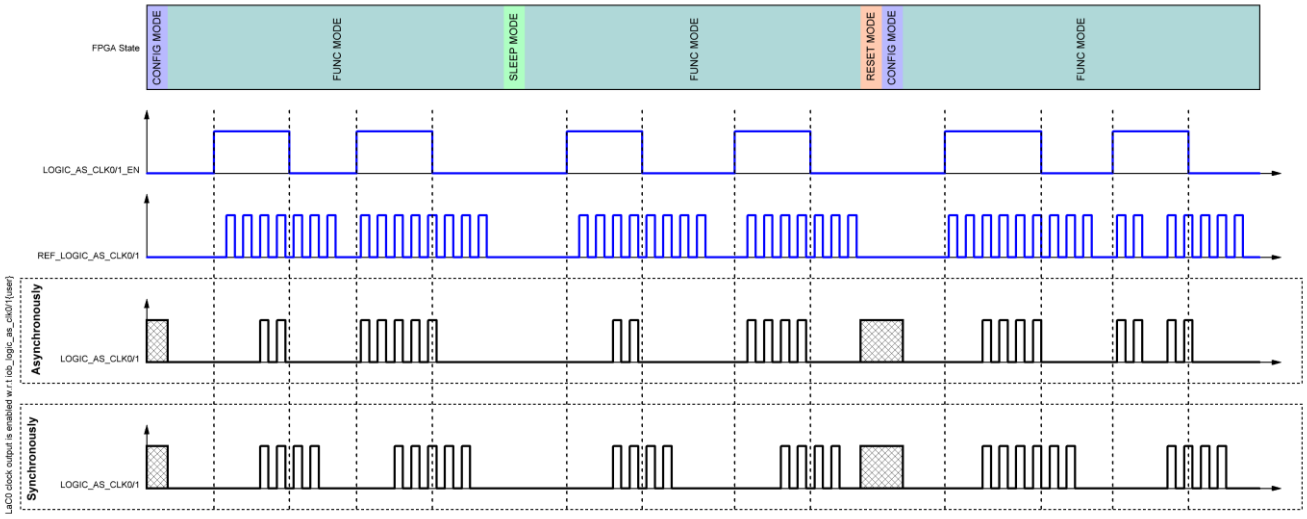


Figure 8: LaC blocks behavior

6. Conclusion

This application note shows how the OSC, PLL, and LaC0/1 behave under different conditions, and it will help with the correct implementation of designs. Understanding the principle of operation of clock signal blocks will help you understand how to build a project that uses a communication interface when the interface clock signal is used as a reference clock for the FPGA. If interested, please contact the ForgeFPGA Business Support Team.

7. Revision History

Revision	Date	Description
1.00	Apr 14, 2025	Initial release.