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H8S/2200 Series

Mode Transition

Introduction

The power-down mode switching function switches among the high-speed mode, medium-speed mode, subactive mode, sleep mode, subsleep mode, watch mode, and software standby mode.

Target Device

H8S/2238

Contents

1. Overview

The switching function of H8S/2238 low-power consumption mode switches among the high-speed mode, medium-speed mode, subactive mode, sleep mode, subsleep mode, watch mode, and software standby mode. Besides these modes, the module stop mode and hardware standby mode are available but they are not explained in this application note. For details, see the Hardware Manual.

2. Configuration

Figure 1 shows the confirmed configuration of this application note.

List of Components Used

No.	Component	Specifications
1	HSB8S2238F H8S/2238 CPU board (HOKUTO DENSHI CO., LTD.)	Board power supply input: 3 to 5 VDC Operating frequency: Main 12.2880 MHz Sub 37.768 kHz MCU operating mode: 7 (Single-chip mode)

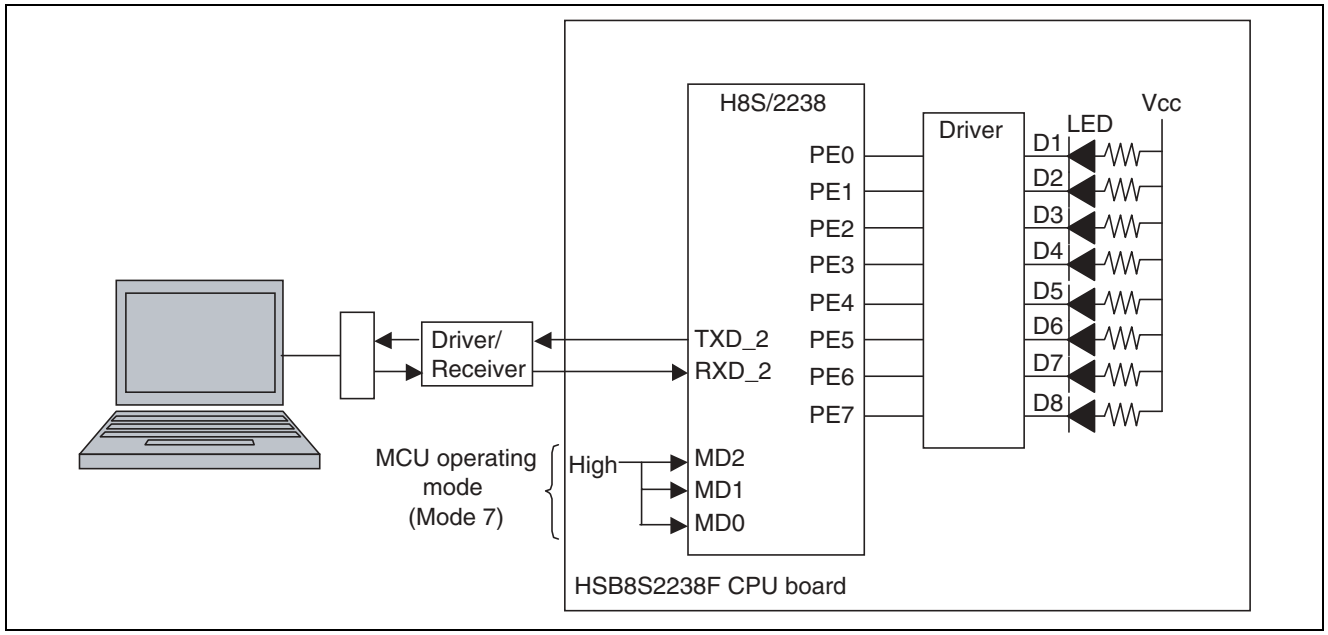


Figure 1 Confirmed Configuration

3. Description of Functions

The transition mode starts by inputting a command from the terminal software connected to the RS-232C interface.

1. Communication specifications
   The terminal software is connected to the specifications below.

Communication method	Asynchronous
Bit rate	38400 bps
Data size	8 bits
Parity	None
Stop bit	1 bit
Terminating code	Line feed

2. Supported functions

No.	Function	Specifications
1	High-speed ↔ transition to medium-speed mode	Format: m1Δ(Transition mode) (Transition mode) Transition mode Settings 0 High-speed mode 1 Medium-speed mode ϕ/2 2 Medium-speed mode ϕ/4 3 Medium-speed mode ϕ/8 4 Medium-speed mode ϕ/16 5 Medium-speed mode ϕ/32
2	High-speed/medium-speed mode → Transition to subactive mode → Return to high-speed/medium-speed mode	Format: m2Δ(Return mode) (Return mode) Return mode Settings 0 High-speed mode 1 Medium-speed mode ϕ/2 2 Medium-speed mode ϕ/4 3 Medium-speed mode ϕ/8 4 Medium-speed mode ϕ/16 5 Medium-speed mode ϕ/32

No.	Function	Specifications
3	High-speed/medium-speed mode → Transition to the specified halt state → Release of program halt state by interrupt → Return to the specified mode	Format: m3Δ(Halt mode)Δ(Return mode) Halt mode Settings / Halt transition mode 0 / Sleep mode 1 / Software standby mode 2 / Watch mode (Return mode) Settings / Return mode 0 / High-speed mode 1 / Medium-speed mode ϕ/2 2 / Medium-speed mode ϕ/4 3 / Medium-speed mode ϕ/8 4 / Medium-speed mode ϕ/16 5 / Medium-speed mode ϕ/32 6 / Subactive mode
4	High-speed/medium-speed mode → Transition to subactive mode → Transition to the specified halt state → Release of program halt state by interrupt → Return to the specified mode	Format: m4Δ(Halt mode)Δ(Return mode) Halt mode Settings / Halt transition mode 2 / Watch mode 3 / Subsleep mode (Return mode) Settings / Return mode 0 / High-speed mode 1 / Medium-speed mode ϕ/2 2 / Medium-speed mode ϕ/4 3 / Medium-speed mode ϕ/8 4 / Medium-speed mode ϕ/16 5 / Medium-speed mode ϕ/32 6 / Subactive mode

4. Principles of Operation

4.1 Initial Setting

Before exercising DTC control, start up the microcomputer and perform the initial setting of internal resister and other operations as needed.

1. Control of the low-power consumption, initialization of the clock oscillator

Register name ←Set value	Bit	Name	Value	Contents
LPWCR ←0x03	7	DTON	0	Directly transfer on flag
	6	LSON	0	Low-speed on flag
	5	NESEL	0	Sampling frequency (use of ϕ/32)
	4	SUBSTP	0	Operates the subclock oscillator
	3	RFCUT	0	Uses the internal feedback resistance control
	2	----	0	
	1:0	STC[1:0]	11	Bypasses the PLL
MSTPCRA ←0x8C	7	MSTPA7	1	(Reserved)
	6	MSTPA6	0	Operates DTC module
	5	MSTPA5	0	Operates the TPU module
	4	MSTPA4	0	Operates the TMR_0 and 1 modules
	3:2	MSTPA[3:2]	11	(Reserved)
	1	MSTPA1	0	Operates the AD module
	0	MSTPA0	0	Operates the TMR_2 and 3 modules
MSTPCRB ←0x1F	7	MSTPB7	0	Operates the SCI0 module
	6	MSTPB7	0	Operates the SCI1 module
	5	MSTPB7	0	Operates the SCI2 module
	4:0	MSTPB[4:0]	1111	(Reserved)
MSTPCRC ←0x4F	7	MSTPC7	0	Operates the SCI3 module
	6	MSTPC6	1	(Reserved)
	5	MSTPC5	0	Operates the DA module
	4	MSTPC4	0	Operates the PC break controller
	3:0	MSTPC[3:0]	11111	(Reserved)

2. Initialization of IO port
   Set the input/output pins of port E and F as below. Set all other pins to the output mode.

Port	Register name ←Set value	Bit	Name	Value	Contents
E	PEDDR ←0xFF	7:0	PE[7:0]DDR	all"1"	Output (LED control)
	PEDR ←0xFF	7:0	PE[7:0]DR	all"1"	Delete All LEDs
F	PEDDR ←0Xf6	7:4	PF[7:4]DDR	all"1"	Output (Not used)
		3	PF3DDR	0	Input (IRQ3)
		2:1	PF[2:1]DDR	all"1"	Output (Not used)
		0	PF0DDR	0	Input (IRQ2)

3. Initialization of the TPU0 timer
   Set the timer to be able to interrupt at every 100 ms for monitoring.

Register name ←Set value	Bit	Name	Value	Contents
TCR_0 ←0x23	7:5	CCLR[2:0]	001	Counter clear by the TGRA compare match
	4:3	CKEG[1:0]	00	Count with rising edge
	2:0	TPSC[2:0]	011	Count with ϕ/64
TMDR_0 ←0x00	7:6	----	00	
	5	BFB	0	Normal TGRB operation
	4	BFA	0	Normal TGRA operation
	3	----	00	
	2:0	MD[2:0]	000	Normal operation
TIORH_0 ←0x00	7:4	IOB[3:0]	0000	TBRB output compare (Not used)
	3:0	IOA[3:0]	0000	TBRA output compare
TIORL_0 ←0x00	7:4	IOD[3:0]	0000	TBRD output compare (Not used)
	3:0	IOC[3:0]	0000	TBRC output compare (Not used)
TIER_0 ←0x00	7	TTGE	0	Disables AD conversion start request. (Not used)
	6	----	0	
	5	TCIEU	0	Disables underflow interrupt. (Not used)
	4	TCIEV	0	Disables overflow interrupt. (Not used)
	3	TGIED	0	Disables TGRD interrupt. (Not used)
	2	TGIEC	0	Disables TGRC interrupt. (Not used)
	1	TGIEB	0	Disables TGRB interrupt. (Not used)
	0	TGIEA	0	Enables TGRA interrupt.
TGRA_0 ←19230	15:0	TGRA_0	19230	TBRA output compare value (To be set to interrupt at every 100 ms)
TCNT_0 ←0x0000	15:0	TCNT_0	0x0000	Counter clear
TSTR ←0x01	7:0	TSTR	0x01	Start TCNT_0 counter

4. Initialization of serial interface (SCI_2)
   Set the interface to connect to the terminal software for starting up DTC.

Register name ←Set value	Bit	Name	Value	Contents
SCR_2 ←0x00	7	TIE	0	Disables transmit interrupt.
	6	RIE	0	Disables receive interrupt.
	5	TE	0	Disables transmit operation.
	4	RE	0	Disables receive operation.
	3	MPIE	0	Disables multi-processor interrupt.
	2	TEIE	0	Disables transmit end interrupt.
	1:0	CKE[1:0]	00	Asynchronous, use internal clock
	7	TIE	0	Disables transmit interrupt.
SMR_2 ←0x00	7	C/A	0	Asynchronous mode
	6	CHR	0	8-bit length
	5	PE	0	No parity check.
	4	O/E	0	Even parity (Not used)
	3	STOP	0	One stop bit
	2	MP	0	Disables the multi-processor communication function.
	1:0	CKS[1:0]	00	Clock source = ϕ
SCMR_2 ←0x00	7:4	----	0000	
	3	DIR	0	LSB first
	2	INV	0	No data inversion
	1-0	----	00	
BRR ←9	7:0	BRR	9	Sets the transmission speed to 38400 bps.

— Await for at least one-stop bit. (38400 bps: About 30 μs)
— Enables the receive processing.

Register name (Address←Set value)	Bit	Name	Value	Contents
SCR_2 ←0x50	7	TIE	0	Disables transmit interrupt.
	6	RIE	1	Enables receive interrupt.
	5	TE	0	Disables transmit operation.
	4	RE	1	Enables receive operation.
	3	MPIE	0	Disables multi-processor interrupt.
	2	TEIE	0	Disables transmit end interrupt
	1:0	CKE[1:0]	00	Asynchronous, use internal clock

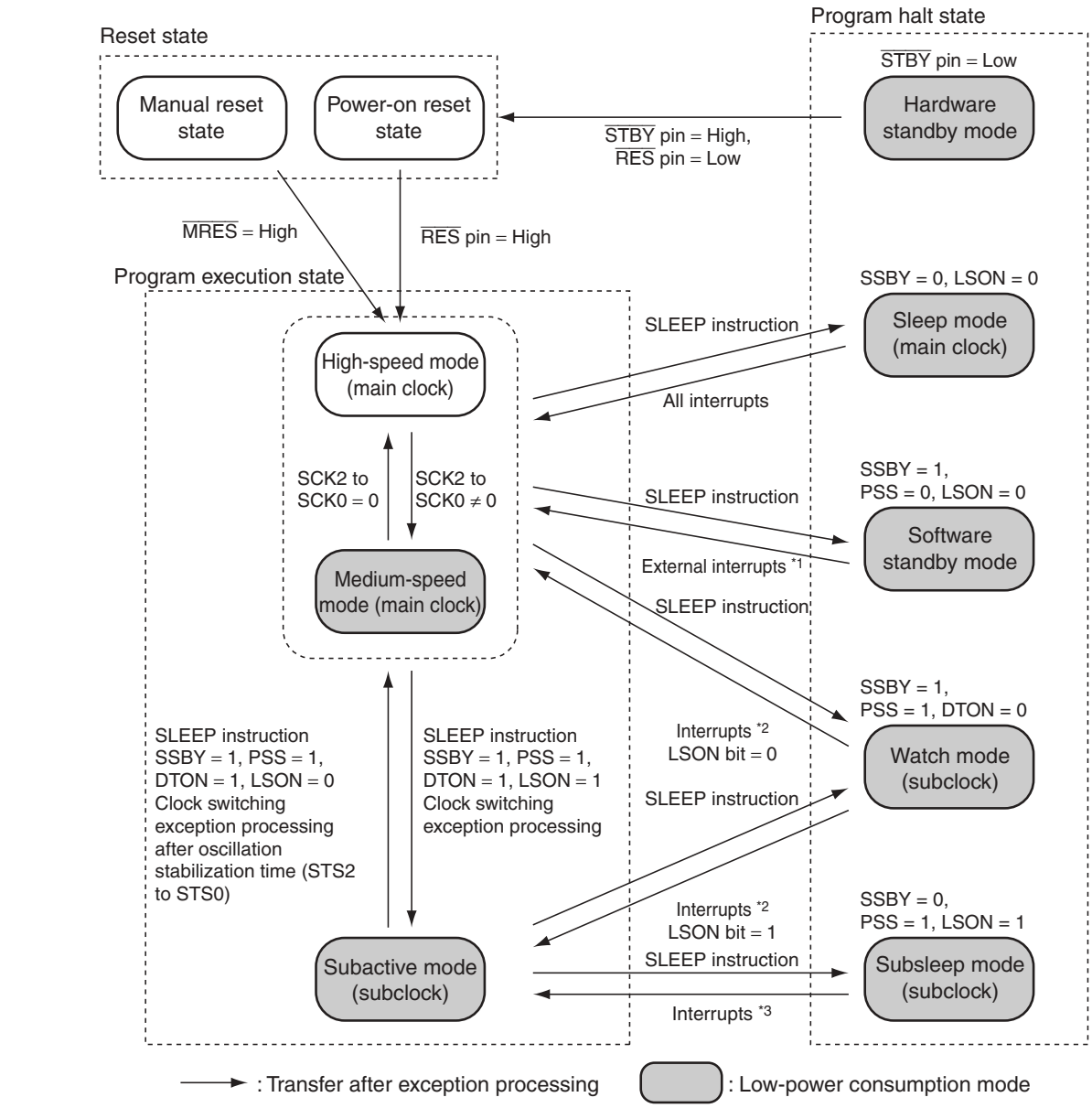
4.2 Mode Transition

Figure 2 shows possible transitions between modes. The SLEEP instruction instructs the transition from the program execution state to the program halt state. An interrupt instructs a return from the program halt state to the program execution state.

You can switch the high-speed mode to the medium-speed mode or vice versa (both modes are the program execution) simply by changing bit 2 (SCK2) to bit 0 (SCK0) in the SCKCR register.

You can also directly switch the high-speed or medium-speed mode to subactive mode without halting program execution.

Table 1 shows transitional conditions for each mode when the SLEEP instruction is executed. The table also shows states of return by interrupts. Table 1 shows the LSI internal states in each operating mode.



Notes: *1 NMI, IRQ0 to IRQ7, and WDT1 interrupt
*2 NMI, IRQ0 to IRQ7, WDT0 interrupt and WDT1 interrupt
*3 NMI and IRQ0 to IRQ7 interrupt

- Only the occurrence of an interrupt source prevents the triggering of transition between modes. Be sure that an interrupt request has been accepted before performing interrupt processing.
- When the RES pin is driven low in all states other than the hardware standby mode, the current state switches to the reset state. When the MRES pin is driven low in all states other than the hardware standby mode and the power-on reset state, the current state switches to the manual reset state.
- When the STBY pin is driven low in all states, the current state switches to the hardware standby mode.
- Be sure to set the high-speed mode when switching to the watch mode and subactive mode.

Figure 2 Diagram of Mode Transition

Table 1 Transitional Conditions in Each Mode when SLEEP Instruction Is Executed and States of Return by Interrupts

Pre-transitional state	Control bit state at transition				Post-transitional state of SLEEP instruction	Post-return state by interruption
	SSBY	PSS	LSON	DTON		
High speed or medium speed	0	×	0	×	Sleep	High speed or medium speed
	0	×	1	×	—	—
	1	0	0	×	Software standby	High speed or medium speed
	1	0	1	×	—	—
	1	1	0	0	Watch	High speed
	1	1	1	0	Watch	Subactive
	1	1	0	1	—	—
	1	1	1	1	Subactive	—
Subactive	0	0	×	×	—	—
	0	1	0	×	—	—
	0	1	1	×	Subsleep	Subactive
	1	0	×	×	—	—
	1	1	0	0	Watch	High speed
	1	1	1	0	Watch	Subactive
	1	1	0	1	High speed	—
	1	1	1	1	—	—

[Note]
— : Do not set these bits.
× : Don't care

Table 4.2 LSI Internal State in Each Operating Mode

Function		High speed	Medium speed	Sleep	Module stop	Watch	Sub-active	Sub-sleep	Software standby	Hard-ware standby
System clock oscillator		Operation	Operation	Operation	Operation	Stop	Stop	Stop	Stop	Stop
Subclock oscillator		Operation/ stop	Operation/ stop	Operation/ stop	Operation/ stop	Operation	Operation	Operation	Operation/ stop	Stop
CPU operation	Instruc-tion	Operation	Medium-speed operation	Stop	Operation	Stop	Subclock operation	Stop	Stop	Stop
	Register			Retention		Retention		Retention	Retention	Undefined
RAM		Operation	Operation	Operation (DTC)	Operation	Retention	Operation	Retention	Retention	Retention
I/O		Operation	Operation	Operation	Operation	Retention	Operation	Operation	Retention	High impedance
External interrupt	NMI	Operation	Operation	Operation	Operation	Operation	Operation	Operation	Operation	Stop
	IRQn									
Peripheral function	PBC	Operation	Medium-speed operation	Operation	Operation/ stop (retention)	Stop (retention)	Subclock operation	Stop (retention)	Stop (retention)	Stop (reset)
	DTC	Operation	Medium-speed operation	Operation	Operation/ stop (retention)	Stop (retention)	Stop (retention)	Stop (retention)	Stop (retention)	Stop (reset)
	DMAC*1									
	WDT_1	Operation	Operation	Operation	Operation	Subclock operation	Subclock operation	Subclock operation	Stop (retention)	Stop (reset)
	WDT_0	Operation	Operation	Operation	Operation	Stop (retention)	Subclock operation	Subclock operation	Stop (retention)	Stop (reset)
	TMR	Operation	Operation	Operation	Operation/ stop (retention)	Stop (retention)	Subclock operation	Subclock operation	Stop (retention)	Stop (reset)
	TPU	Operation	Operation	Operation	Operation/ stop (retention)	Stop (retention)	Stop (retention)	Stop (retention)	Stop (retention)	Stop (reset)
	SCI									
	I^2C*2									
	D/A*3									
	A/D	Operation	Operation	Operation	Operation/ stop (reset)	Stop (reset)	Stop (reset)	Stop (reset)	Stop (reset)	Stop (reset)

[Note]
"Stop (retention)" indicates that the internal register values are retained. The internal state is disrupted.
"Stop (reset)" indicates that the internal register values and the internal state are initialized.
In the module stop mode, only the modules which is set to stop is set stop (reset or retention).
*1 Only the H8S/2239 products provides this function.
*2 The H8S/2237 and H8S/2227 products do not provide the I^2C bus interface.
*3 The H8S/2227 products does not provide D/A.

5. Description of Sample Program

5.1 File Configuration

A sample program is provided as a project of HEW (High-performance Embedded Workshop). When h8s.hws is executed, HEW starts up to enable source program referencing and updating. If you do not have HEW, directly refer to the following source files with an editor:

No.	File name	Application
1	resetprg.c	Executed starting at reset vector address 0 when the microcomputer is reset.
2	intprg.c	Executed when an interrupt source other than a reset is generated. DTC vector address is also set in this file.
3	dbsct.c	Processing for setting the start and end addresses of a section used by the _INITSCT function of resetprg.c in the section initialization table. For details of the processing, refer to sections 9 and 10 of the "H8S and H8/300 Series C/C++ Compiler, Assembler, Optimizing Linkage Editor User's Manual."
4	h8s2238.c	Main routine of this application note
5	com.c	Main common and interrupt processing routine of this application note
6	2238S.H	Structure definition file of the internal registers of the H8S/2238 products This file can be obtained from *2.
7	cwtbl.h	Variable and constant for this application note are defined.
8	prototypeh	A prototype for this application note is declared.
9	stacksct.h	A stack size is defined.

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5.2 Linkage

The linkage address of each section is indicated below.

In a HEW project file, a section can be referred to or set with "Category : section" in the Link/Library tab of the - "Standard Toolchain" of "Option".

Section	Start address
PResetPRG	0x000400
PIntPRG	
P	0x000800
C	
C$DSEC	
C$BSEC	
D	
B	0xFFB000
R	
S	0xFFEDB0

5.3 Subroutine Specifications

With this application note, Mode transition can be set and started using one subroutine. This function eases the use of mode transition.

1. Directly performs the transmission between modes.

   Subroutine name: **int** com_active_mode_change (**int** return_mode)

Parameter	Setting
return_mode	Specifies the transition destination mode.

Settings	Value	Transition destination mode
ACTIVE_MODE_PER_1	0	High-speed mode
ACTIVE_MODE_PER_2	1	Medium-speed mode ϕ/2
ACTIVE_MODE_PER_4	2	Medium-speed mode ϕ/4
ACTIVE_MODE_PER_8	3	Medium-speed mode ϕ/8
ACTIVE_MODE_PER_16	4	Medium-speed mode ϕ/16
ACTIVE_MODE_PER_32	5	Medium-speed mode ϕ/32
SUB_ACTIVE_MODE	6	Subactive mode

Return value	Description
0	Normal end of mode transition
–1	A mode that cannot be switched was specified. • An attempt was made to the switch subactive mode to the subactive mode.

2. This subroutine switches to the program halt state and then to the specified mode.

   Subroutine name: **int** com_sleep_mode_change (**int** stop_mode , **int** return_mode)

Parameter	Setting
stop_mode	Specifies the program halt state mode.

Settings	Value	Transition destination mode
SLEEP_MODE	0	Sleep mode
STANDBY_MODE	1	Software standby mode
WATCH_MODE	2	Watch mode
SUB_SLEEP_MODE	3	Subsleep mode

Parameter	Setting
return_mode	Specifies the return destination mode.

Settings	Value	Transition destination mode
ACTIVE_MODE_PER_1	0	High-speed mode
ACTIVE_MODE_PER_2	1	Medium-speed mode ϕ/2
ACTIVE_MODE_PER_4	2	Medium-speed mode ϕ/4
ACTIVE_MODE_PER_8	3	Medium-speed mode ϕ/8
ACTIVE_MODE_PER_16	4	Medium-speed mode ϕ/16
ACTIVE_MODE_PER_32	5	Medium-speed mode ϕ/32
SUB_ACTIVE_MODE	6	Subactive mode

Return value	Description of setting
0	Normal end of mode transition
–1	Indicates that A mode disabled to switched was specified. • When the current mode is the subactive mode, the mode transition to a program halt state other than the watch mode and subsleep mode was specified. • When the current mode is the subactive mode, the transition to a state other than the subactive mode was specified after transition to the subsleep mode. • When the current mode is the high-speed/medium-speed mode, the transition to a program halt state (subsleep mode) was specified. • When the current mode is the high-speed/medium-speed mode, the transition to the subactive mode was specified after the transition to a program halt state (sleep mode). • When the current mode is the high-speed/medium-speed mode, the transition to the subactive mode was specified after the transition to a program halt state (software standby mode).

5.4 Notes

To switch from the software standby mode, watch mode, or subactive mode to another mode, you must set the clock stabilization standby time with bits 2 to 0 (STS2 to STS0) in the SBYCR register. In this application note, the clock stabilization standby time is fixed at "STS[2:0] = 100" (standby time = 130172 states). Modify this fixed value appropriately according to the operating frequency of the microcomputer you are using. For information about where the clock stabilization standby time is modified, see the source code of subroutines in Section 5.3.

For information about how to calculate settings, see Section 23.11 in the "Hardware Manual."

5.5 LED Status Display

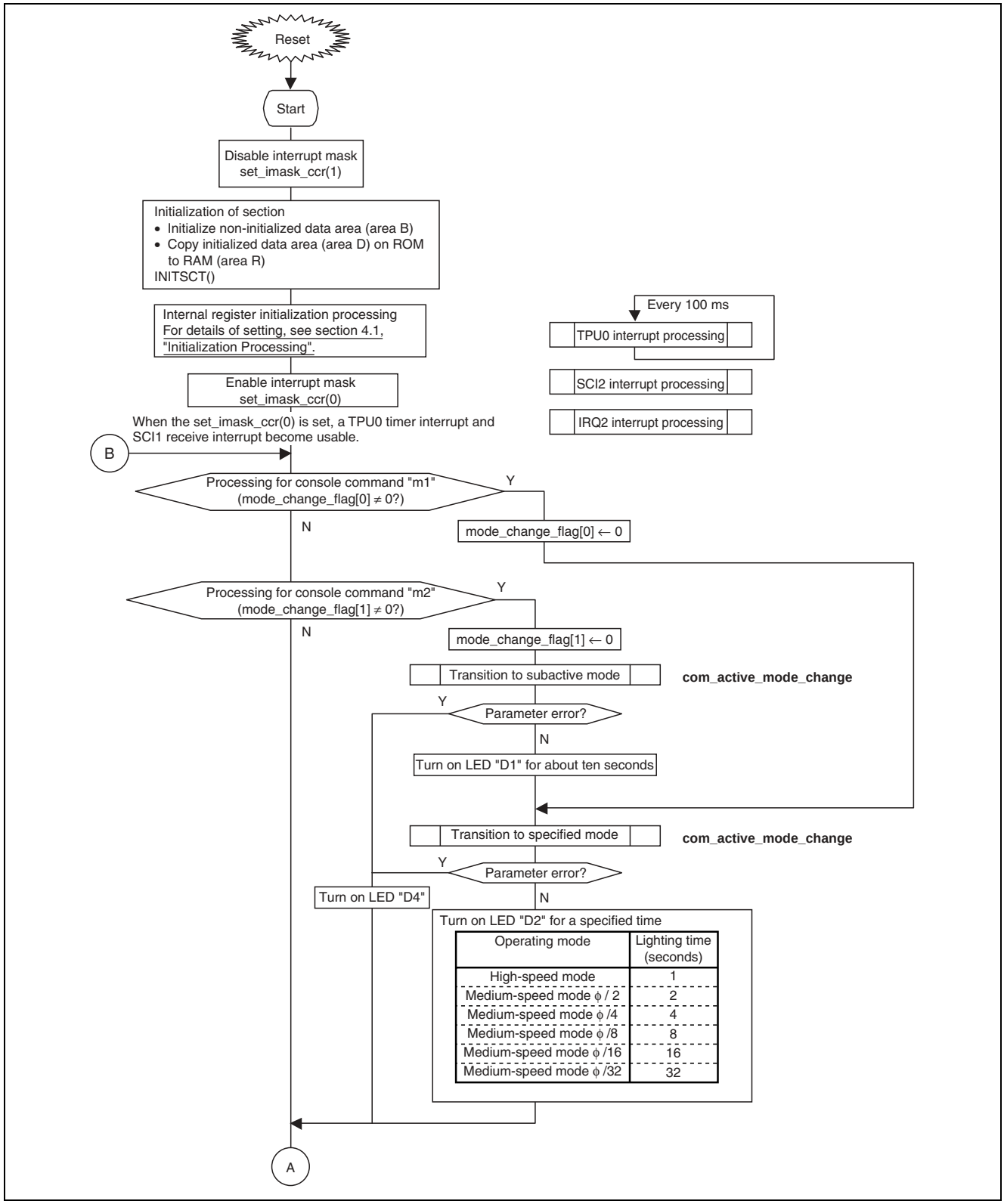
In this application note, LED ON/OFF indicates the mode transition state.

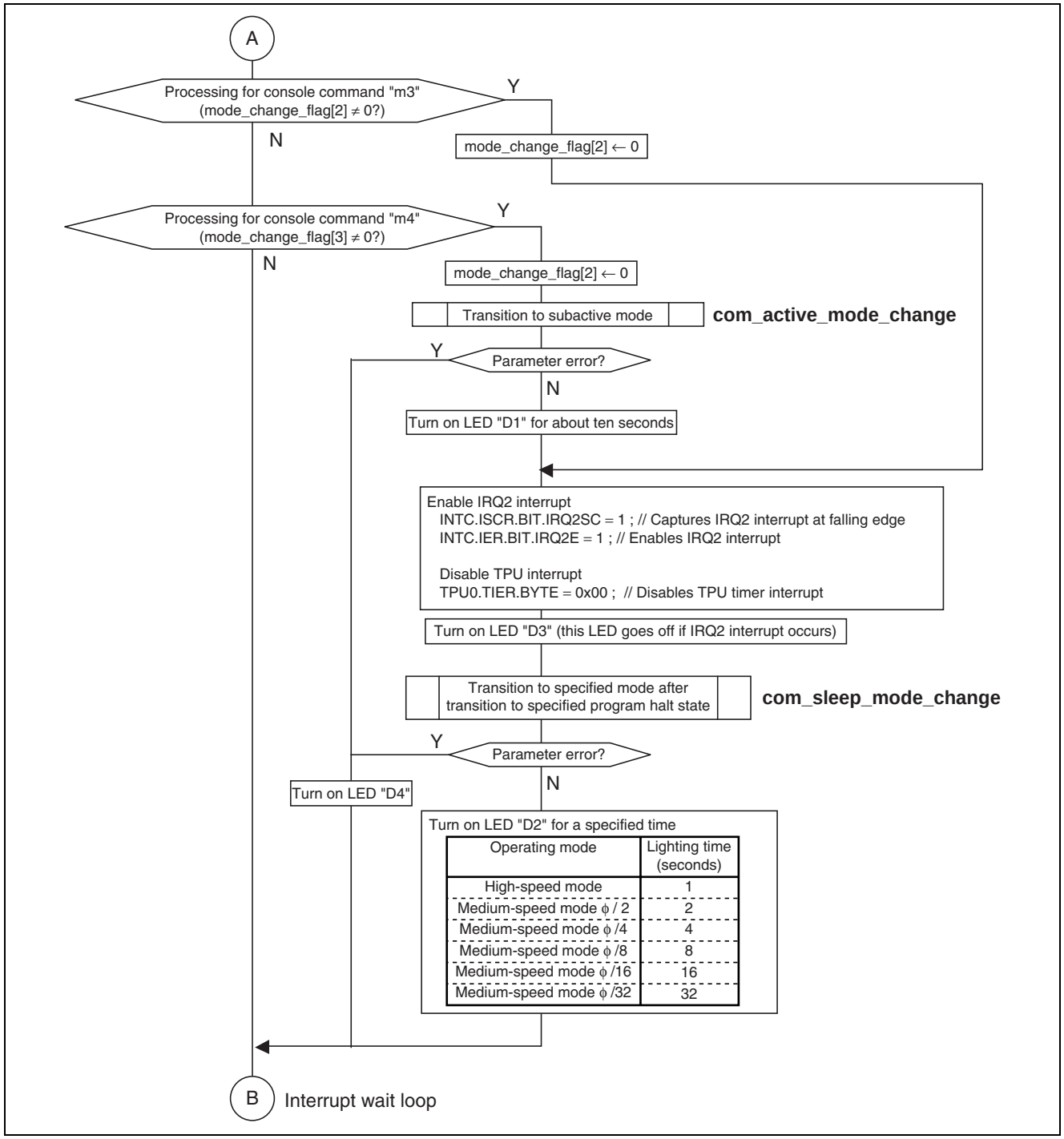
LED name	Description
D1	Illuminates for ten seconds when the current mode switches to the subactive mode.
D2	Illuminates for several seconds according to the CPU operating speed when the current mode switches to the high-speed/medium-speed mode.
D3	Illuminates when the H8S/2238 waits for the IRQ2 interrupt in the program halt state. Extinguishes when the IRQ2 interrupt occurs.
D4	Illuminates when the mode transition specification parameter error occurs.
D5 to D8	(Not used)

Operating mode	Lighting time (seconds)
High-speed mode	1
Medium-speed mode ϕ/2	2
Medium-speed mode ϕ/4	4
Medium-speed mode ϕ/8	8
Medium-speed mode ϕ/16	16
Medium-speed mode ϕ/32	32

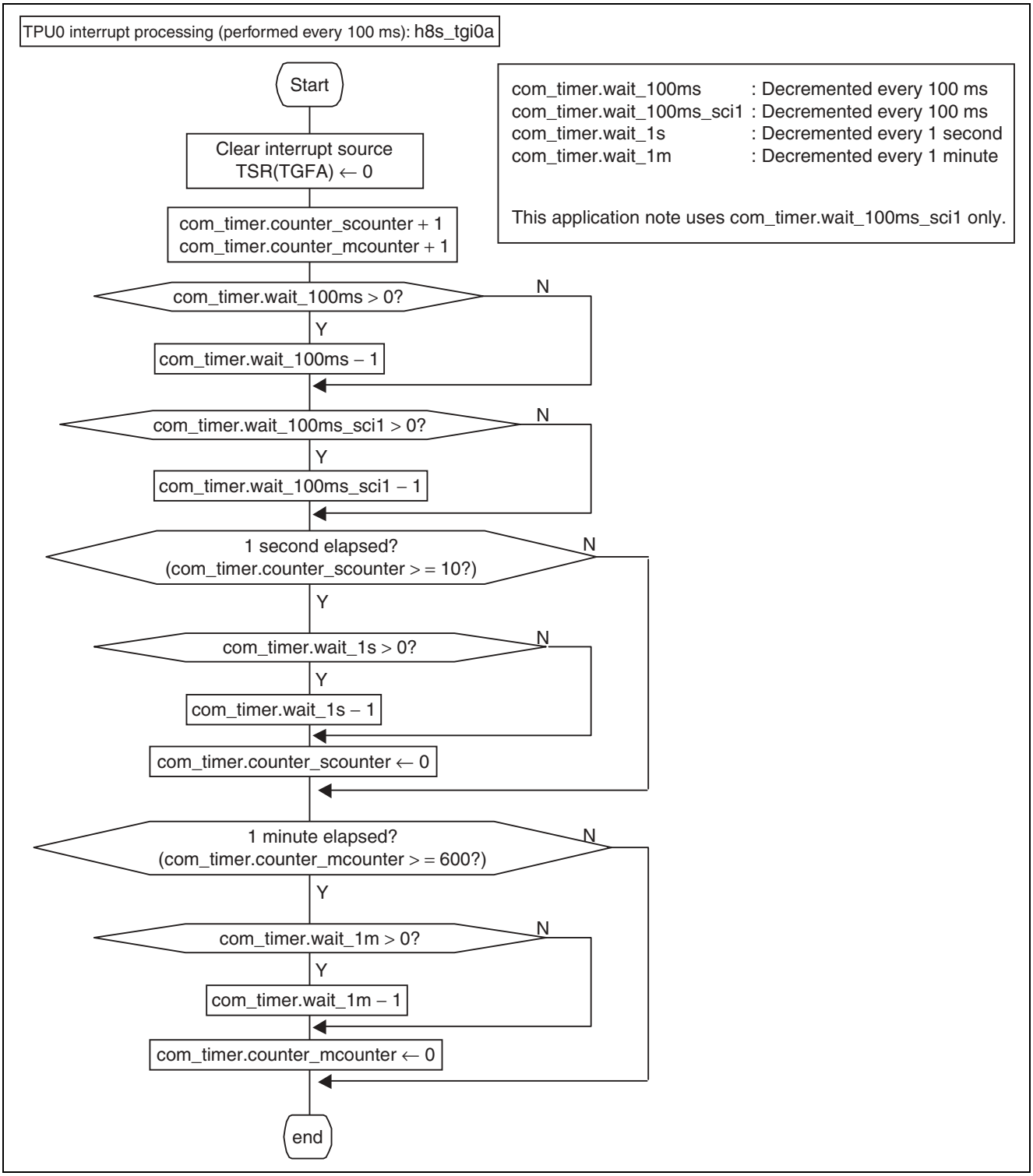
6. Flowchart

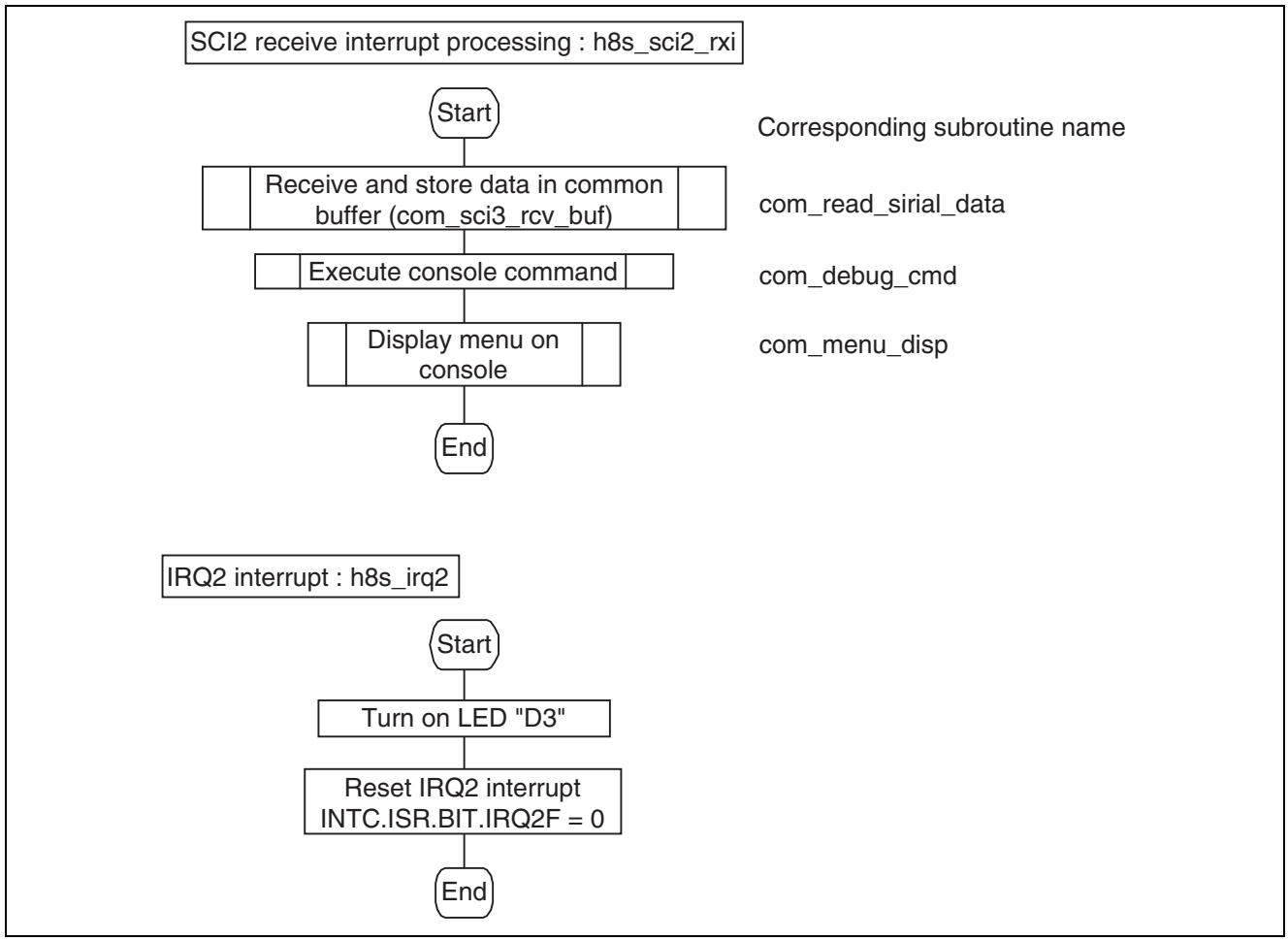
6.1 Overall Flow




A
Processing for console command "m3" (mode_change_flag[2] ≠ 0?)
Y
N
mode_change_flag[2] ← 0
Processing for console command "m4" (mode_change_flag[3] ≠ 0?)
Y
N
mode_change_flag[2] ← 0
Transition to subactive mode
com_active_mode_change
Y
Parameter error?
N
Turn on LED "D1" for about ten seconds
Enable IRQ2 interrupt
INTC.ISCR.BIT.IRQ2SC = 1 ; // Captures IRQ2 interrupt at falling edge
INTC.IER.BIT.IRQ2E = 1 ; // Enables IRQ2 interrupt
Disable TPU interrupt
TPU0.TIER.BYTE = 0x00 ; // Disables TPU timer interrupt
Turn on LED "D3" (this LED goes off if IRQ2 interrupt occurs)
Transition to specified mode after transition to specified program halt state
com_sleep_mode_change
Y
Parameter error?
N
Turn on LED "D4"
Turn on LED "D2" for a specified time
Operating mode
Lighting time (seconds)
High-speed mode
1
Medium-speed mode ϕ / 2
2
Medium-speed mode ϕ /4
4
Medium-speed mode ϕ /8
8
Medium-speed mode ϕ /16
16
Medium-speed mode ϕ /32
32
B
Interrupt wait loop

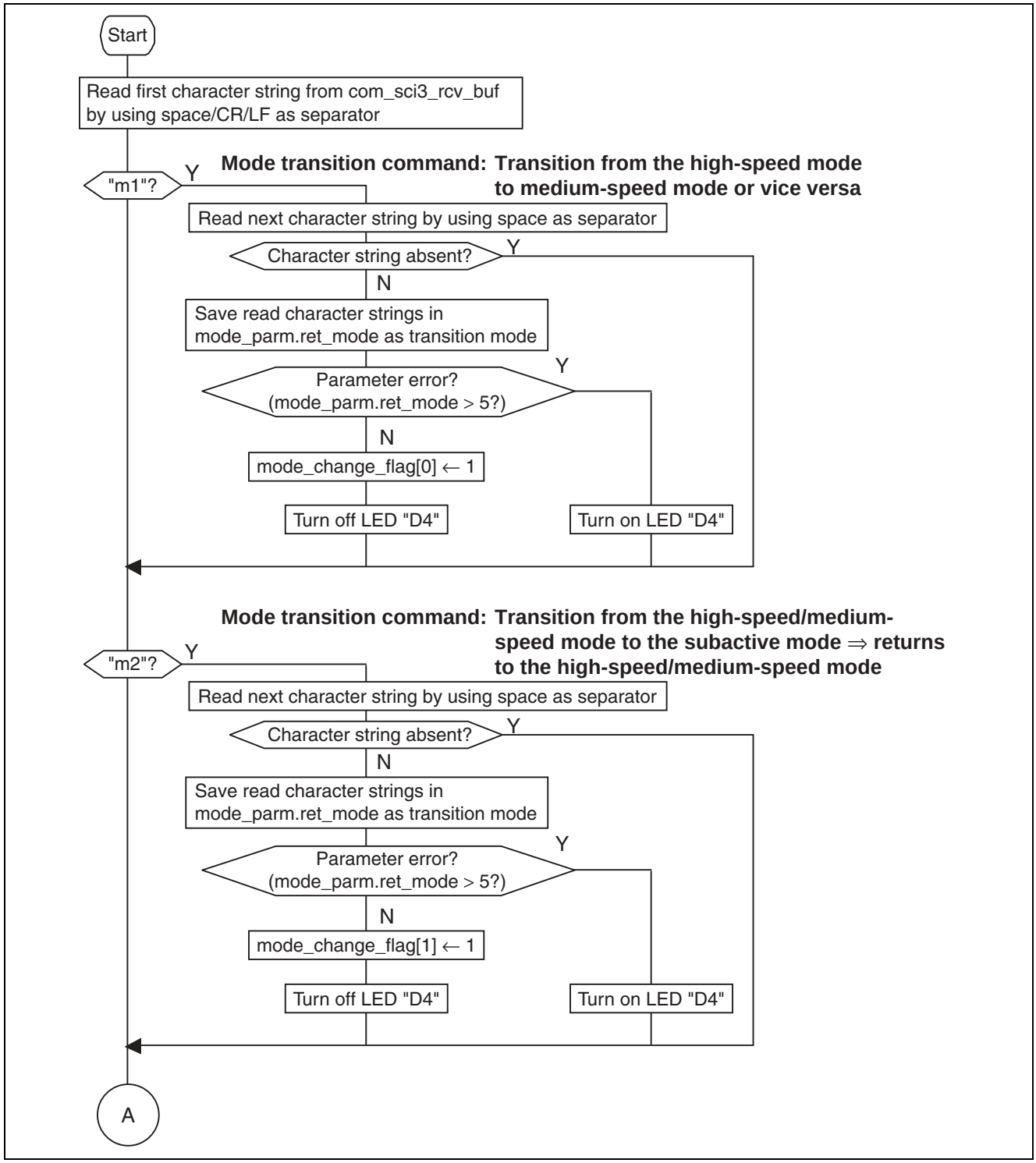
6.2 Interrupt Processing

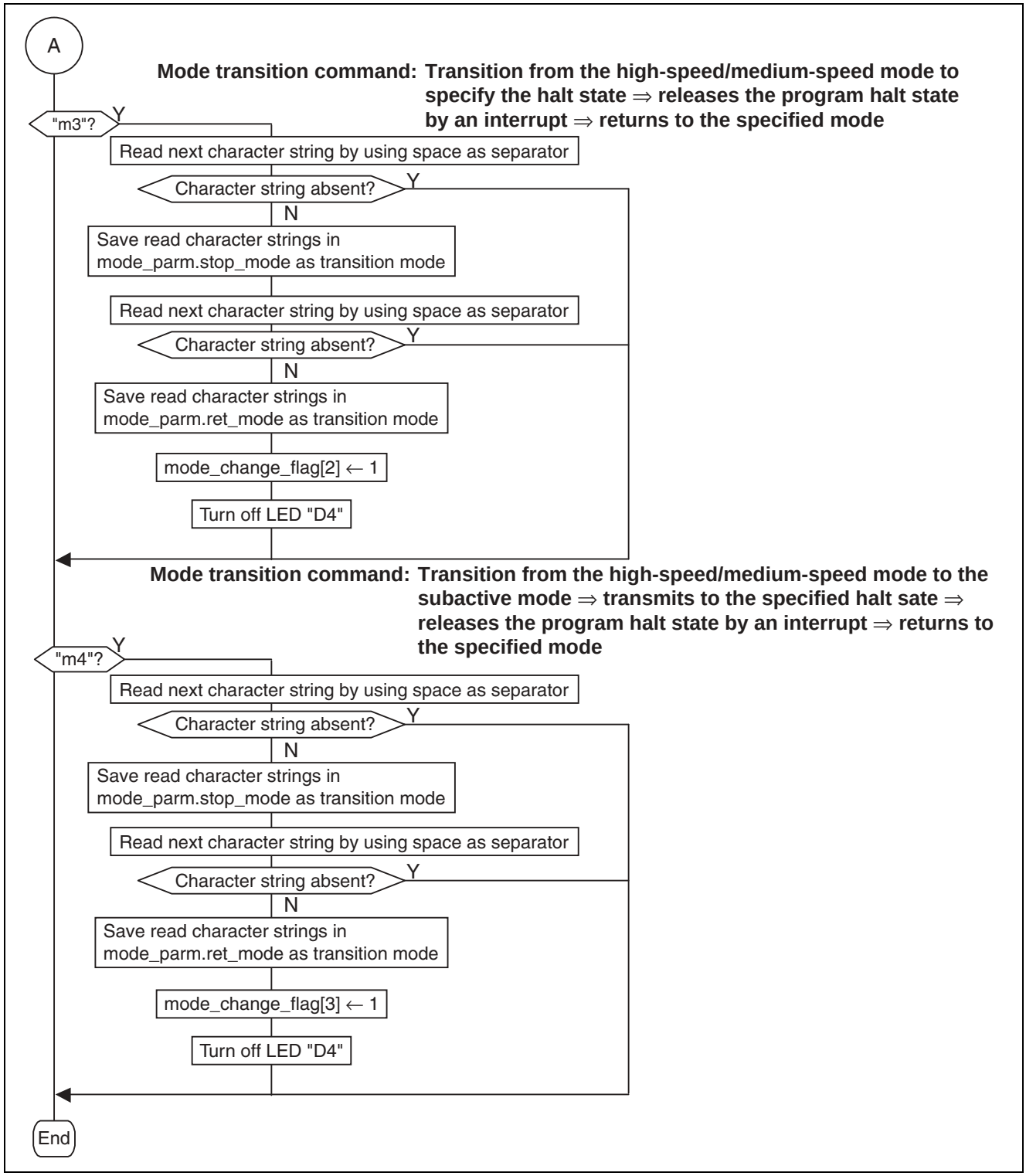



SCI2 receive interrupt processing : h8s_sci2_rxi
Start
Receive and store data in common buffer (com_sci3_rcv_buf)
Execute console command
Display menu on console
End
Corresponding subroutine name
com_read_sirial_data
com_debug_cmd
com_menu_disp
IRQ2 interrupt : h8s_irq2
Start
Turn on LED "D3"
Reset IRQ2 interrupt
INTC.ISR.BIT.IRQ2F = 0
End

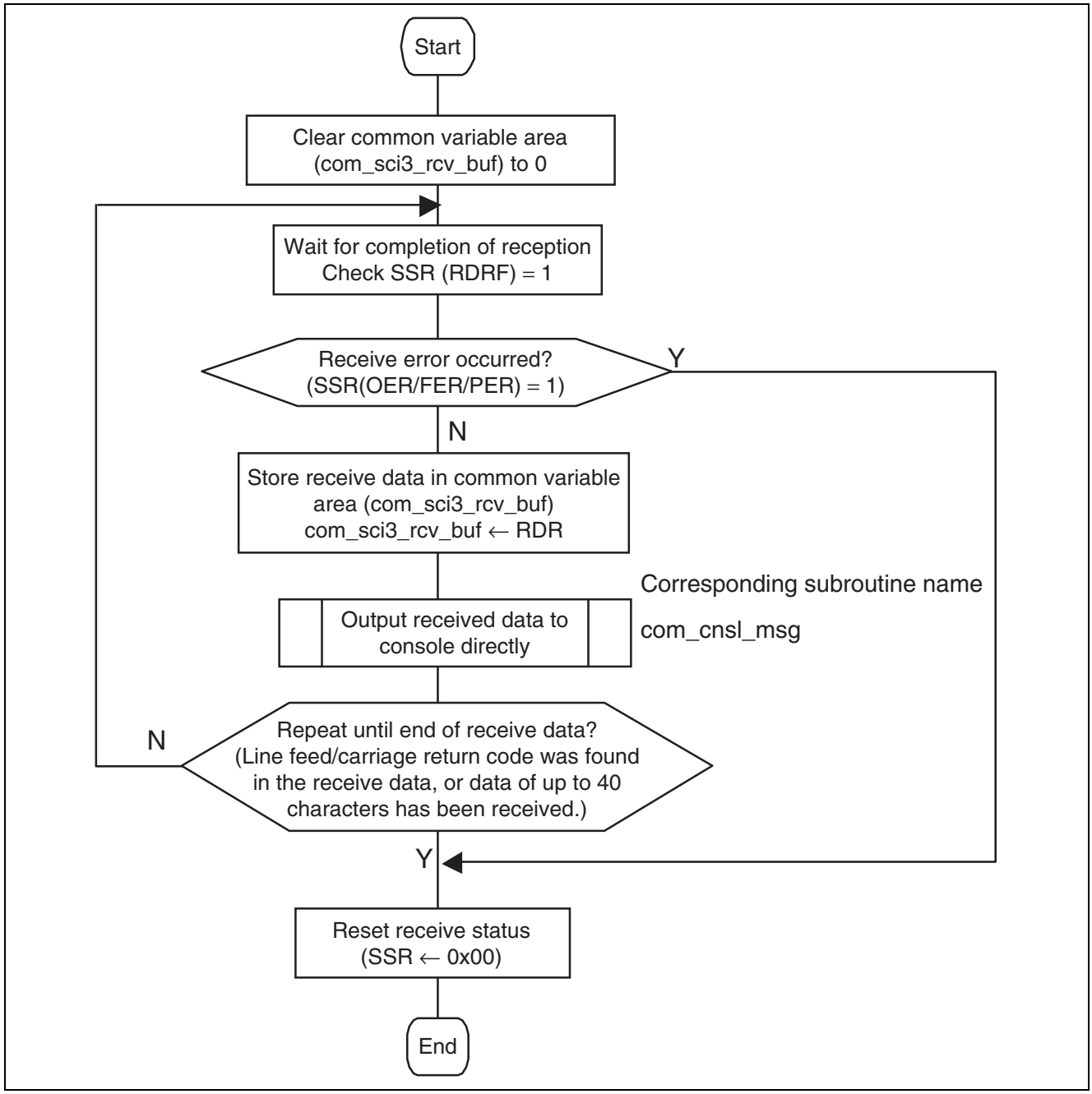
6.3 Detailed Processing

com_debug_cmd
: Console command analysis and execution

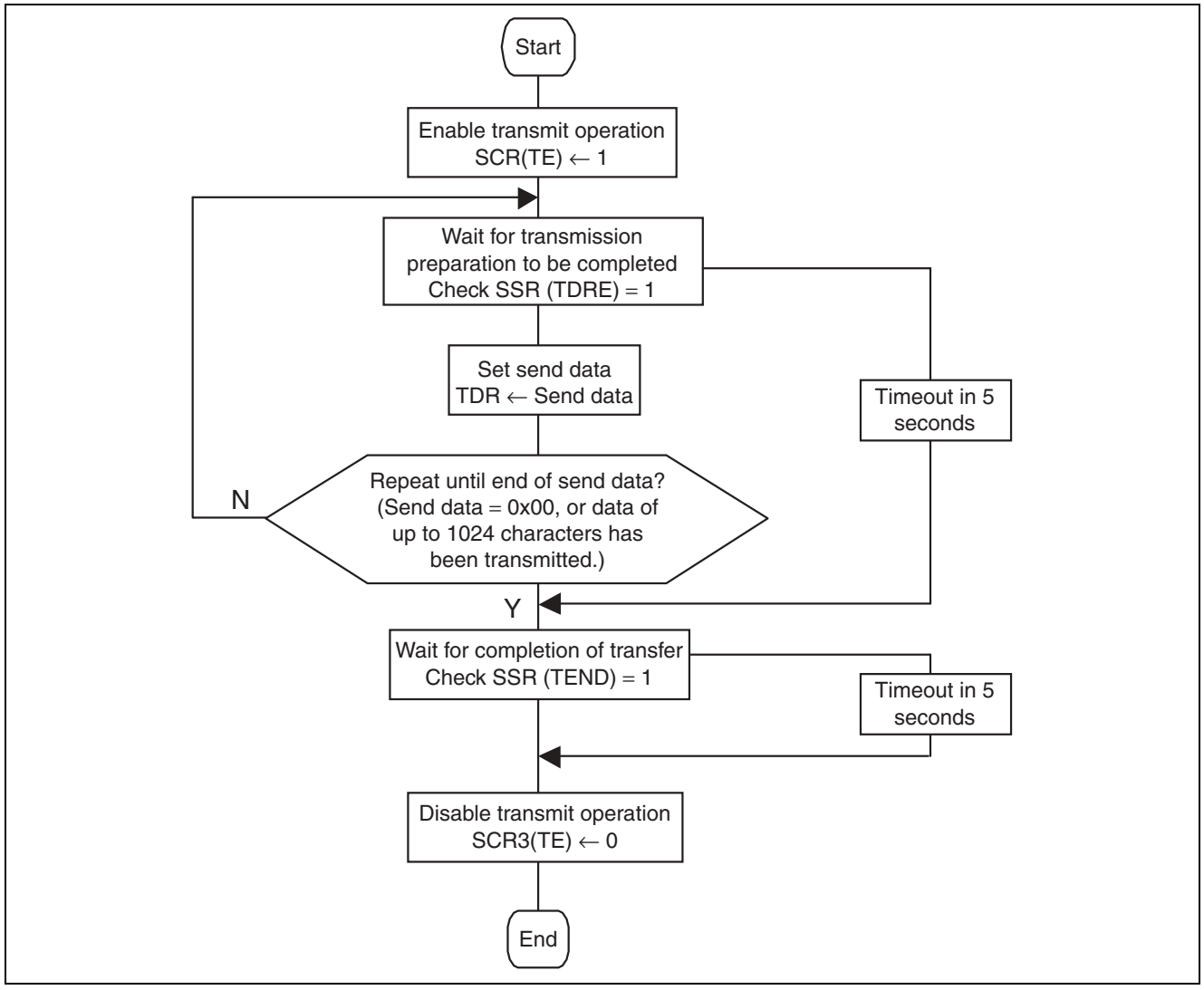



A
Mode transition command: Transition from the high-speed/medium-speed mode to specify the halt state ⇒ releases the program halt state by an interrupt ⇒ returns to the specified mode
"m3"?
Y
Read next character string by using space as separator
Character string absent?
Y
N
Save read character strings in mode_parm.stop_mode as transition mode
Read next character string by using space as separator
Character string absent?
Y
N
Save read character strings in mode_parm.ret_mode as transition mode
mode_change_flag[2] ← 1
Turn off LED "D4"
Mode transition command: Transition from the high-speed/medium-speed mode to the subactive mode ⇒ transmits to the specified halt sate ⇒ releases the program halt state by an interrupt ⇒ returns to the specified mode
"m4"?
Y
Read next character string by using space as separator
Character string absent?
Y
N
Save read character strings in mode_parm.stop_mode as transition mode
Read next character string by using space as separator
Character string absent?
Y
N
Save read character strings in mode_parm.ret_mode as transition mode
mode_change_flag[3] ← 1
Turn off LED "D4"
End

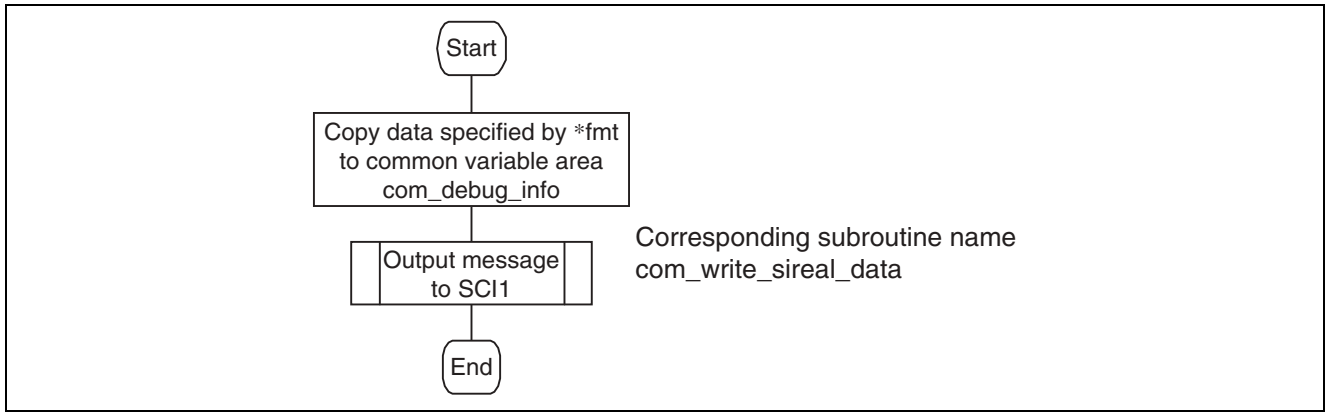
com_read_sirial_data
: Receives a message from the SCI1 interface
Received data with maximum of 40 characters is received
in the common variable area (com_sci3_rcv_buf).



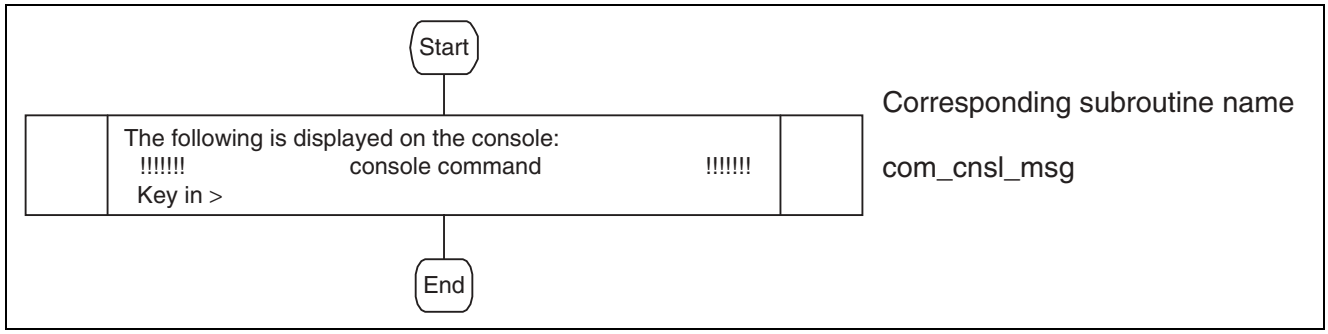
com_write_sireal_data (char *p)
: Transmits a message to the SCI3 interface
*p : Address where message data is stored



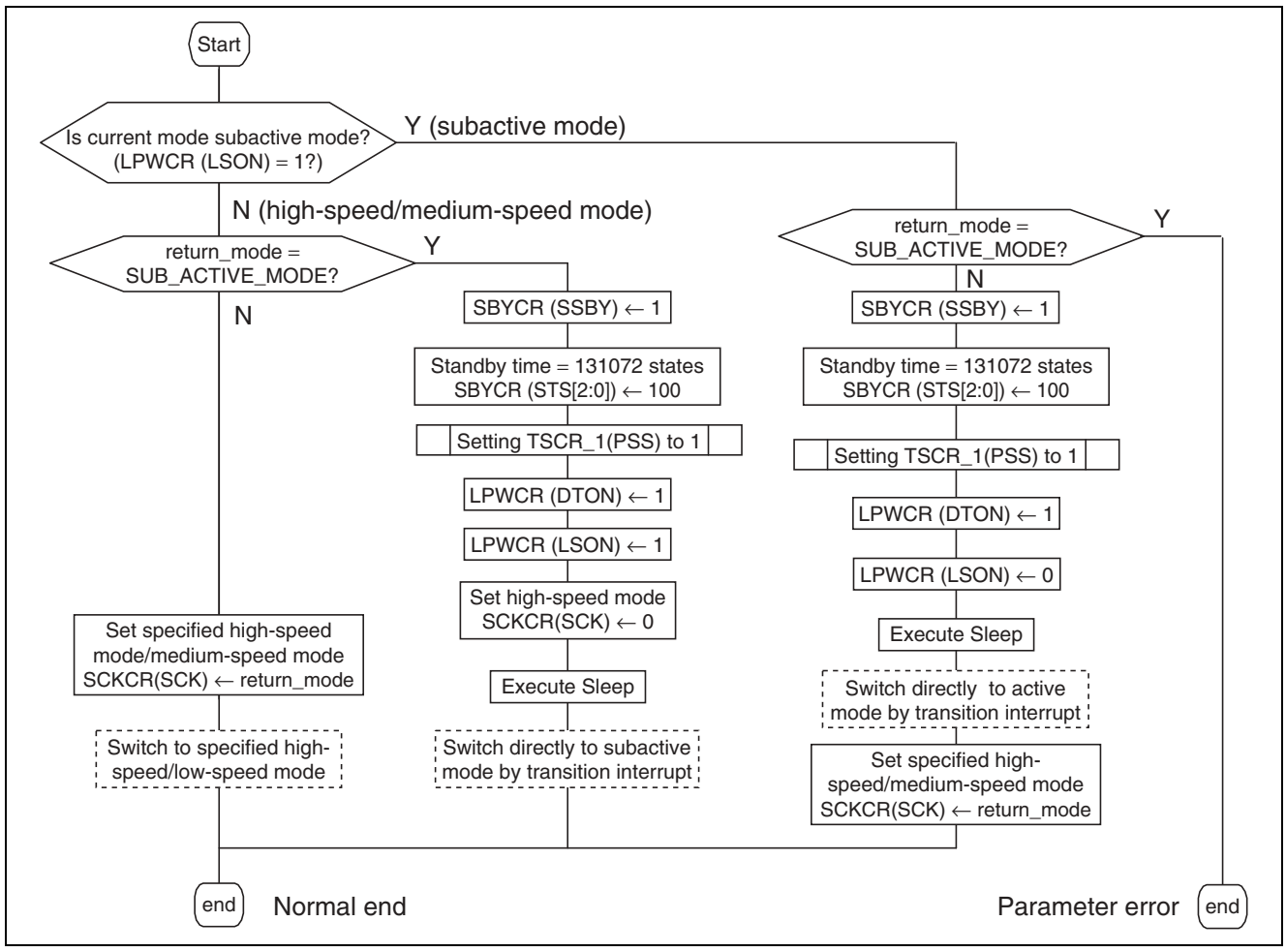
com_cnsl_msg(char *fmt, ...)
: Transmits a message to the console
*fmt : Address where variable-length message data is stored



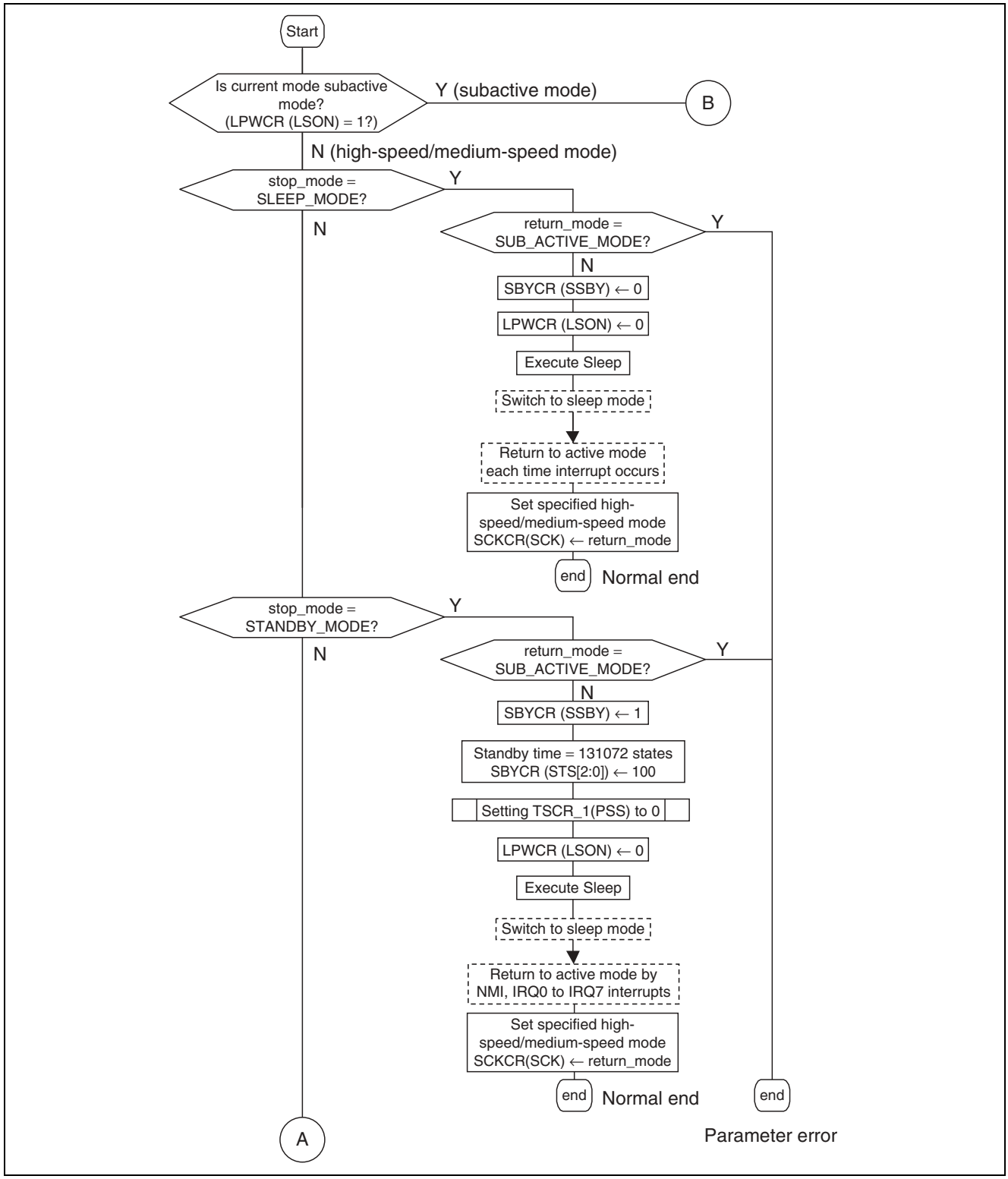
com_menu_disp
: Display of the operation menu on the console

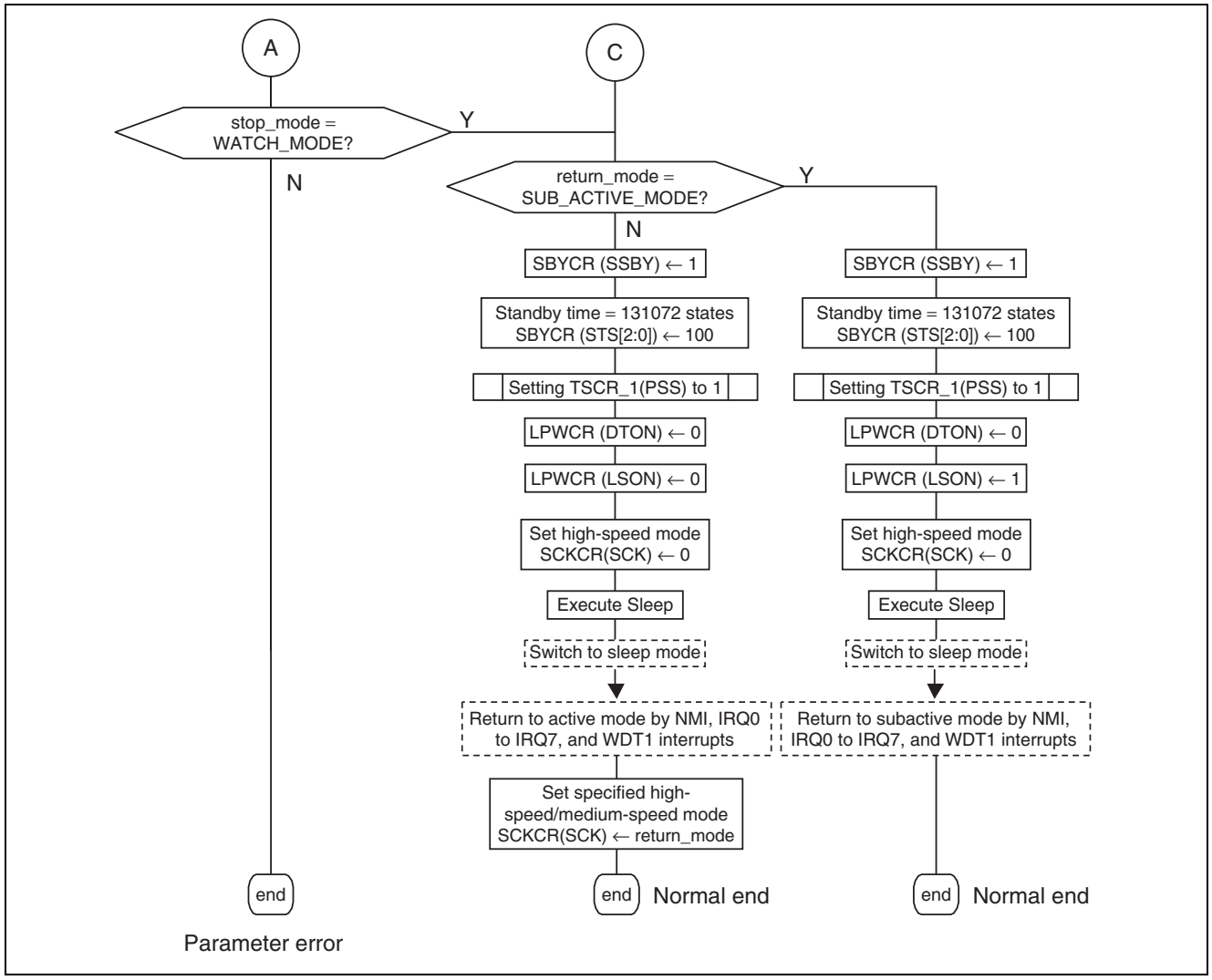


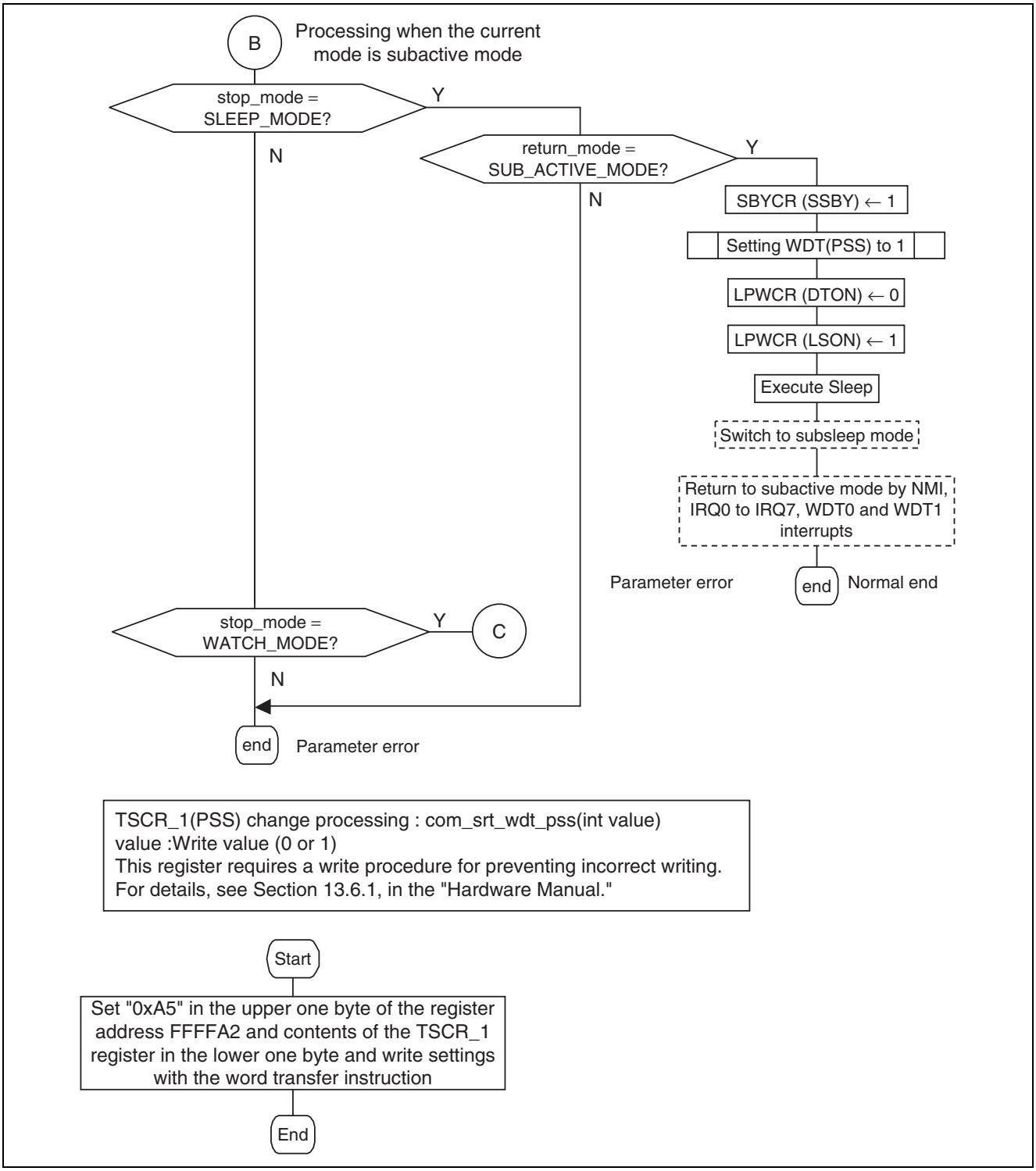
int com_active_mode_change (int return_mode)
: Directly performs the transition between modes.
  return_mode : Specifies the transition operating mode.



com_sleep_mode_change (int stop_mode , int return_mode)
: Switches to the program halt state and then to the specified mode.
stop_mode : Specifies the program halt state mode.
return_mode : Specifies the return destination mode.




A
C
stop_mode = WATCH_MODE?
Y
N
return_mode = SUB_ACTIVE_MODE?
Y
N
SBYCR (SSBY) ← 1
Standby time = 131072 states
SBYCR (STS[2:0]) ← 100
Setting TSCR_1(PSS) to 1
LPWCR (DTON) ← 0
LPWCR (LSON) ← 0
Set high-speed mode
SCKCR(SCK) ← 0
Execute Sleep
Switch to sleep mode
Return to active mode by NMI, IRQ0 to IRQ7, and WDT1 interrupts
Set specified high-speed/medium-speed mode
SCKCR(SCK) ← return_mode
SBYCR (SSBY) ← 1
Standby time = 131072 states
SBYCR (STS[2:0]) ← 100
Setting TSCR_1(PSS) to 1
LPWCR (DTON) ← 0
LPWCR (LSON) ← 1
Set high-speed mode
SCKCR(SCK) ← 0
Execute Sleep
Switch to sleep mode
Return to subactive mode by NMI, IRQ0 to IRQ7, and WDT1 interrupts
end
Parameter error
end
Normal end
end
Normal end


B
Processing when the current mode is subactive mode
stop_mode = SLEEP_MODE?
Y
N
return_mode = SUB_ACTIVE_MODE?
Y
N
SBYCR (SSBY) ← 1
Setting WDT(PSS) to 1
LPWCR (DTON) ← 0
LPWCR (LSON) ← 1
Execute Sleep
Switch to subsleep mode
Return to subactive mode by NMI, IRQ0 to IRQ7, WDT0 and WDT1 interrupts
Parameter error
end
Normal end
stop_mode = WATCH_MODE?
Y
C
N
end
Parameter error
TSCR_1(PSS) change processing : com_srt_wdt_pss(int value)
value :Write value (0 or 1)
This register requires a write procedure for preventing incorrect writing.
For details, see Section 13.6.1, in the "Hardware Manual."
Start
Set "0xA5" in the upper one byte of the register address FFFFA2 and contents of the TSCR_1 register in the lower one byte and write settings with the word transfer instruction
End

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.16.04	—	First edition issued

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