IGBT

IGBT Module Application Note

Introduction

This application note describes IGBT module specifications, how to mount the module, and related usage notes.

Contents

1. Overview

This document was written specifically for power electronics engineers developing inverters for xEVs using IGBT (Insulate-gate Bipolar Transistor) modules. We aim to help engineers understand each parameter listed on the datasheet and to explain the precautions and usage notes for using the module (mounting method, gate drive, etc.).

The target module described in this document is a 6-in-1 module with single-sided cooling, module withstand voltage of 750V or 1200V, and a current range of several hundred amps.

2. Target Module Structure

The module under consideration is a 6-in-1 module for 3-phase inverters with U, V, and W phases, 3-arm IGBTs and FRDs (Fast Recovery Diode) (which is an FWD (Free-Wheeling Diode), in a single housing.

An equivalent circuit diagram is shown in Fig.1-1 In addition to the IGBT and FRD, thermistors are provided for temperature measurement in U, V, and W phases.
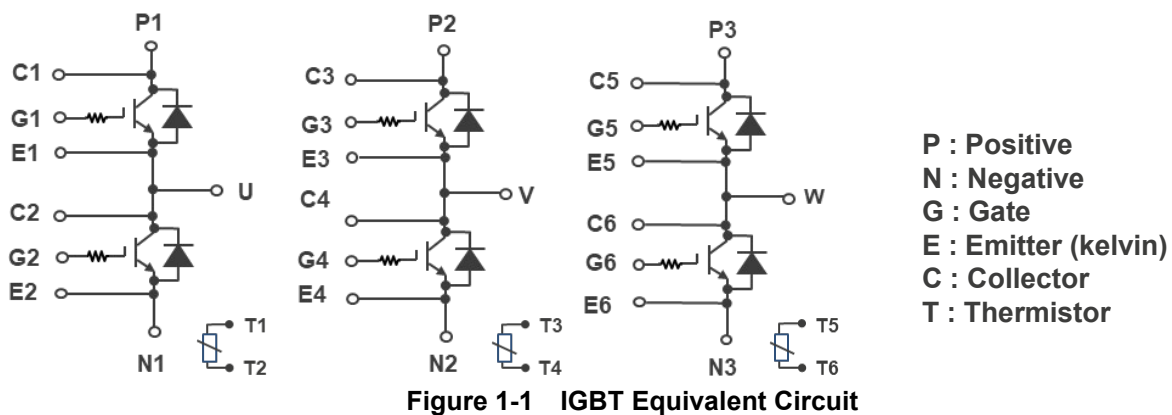

P : Positive
N : Negative
G : Gate
E : Emitter (kelvin)
C : Collector
T : Thermistor

Figure 1-1   IGBT Equivalent Circuit

Figure 1-2 shows exterior views of the module. There are two types of heat sinks (copper base) on the back: flat plate and pin fin. The pin-finned copper base module is a direct water-cooling type in which an LLC (Long Life Coolant—antifreeze used for engine cooling; main ingredient is ethylene glycol) solution is directly applied to the back of the copper base. In general, the LLC solution is 50% water and 50% LLC. On the other hand, the flat copper-base module is basically cooled by adhering it to the cooling component with high thermally conductive grease. The two types of modules differ only in whether the back copper base is flat or equipped with pin fins; the remaining materials are essentially the same. Compared to flat copper base modules, the pin-finned copper base module significantly reduces thermal resistance due to the absence of both grease thermal resistance and the thermal resistance of the cooling component.

Figure 1-3 shows the cross-sectional schematic of the module, illustrating a flat copper base module. The Si chips (IGBT, FRD) are soldered or similarly attached to the surface of a ceramic substrate, which has a thin copper plate, about 0.5 mm thick or less, bonded to both sides. The ceramic material is typically alumina or silicon nitride with a thickness of a few tenths of a millimeter. The purpose of the ceramic substrate is to insulate the Si chips, which are subjected to high voltage. The ceramic substrate mounted with the Si chips is soldered or similarly attached to the copper base. The ceramic substrate electrodes (copper patterns on the substrate surface) are connected to the Si chip surface electrodes using Al wires, Al ribbons, etc. The ceramic substrate electrodes and the module terminals are connected using solder bonding, ultrasonic bonding, or similar methods using conductive materials like copper. The IGBT and FRD are electrically connected to the module terminals in the above-described structure.

The heat generated by the Si chip due to loss during current drive (steady-state loss during conduction and switching loss during switching) is dissipated via the copper base, which serves as a cooling component. Therefore, the temperature of the Si chip when using pin-fin cooling component is controlled by adjusting the temperature of the LLC solution and the cooling water flow rate, which are the main determinants of the heat transfer rate. For flat-type cooling component, in addition to the above, the material and thickness of the high

thermally conductive grease, as well as the material and fin shape of the cooling component, must be adjusted.

Since the materials used in the module (aluminum, silicon (Si), solder, copper, and ceramics) each have different linear coefficients of expansion, stress and strain occur between the materials during heating and cooling from current drive. The repeated strain causes cracks to form and propagate at the aluminum wire/Si chip interface and in the solder. These cracks lead to increased conduction and thermal resistance, which constitutes the thermal fatigue of the module. Since thermal fatigue ultimately causes damage to the Si chip, the thermal fatigue life of the module must be considered during the system design stage.
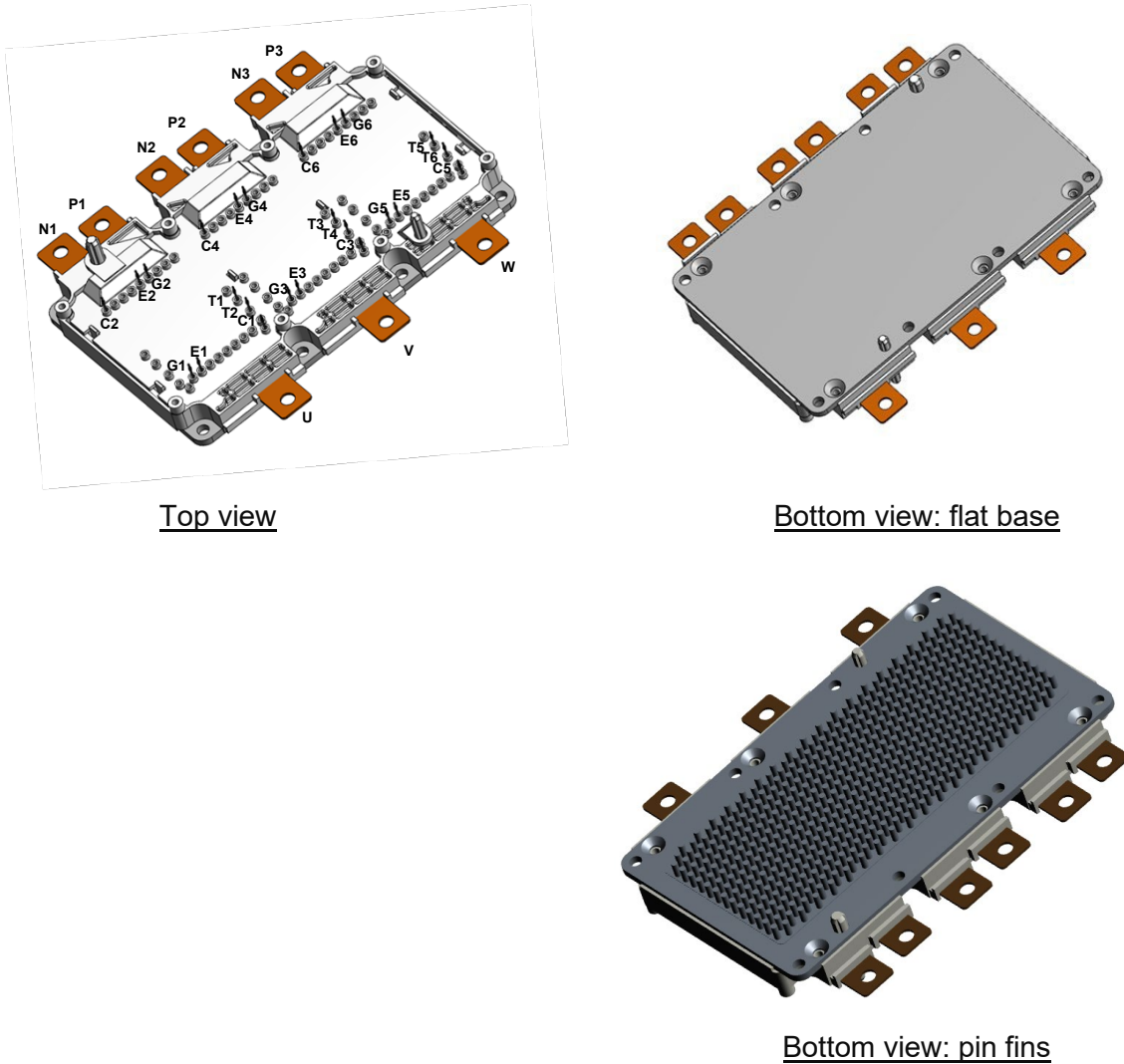

Top view   Bottom view: flat base

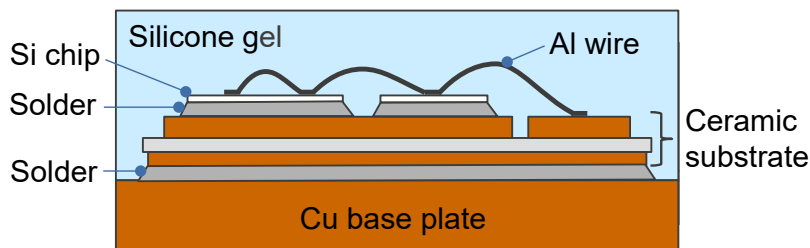Bottom view: pin fins

Figure 1-2   Exterior View

Figure 1-3 Cross-sectional Schematic (flat base)

3.   Datasheet Parameters

3.1   IGBT

3.1.1   Absolute Maximum Ratings

Absolute maximum ratings are rated values set to ensure safe usage of the IGBT. Exceeding the absolute maximum ratings even instantaneously may lead to degradation or breakdown of the circuit, so always use IGBTs within the maximum ratings stated here.

Table 1-1   Absolute Maximum Ratings

| Name		Symbol	Definition
Collector to Emitter voltage		V_{CES}	Maximum voltage that can be applied between collector and emitter.
Collector current	Nominal current	I_{CN}	Current value used in the product number; used to roughly classify the output.
	Continuous DC current	I_{Cnom}	Maximum allowable current during continuous DC current flow. Determined by the thermal characteristics (loss x thermal resistance) that satisfy the maximum junction temperature (T_{vj}) or less.
	Repetitive peak current	I_{CRM}	Maximum allowable current during pulse operation. Determined by conditions that satisfy switching reliability (RBSOA) and do not exceed maximum T_{vj}.
Collector loss		P_{tot}	Maximum allowable dissipation (loss) to satisfy maximum T_{vj}.
Gate voltage		V_{GES}	Maximum voltage that can be applied between gate and emitter.

3.1.2   Characteristics

Table 1-2 lists parameters and corresponding definitions related to IGBTs.

Table 1-2   IGBT Parameters

Name		Symbol	Definition
Collector to Emitter saturation voltage		V_{CEsat}	Collector-emitter voltage at a specified gate-emitter voltage and a specified collector current.
Gate to Emitter threshold voltage		V_{GEth}	Gate-emitter voltage at a specified collector-emitter voltage and a specified collector current.
Total Gate charge		Q_G	Gate charge required to reach a specified gate-emitter voltage.
Internal Gate resistance		R_{Gint}	Internal gate series resistance value
Parasitic capacitance [1]	Input capacitance	C_{ies}	Gate-emitter capacitance at a specified gate-emitter voltage, specified collector-emitter voltage, and specified frequency.
	Reverse transfer capacitance	C_{res}	Gate-collector capacitance at a specified gate-emitter voltage, specified collector-emitter voltage, and specified frequency.
	Output capacitance	C_{oes}	Collector-emitter capacitance at a specified gate-emitter voltage, specified collector-emitter voltage, and specified frequency.
Collector to Emitter cut-off current		I_{CES}	Collector current when the gate-emitter is shorted and a specified voltage is applied between collector and emitter.
Gate to Emitter leakage current		I_{GES}	Gate current when the collector-emitter is shorted and a specified voltage is applied between gate and emitter.

1) Figure 2-1 shows a diagram explaining parasitic capacitance.

Input capacitance $C_{ies} = C_{gc} + C_{ge}$
Output capacitance $C_{oes} = C_{ce} + C_{gc}$
Reverse transfer capacitance $C_{res} = C_{gc}$
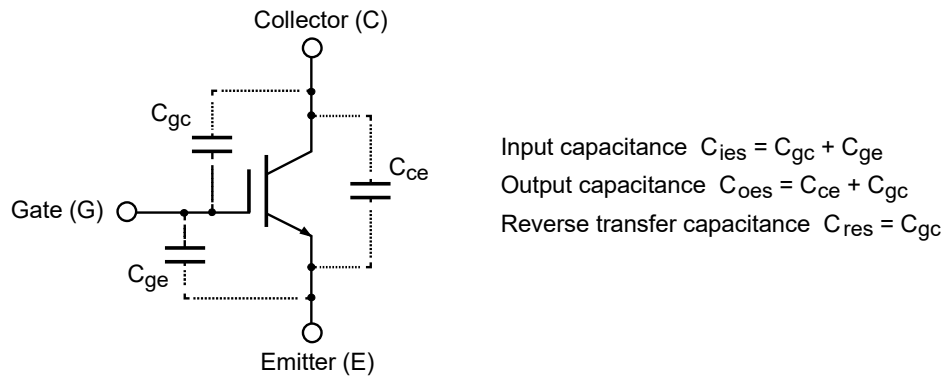
Figure 2-1   Gate Capacitance Explanation

3.2 FRD

3.2.1 Absolute Maximum Ratings

As with the absolute maximum ratings for the IGBT, these are rated values set to ensure safe usage of the FRD. Exceeding absolute maximum ratings even instantaneously may lead to deterioration or breakdown of the circuit, so please be sure to use IGBTs within the maximum ratings stated here

Table 2-1   Absolute Maximum Ratings

Name		Symbol	Definition
Repeated peak reverse voltage		V_{RRM}	Maximum voltage that can be applied between the cathode and anode of reverse-parallel diodes. Same value as V_{CES} of the IGBT.
Forward current	Nominal forward current	I_{FN}	Same as I_{CN} of the IGBT -- used to roughly classify the output.
	Continuous DC current	I_F	Maximum current allowed during continuous DC current flow. Determined by the thermal characteristics (loss x thermal resistance) that satisfy the maximum junction temperature (T_{vj}) or less.
	Repetitive peak current	I_{FRM}	Maximum current allowed during switching operation. Determined by conditions that satisfy switching reliability (SOA) and do not exceed maximum T_{vj}.
I^2t value		I^2t	The overcurrent's Joule integral value that the diode can tolerate; specified for one cycle of a commercial half-sine wave (50, 60Hz).

3.2.2 Characteristics

Table 2-2 lists parameters and corresponding definitions for the FRD.

Table 2-2   FRD Parameters

Name	Symbol	Definition
Diode forward voltage	V_F	Forward voltage value when specified forward current flows into FWD.
Maximum diode reverse recovery current	I_{RM}	Maximum value of reverse current that flows when forward current in the FWD is cut off.
Diode reverse recovery charge	Q_r	Total charge that disappears during reverse recovery operation.
Reverse recovery loss	E_{rec}	Energy loss generated during reverse recovery in the FWD
Thermal resistance	R_{thJF}	Thermal resistance from junction to cooling water.
	R_{thJC}	Thermal resistance from junction to back of case (back of copper base).
Junction temperature during continuous operation	$T_{vj\ op}$	Temperature of junction at which the element can be continuously operated.

3.3 Thermistor

Table 3-1 shows the parameters and corresponding definitions for the NTC thermistor.

Table 3-1   NTC Thermistor Parameters

| Name	Symbol	Definition	
Thermistor resistance	R_{25}	Electrical resistance between thermistor terminals at 25℃.	
Resistance variation	$\Delta R/R$	Variation in resistance at a specified temperature.	
Power dissipation	P_{25}	Self-heating of the thermistor must be avoided to ensure accurate temperature measurement. Power dissipation is the amount of heat (loss) generated by the thermistor to raise its temperature by 1K.	
B Value[1]	$B_{25/50}$	In resistance-temperature characteristics, this constant indicates the magnitude of resistance change between any two temperatures.	Constant between 25 and 50℃
	$B_{25/80}$		Constant between 25 and 80℃
	$B_{25/100}$		Constant between 25 and 100℃

For example, when B is between 25 and 50 ℃, thermistor resistance R2 of temperature T2 is calculated with the following equation: $R2 = R25\ \exp\ [B_{25/50}(1/T2 - 1/298.15\ K)]$

3.4 Module Parameters

Table 4-1 shows the parameters and corresponding definitions for the module.

Table 4-1 Module Parameters

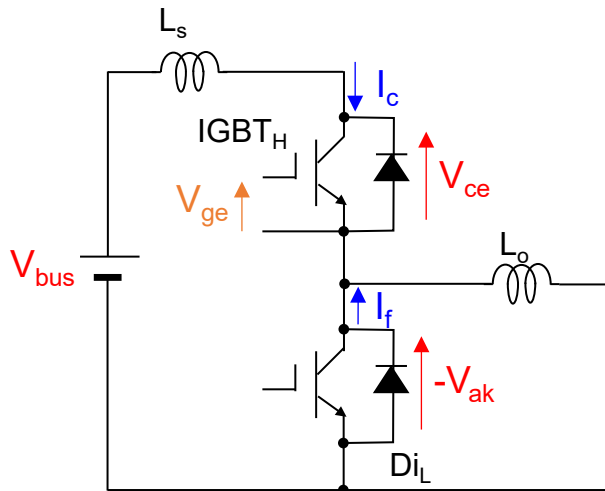| Name	Symbol	Definition
Dielectric strength test voltage	V_{ISOL}	Effective value of voltage applied between electrodes and heat sink when all IGBT module electrodes are short-circuited.
Maximum terminal current	I_{tRMS}	Maximum thermally allowable current under specified current conditions.
Creepage distance	d_{Creep}	Distance along the surface of an insulating material between a terminal and heat sink or between terminals.
Clearance distance	d_{Clear}	Shortest distance through air between a terminal and heat sink or between terminals.
Comparative tracking index	CTI	Insulation performance index of resin evaluated under insulation test conditions specified in IEC60112. The larger the value, the better the insulation performance.
Pressure loss	Δp	Pressure loss generated between inlet and outlet when cooling water flows through the module cooling component under specified conditions.
Module cooling component maximum pressure	p	Maximum allowable water pressure to prevent cooling water leakage and other malfunctions.
Parasitic inductance	L_{sCE}	Parasitic inductance from terminal P to terminal N per one phase. Refer to Figure 3-1.
Module wiring resistance	$R_{CC'+EE'}$	Parasitic resistance between power terminals of a single switch. Refer to Figure 3-1.
Storage temperature	T_{stg}	Maximum and minimum temperatures for long-term storage.
Module tightening torque	M	Torque required to achieve appropriate clamping of heat sink. Especially important for direct cooling types to prevent cooling water leakage.
Weight	G	—

$L_{sCE}=Ls1+Ls2+Ls3+Ls4$
$R_{CC'+EE'}=Rs1+Rs2+Rs5$ for Upper arm
$R_{CC'+EE'}=Rs4+Rs3+Rs5$ for Lower arm
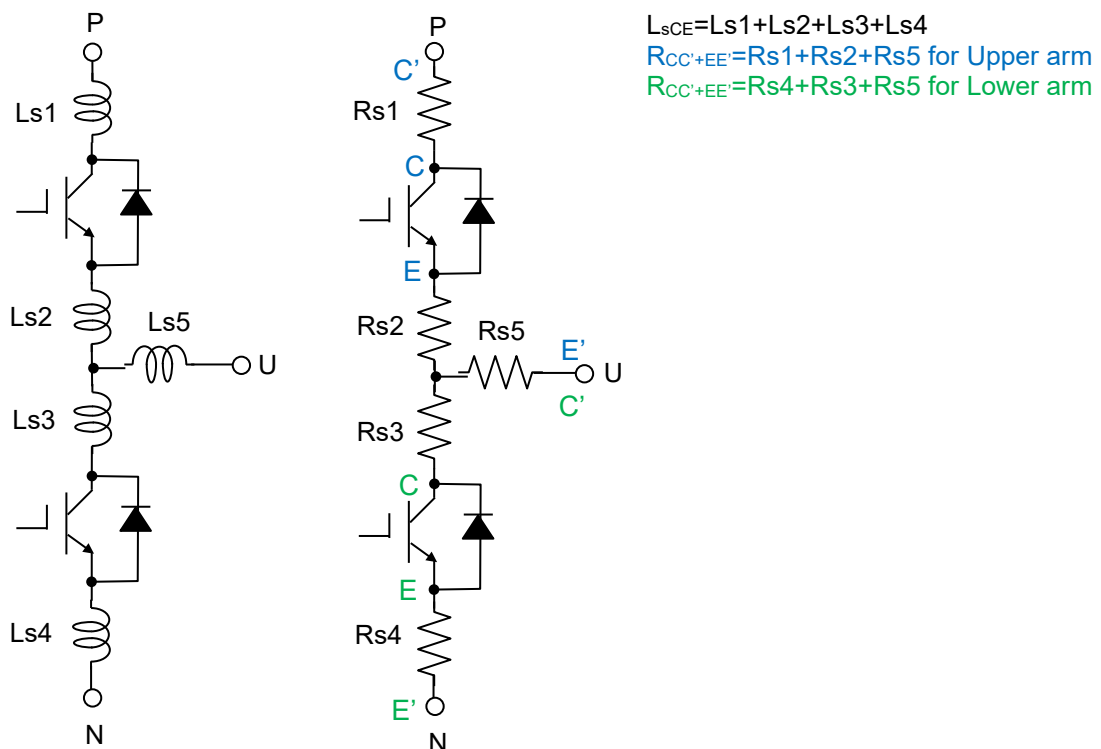
Figure 3-1 Parasitic Inductance/Resistance Schematics

4.   Usage Notes

4.1   Selection of Gate Resistance R_g

The most important factor in driving IGBTs is the selection of the gate resistor, R_g. The minimum requirement for selecting R_g is to keep the surge voltage generated during IGBT switching below the rated voltage. This is explained using the diagrams shown below.

For simplicity, Figure 4-1 shows a diagram of the circuit when switching with an inductive load by extracting one phase of a three-phase inverter circuit. Here, we consider the case where $IGBT_H$ (the high-side IGBT) is turned on and then off while return current I_f flows through the low-side freewheeling diode Di_L. Figure 4-2 shows the resulting switching waveforms.

Figure 4-1   Switching Circuit Diagram

When $IGBT_H$ turns on, I_f of Di_L is commutated to collector current I_c of $IGBT_H$ and decreases. Then, when -V_{ak} (the reverse voltage of Di_L) rises, reverse current I_r flows momentarily due to the residual charge in Di_L, and I_r decreases as the charge disappears. When I_r decreases, voltage $dI_r/d_t \times L_s$ is generated by the back electromotive force (BEF), and this voltage is applied to V_{ak} as a surge on Vbus. This phenomenon is called "diode reverse recovery".

On the other hand, at turn-off, when I_c starts to divert to I_f and I_c decreases, voltage -$dI_c/d_t \times L_s$ is generated and this voltage is added to V_{ce} as a surge voltage to V_{bus}.

The above explains the surge voltage generated when the IGBT turns on and off. There are various factors causing variation in this surge voltage. Figure 4-3 shows the related schematics. The main factors contributing to an increase in surge voltage, in addition to the typical surge voltage, include: (1) variations in IGBT and FWD characteristics, (2) variability in the gate circuit, primarily due to variations in gate voltage and gate resistance, and (3) variations in the stray inductance (Ls) and other factors, although their impact is typically smaller compared to the first two factors. Even considering all these variability factors, it is imperative that the gate drive conditions prevent the surge voltage from exceeding the rated voltage. Furthermore, if simply adding all these variability factors is considered excessive, statistical processing may be a more reasonable solution. The key point is to ensure that, after considering all variabilities, the surge voltage does not exceed the rated voltage across the entire operating temperature range (typically -40°C to 175°C).
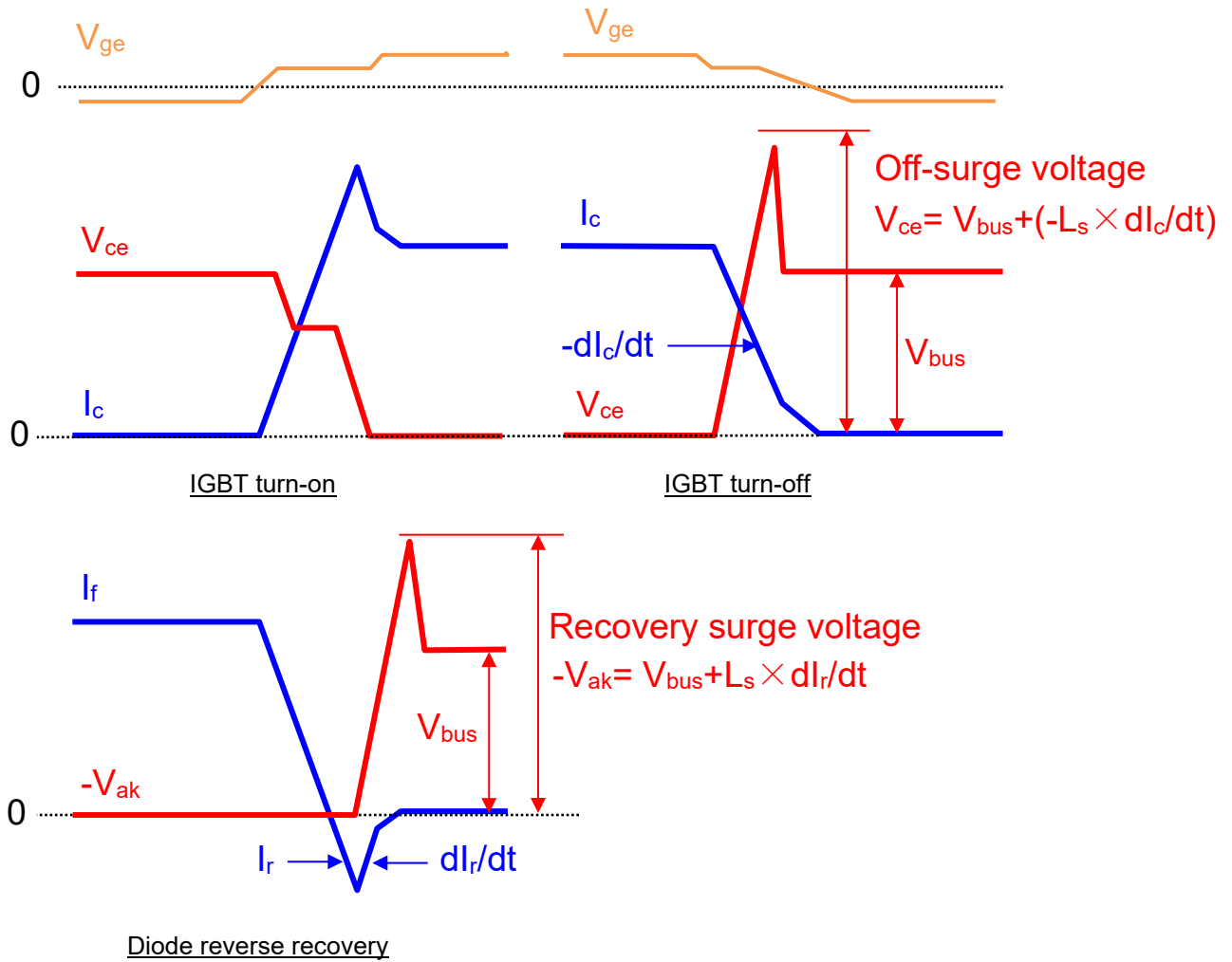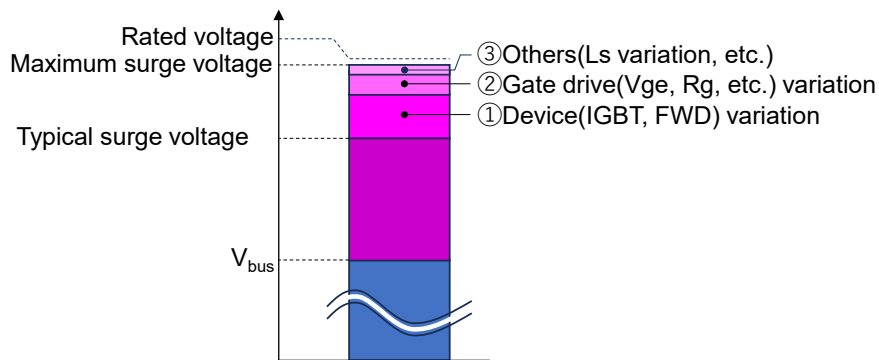
Figure 4-2   Switching Wave Diagram

Figure 4-3   Variability Factors Causing Variation in Surge Voltage (image)

4.2   Dead Time Settings

In an inverter, if the IGBTs on the upper and lower arms are turned on at the same time, no current flows to the load such as the motor, so the IGBTs are directly connected to the power supply, causing an excessive short-circuit current to flow through the upper and lower arms. As a result, the IGBTs are at risk of breakdown. In addition, not only will the IGBTs breakdown, but the destruction may also cause irreversible damage to surrounding components due to scattered module sealing materials, etc. There is also the risk of fire. In short, a short-circuited IGBT can cause a major accident and must be avoided. Therefore, the IGBTs on upper and lower arms should never be turned on at the same time.

Figure 5-1 shows the switching waveform diagram for when the upper and lower arms are short-circuited. In this example, the upper arm IGBT turns on before the lower arm IGBT is completely off. The area covered with red hatching represents the period during which both the upper and lower arm IGBTs are simultaneously on, indicating that a short-circuit current is flowing through the upper and lower arms. This period must be eliminated consider the gate drive conditions.
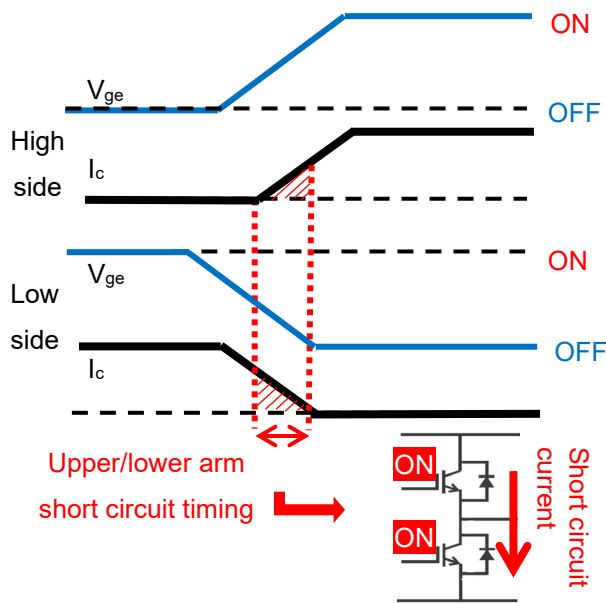
Figure 5-1   Upper/Lower Arm Short Circuit Timing Diagram

As a solution, a period called dead time, during which both the upper and lower arms are off, is introduced in inverter circuits to prevent a short circuit between the upper and lower arms. Figure 5-2 shows the timing diagram for dead time. Periods (2) and (4) in the figure represent dead time periods. To prevent short circuits between the upper and lower arms, the dead time should be as long as possible. However, if the dead time is too long, it can increase the distortion of the output AC current waveform, leading to decreased efficiency and other issues. Therefore, the dead time must be long enough to reliably prevent short circuits between the upper and lower arms, but also as short as possible to minimize the latter issues.
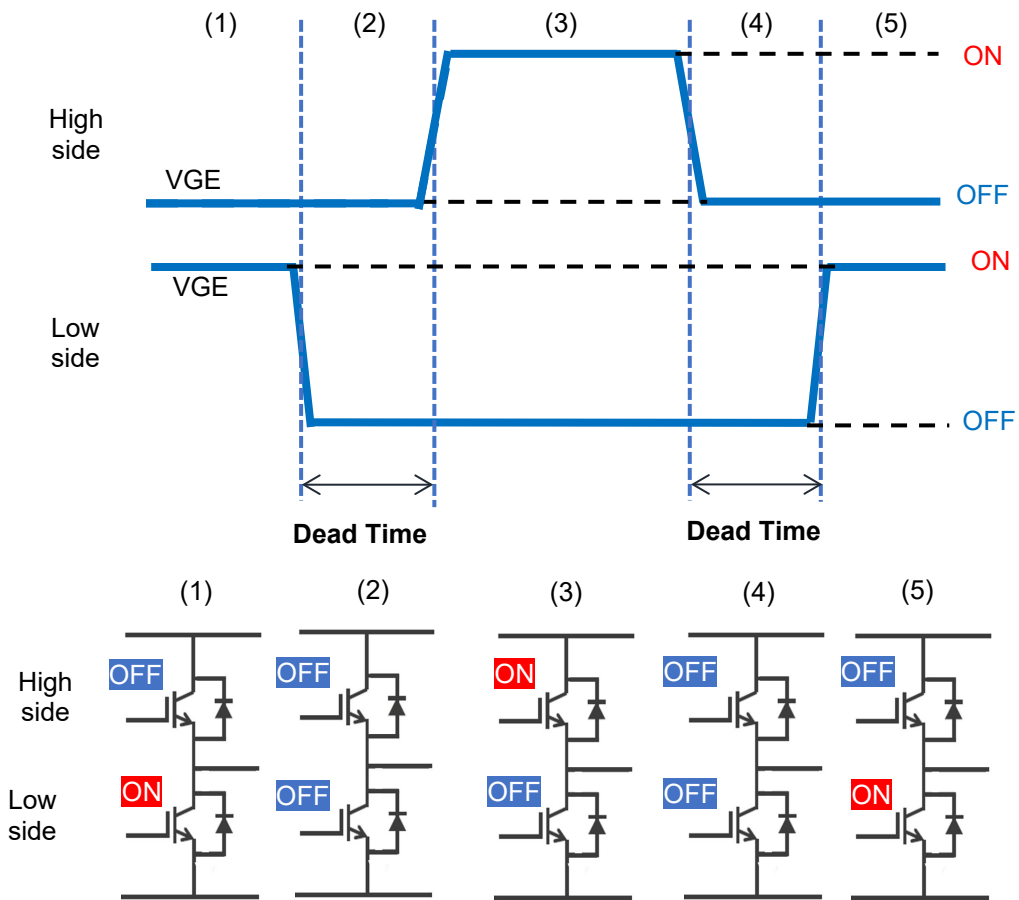
Figure 5-2   Upper/lower Arm On/Off Timing Chart

The dead time should generally be set for longer than the IGBT switching time.

Consideration should be given to Rg and other gate drive conditions, as well as temperature characteristics and other factors which may impact switching time.

4.3   Derating

The absolute maximum ratings explained in section 3.1.1 are instantaneous values determined to prevent damage to a semiconductor device and do not guarantee long-term reliability. In addition, as with similar semiconductor devices, IGBTs and FRDs have a certain probability of defects and failure, which is unavoidable. Therefore, when designing equipment such as inverters, it is necessary to derate the modules according to the target application and expected operating conditions to extend the equipment's reliability and lifespan.

There are no general rules for determining the extent to which voltage, current, temperature and other values should be derated from the rated values of each module for a specific design, as it depends on the device's application, operating conditions, operating environment, and design life. We recommend that the device designer sets standards for deratings based on accumulated design and technical know-how. That said, Table 5-1 offers general derating examples to be used as a reference. In addition, when connecting modules in parallel, the designer must consider the current imbalance between each module while carefully determining the current derating.

Table 5-1   Derating Example

Item	Example of Reduction Rate
Voltage	Use within 70% to 80% of the rated value, including the maximum surge voltage.
Current	Use within 70% to 80% of the rated value, including the maximum surge current.
	Use with the mean current within 50% of the rated value.
Temperature	Use within 70% to 80% of the rated values, including transient temperature rises due to surge voltage, current, etc. Reduce temperature from the rated value further based on expected equipment lifespan.

4.4   Module Protection

In the previous section, we described the importance of derating to ensure that the module operates normally throughout the design life of the equipment. However, this does not eliminate the possibility of damage to the module due to system operation abnormalities, etc. Therefore, to prevent module breakdown, the designer must introduce a module protection function into the equipment to prevent module damage.

Module protection is mainly handled by the gate drive circuit; please refer to the gate drive IC specifications for details when designing the target device. This section explains what to detect, the characteristics to protect, and protection function concepts.

The main types of damage that occur in IGBT modules are as follows: 1) short-circuit damage, 2) overload voltage damage: when a voltage higher than the rated voltage is applied to the collector and/or cathode, 3) overcurrent damage: when excessive current flows through the IGBT and FRD, and 4) overheat damage: when junction temperature $T_{vj\,op}$ exceeds the allowable temperature.

1) **Short-circuit damage protection:** Short-circuit damage occurs not only due to unsuitable dead time settings that upper and lower arms to short circuit, as explained in section 4.2, but also due to output short circuits caused by insulation damage in loads such as motors and ground faults that cause a short circuit with the earth. Therefore, short-circuit damage cannot be prevented by adjusting the dead time alone.

2) **Overvoltage damage protection:** This module does not detect collector current, but rather uses a method of detecting on-voltage when the IGBTs are on. In other words, when the gate voltage is on and the collector potential is high, the module detects a short-circuit condition. Terminals C1 through C6 are used to monitor on-voltage. If a short-circuit condition is detected, the IGBTs must be turned off within the short-circuit withstand time specified in the data sheet to prevent damage to the device. In this case, since the excessive current is turned off, the off-surge voltage in normal off operations will be excessive, which could result in overvoltage breakdown (2).
At this point, overvoltage damage may occur. Therefore, a method known as soft shutdown is generally adopted to reduce the diC/dt and surge voltage by shutting down the device with a large Rg, separate from normal switching Rg.

3) **Overcurrent damage protection:** This is protection for cases where the overcurrent is not as severe as a short-circuit current, but is expected to continue for a long period of time due to overload, etc. The collector current is detected by a current sensor such as a Current Transformer (CT), and after an appropriate filtering time for the detection signal, current limitation and shutdown are implemented. Consideration for surge voltage at shutdown is required in the same way as for short-circuit protection.

4) **Overheat protection:** This is achieved by detecting temperatures using the thermistors mounted on the U, V, and W phases of the module. Terminals T1-T2, T3-T4, and T5-T6 are used for detection. Since IGBT/FRD temperature and thermistor temperature are different, the designer needs to obtain the correlation characteristics between the two in advance and determine the thermistor temperature at which protection will begin, or at which temperature current limitation will begin. Also, note that the thermistor cannot keep up with a sudden rise in IGBT/FRD temperature, and will not function effectively when this occurs.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2024.09.19	-	First edition

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