IGBT

Usage Notes on Gate Drive

Introduction

This document provides notes on gate drive conditions for Renesas IGBT and FRD products.

Contents

1. IGBT DRIVE GATE VOLTAGE

1.1 Recommended gate voltage

Figure 1-1 shows output characteristics of the Renesas JP6831JWS IGBT.

The recommended gate voltage when the IGBT is on is VGE = 15 V.

The effect of gate voltage on operations is as follows.

- When VGE is low:
  Stress resulting from increased loss may damage the device.
- When VGE is high:
  VCE(sat) decreases, resulting in less loss, but short-circuit withstand time (SCWT) decreases and there is greater probability of device damage in the event of a short circuit.
  Surges may cause over-rating, another cause of damage to the device.

The absolute maximum VGES rating is noted on each product datasheet;

always use IGBT within the rating range.

*Exceeding maximum rating may destroy gate oxide film and cause malfunction.

Off-state gate voltage should be set to a negative value (-5 V to -10 V) to prevent false turn on during upper and lower arm operation.

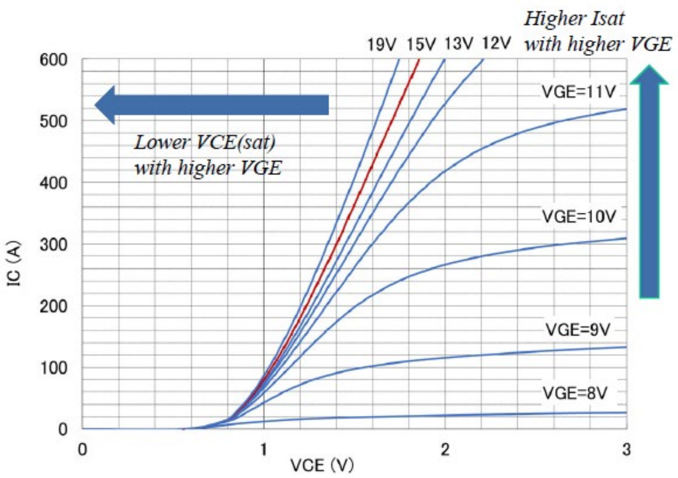


Figure 1-1 VCE - IC characteristics (AE4 RJP6831JWS)

1.2 VCE(sat), short-circuit withstand time (SCWT)

Increasing gate voltage lowers VCE(sat), but also decreases withstand time (tsc) at load short circuit (arm short circuit), as shown in Figure 1-2.

Gate drive voltage must be determined based on the relationship between VCE(sat) and tsc.

Choose the optimum point for your application.

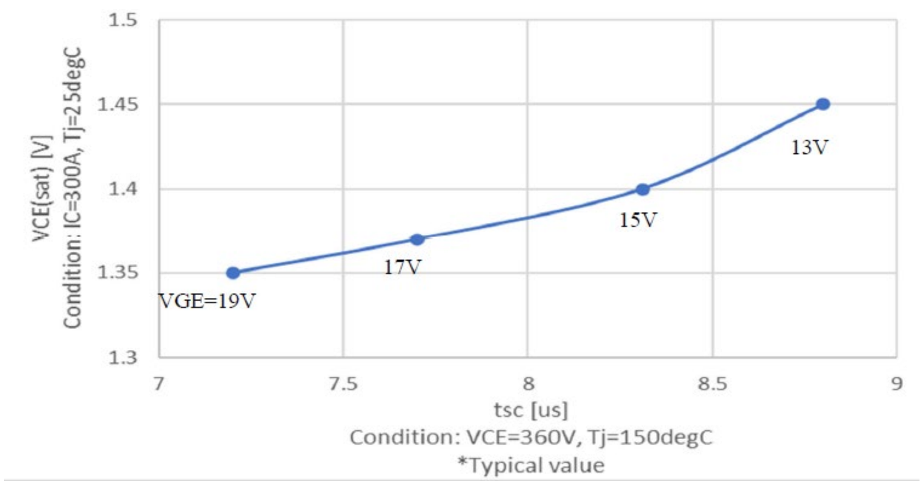


Figure 1-2 tsc - VCE(sat)（AE4 RJP6831JWS）

2. DRIVE CURRENT

Gate current Ig flows because the gate is charged or discharged during IGBT turn-on and turn-off.

If Ig is not sufficiently large, switching speed decreases, and may incur increased loss.

To maximize IGBT switching performance, design the driver circuit with a current capacity sufficient for the Ig (peak) shown below.

∗ When calculating Ig, it is necessary to consider chip built-in resistor rg and internal resistor RS of the driver circuit (Figure 2-1).

$$Ig(peak) = \frac{VGE(on) - VGE(off)}{(RS + Rg + rg)min}$$

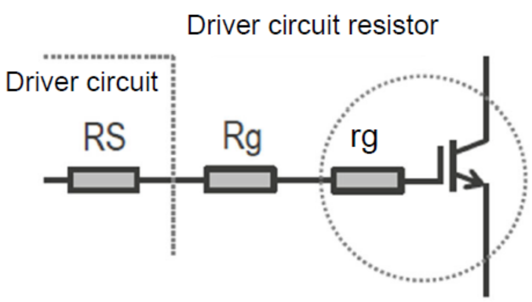


Figure 2-1 Gate Resistors

3. SELECTING GATE RESISTOR Rg

3.1 External gate resistor Rg selection

Gate resistor Rg should be optimally set to enable the most efficient product handling.

As shown in Figure 3-1, the external Rg value may impact characteristics.

- - - Better, - - - Worse

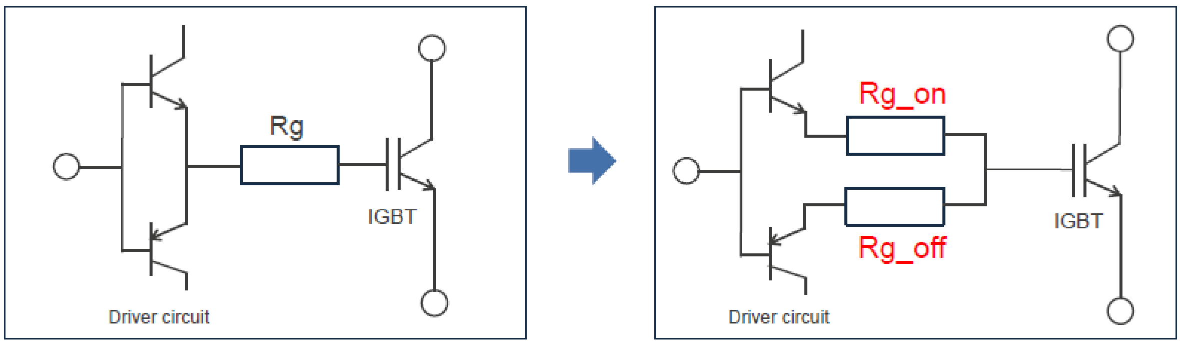
	Switching time	Switching loss	Surge voltage	False turn on	Ringing noise
Small Rg	↘	↘	↗	↗	↗
Big Rg	↗	↗	↘	↘	↘

Figure 3-1 Impact of gate resistance on key characteristics

As indicated above, when selecting Rg, consider the entire configuration, including switching time, switching loss, surge voltage and ringing, as well as the EMI noise of the entire system.

3.2 Turn on/Turn off Rg selection

Although Rg is generally indicated as shown in Figure 3-2(a) below, the product can be used more efficiently by setting two resistors in series, Rg on and Rg off for IGBT turn-on/turn-off, as shown in Figure 3-2(b).



(a) (b)

Figure 3-2 Gate resistor Rg on and Rg off

3.3 Switching time

3.3.1 Switching time (in relation to Rg)

As shown in Figure 3-3, switching time increases as Rg increases, and decreases as Rg decreases.

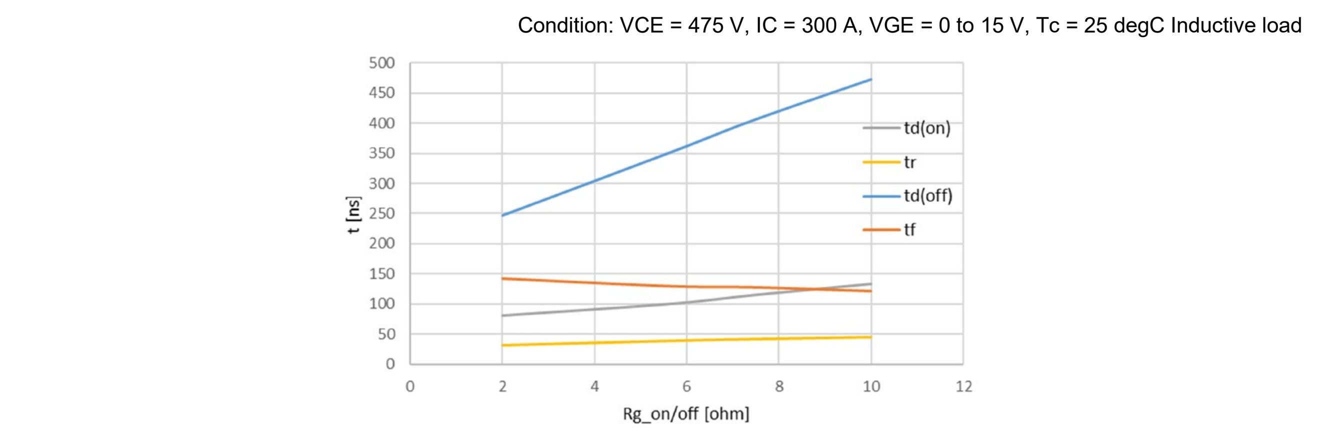


Figure 3-3 Rg vs. switching times (AE4 RJP6831JWS)

Figure 3-4 shows the difference in the waveforms of VGE, VCE, and IC during switching operation at Rg = 2, 10 ohm.

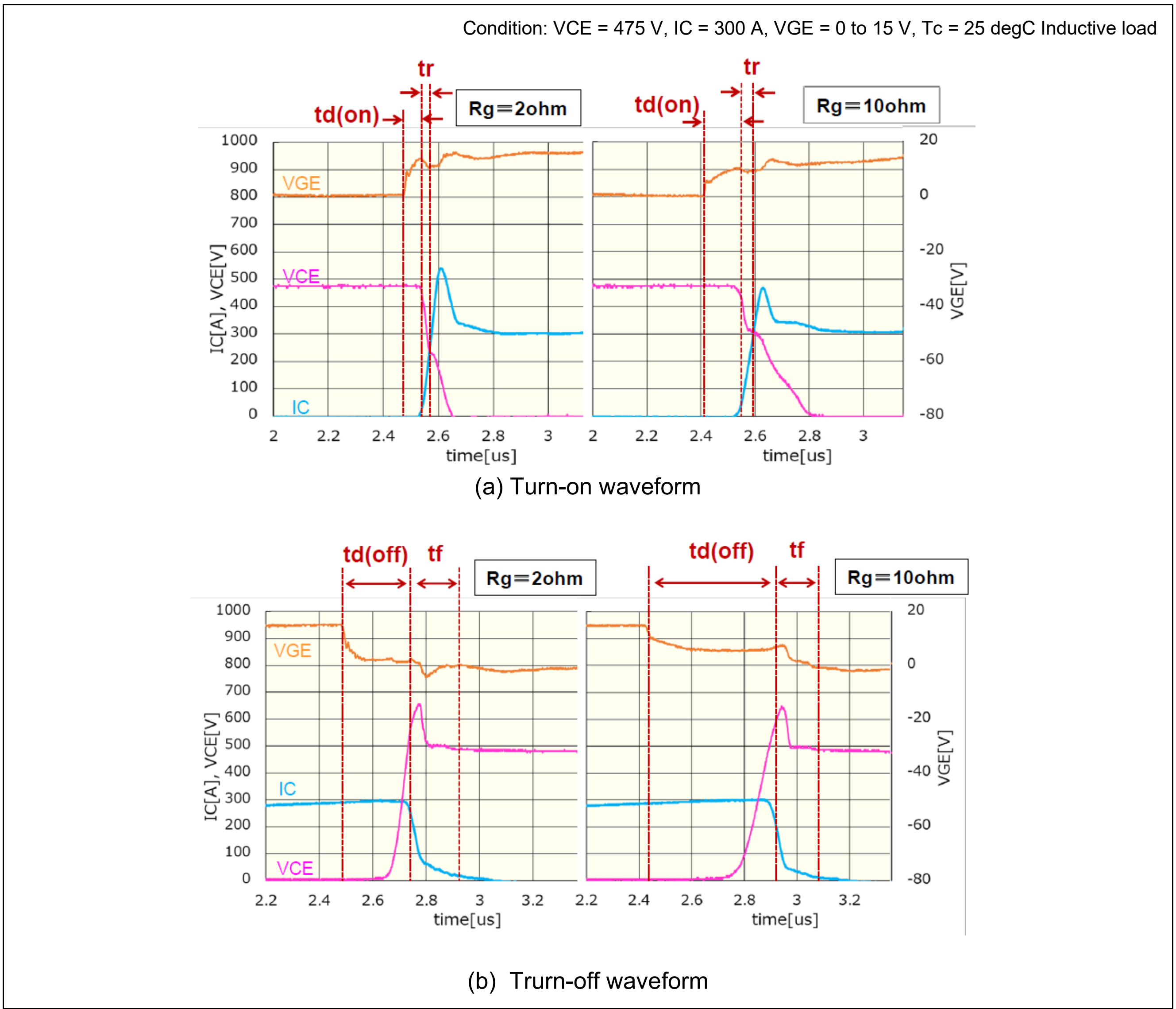


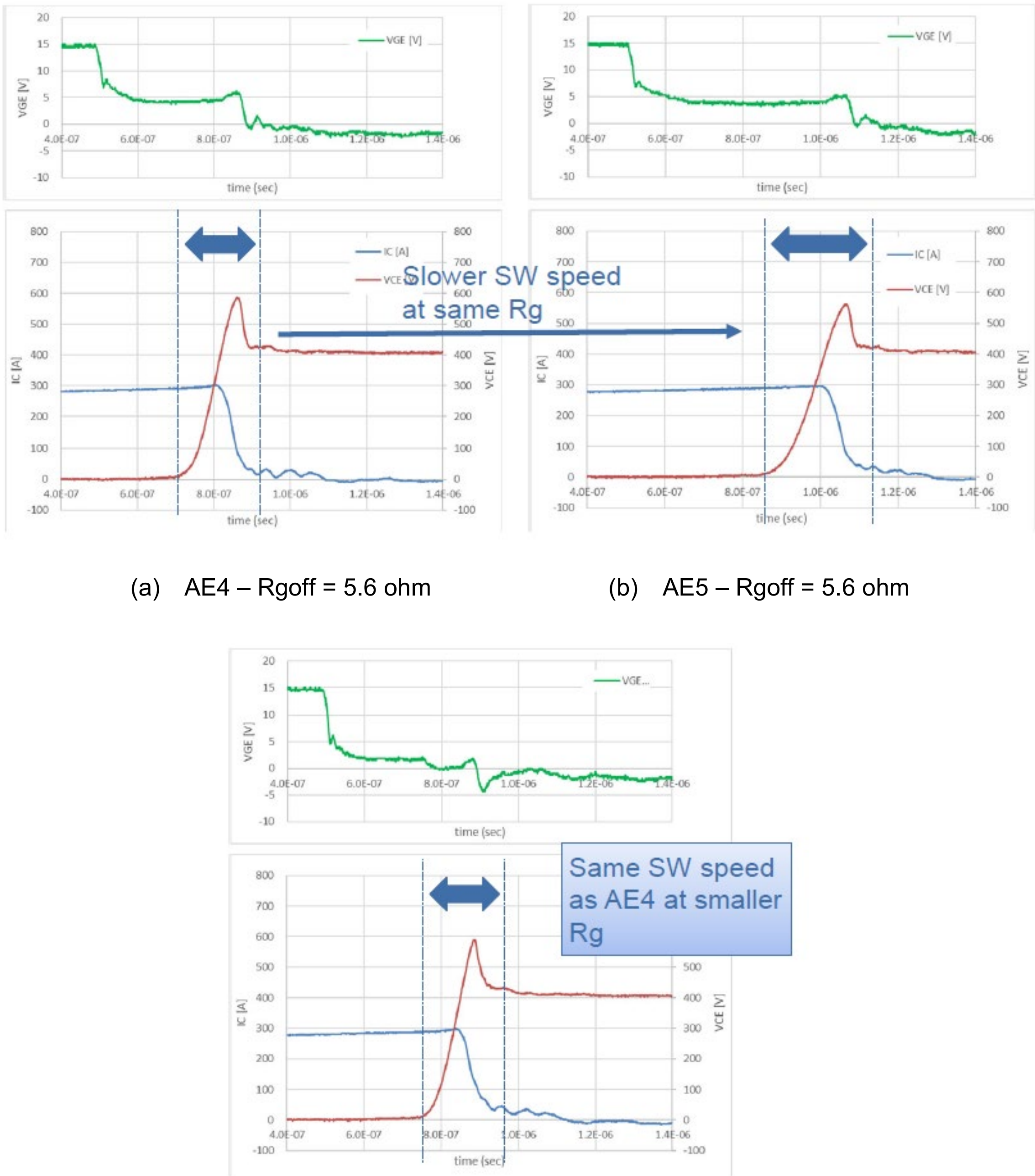
Figure 3-4 VGE, VCE, and IC waveforms during AE4 RJP6831 JWS SW operation

3.3.2 Switching time (comparison of process generations)

Differing IGBT process generations may have considerably different switching characteristics even within the same rating class. The latest-generation Renesas IGBT AE5 for automotive use has a smaller cell size than the current AE4 to reduce conduction loss.

AE5 therefore has higher gate capacitance and slower speed for the same gate resistance (Figure 3-5(a), (b)). A smaller Rg drive is required to achieve the same switching speed as AE4. (Figure 3-5(c))

When considering products of differing process generations, optimize drive conditions such as gate resistance according to the switching characteristics of each product.



(a) AE4 – Rgoff = 5.6 ohm

(b) AE5 – Rgoff = 5.6 ohm

(c) AE5 – Rgoff = 2.0 ohm

Figure 3-5 Renesas AE4/AE5 turn-off waveform comparison

3.3.3 Switching time (dead time)

As shown in Figure 3-6, a dead time must be set for the on/off switching timing in inverter circuits to prevent a short circuit between the upper and lower arms.

The dead time should generally be set for longer than the IGBT switching time.

Consideration should be given to Rg and other gate drive conditions, as well as temperature characteristics and other factors which may impact switching time.

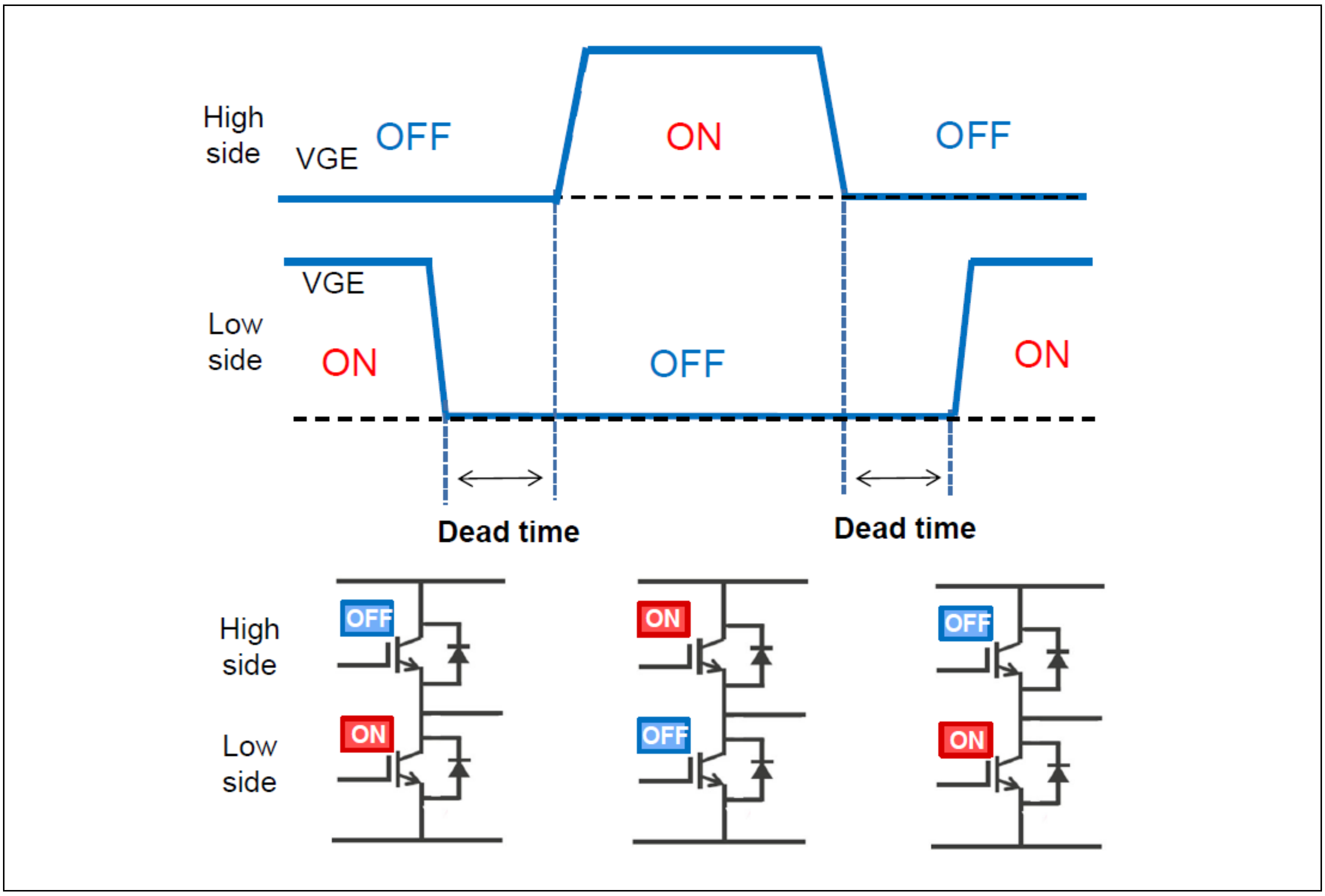


Figure 3-6 Upper/lower arm operation timing chart

Be careful with dead time settings when increasing the Rg value.

As shown on pp. 4-5, increasing Rg_on also increases td(on) and tr; similarly, increasing Rg off increases td(off) and tf.

As shown in Figure 3-7, extended switching time may cause an overlap between the ON time of the upper/lower arms, resulting in a short circuit between the two arms.

In the worst case, the heat produced by the short circuit current may damage the product. Therefore, set a generous dead time t to prevent short circuits. Also, carefully consider td(off), because it is greater than td(on), tr, and tf, and it has a high dependence on Rg (Figure 3-3).

While keeping the above in mind, make sure you set the most appropriate margin, as a long dead time will decrease efficiency and limit operating frequency.

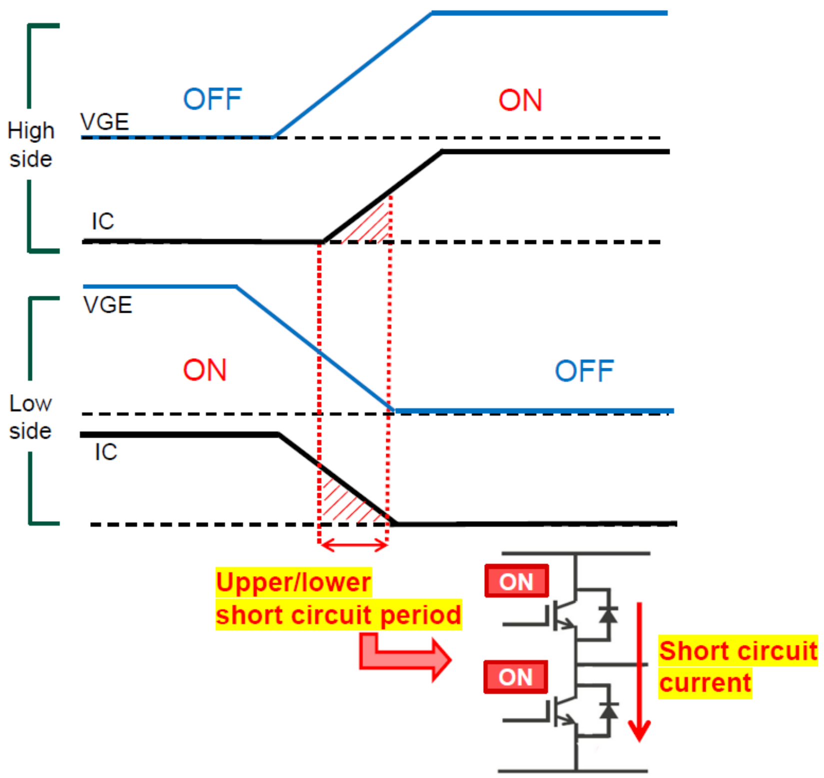


Figure 3-7 Upper/lower short circuit waveform example

3.4 Switching loss

Figure 3-8 shows the relationship between Rg and switching loss.

Increasing gate resistance normally extends switching time and increases switching loss.

Selecting low gate resistance speeds up switching time and reduces switching loss, but surges and ringing generated by di/dt and dv/dt may cause problems due to product damage and malfunctions, noise.

When selecting Rg, consider the trade-off between switching loss and surges, ringing.

Careful selections are advised.

Condition: VCE = 475 V, IC = 300 A, VGE = 0 to 15 V, Tc = 25 degC Inductive load

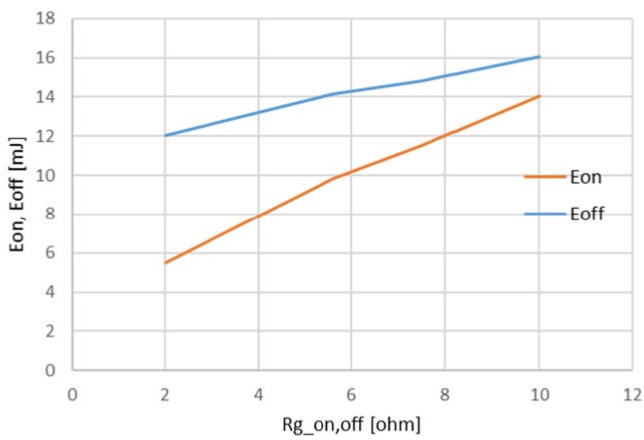


Figure 3-8 Relationship between Eon/Eoff and Rg (AE4 RJP6831JWS)

3.5 Surge voltage

3.5.1 Surge voltage (turn off)

Surge voltage generated at turn-off depends on the collector current di/dt value as shown in Figure 3-9.

As mentioned earlier, decreasing Rg_off reduces Eoff, but causes off-surge voltage to increase as the di/dt value increases.

Figure 3-10 shows the relationship between off-surge voltage and Eoff. This relationship causes a tradeoff between surge and Eoff in Renesas AE4 products.

Make sure turn-off surge voltage does not exceed rated voltage. At the same time, consider the effect on loss when adjusting Rg_off.

Condition: VCE = 475 V, IC = 300 A, VGE = 0 to 15 V, Tc = 25 degC Inductive load

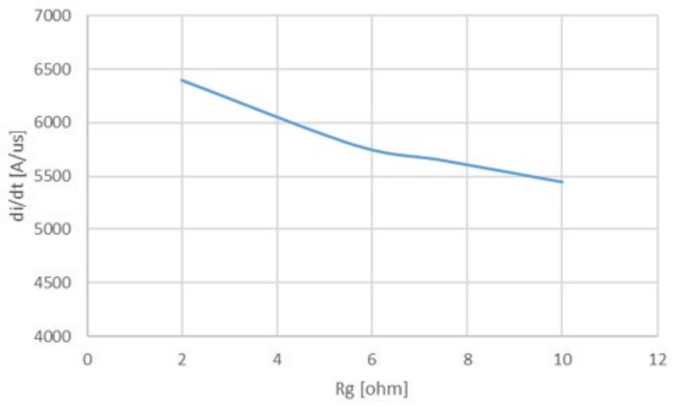


Figure 3-9 Rg vs. di/dt (AE4 RJP6831JWS)

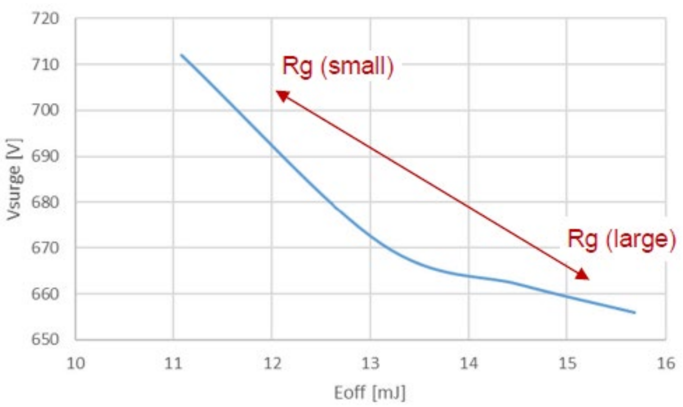


Figure 3-10 Eoff vs. surge (AE4 RJP6831JWS)

3.5.2 Surge voltage (FRD recovery operation)

The recovery current produced by the FRD recovery operation (Figure 3-11) generates a recovery surge at Vak.

As shown in Figure 3-12, there is a proportional relationship between di/dt and the recovery current.

A steep di/dt may generate a surge which exceeds the rating and increases the chance of damage to the device.

Rg should therefore be adjusted with due consideration to the effect on loss.

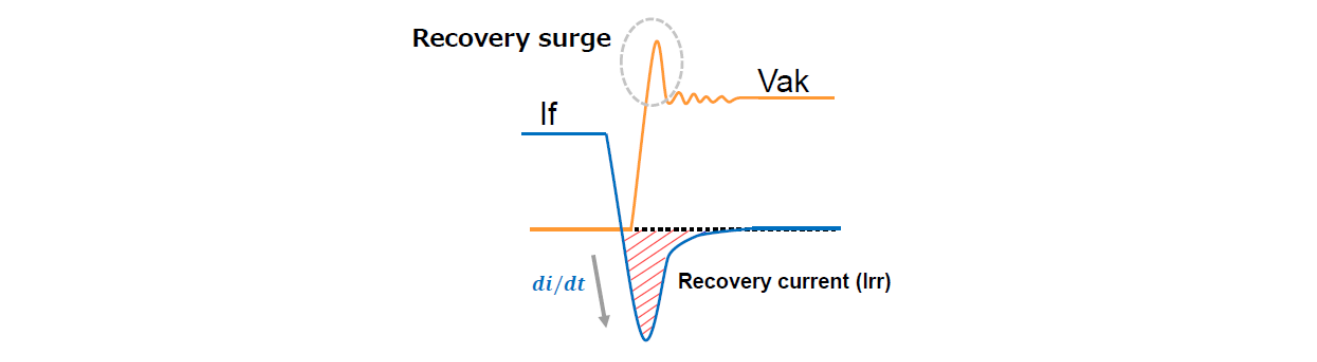


Figure 3-11 FRD waveform during recovery operation

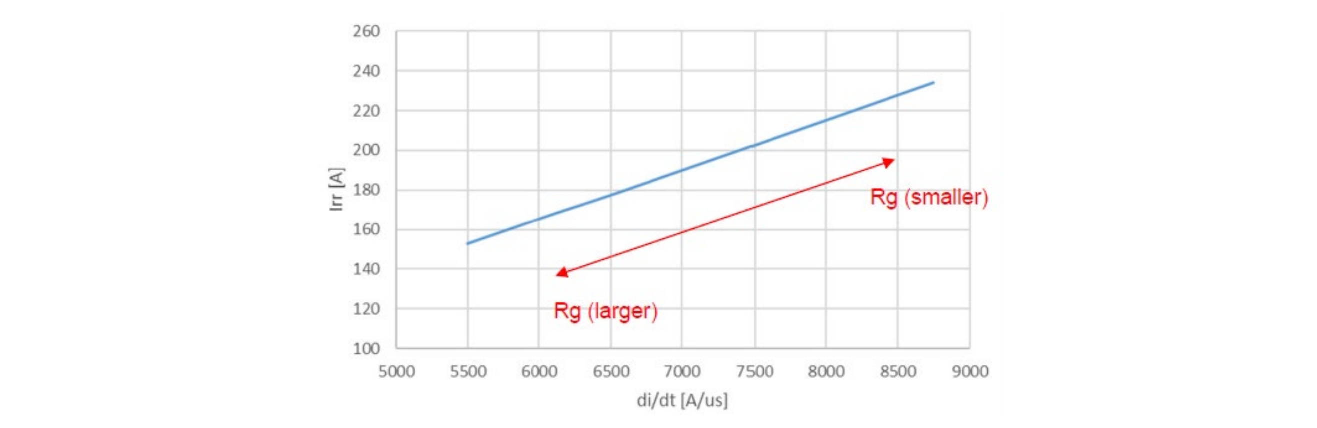


Figure 3-12 Relationship between di/dt and recovery current

3.6 False turn on

As shown in Figure 3-13, when IGBT1 is turned on, the IGBT2 Vce rises rapidly. The IGBT2 Cgc yields a displacement current i from the collector to the gate.

$$i = Cgc \times dv/dt$$

Current i pushes up Vge through gate resistor Rg2, and if dv/dt is steep, it generates a surge in Vge (Figure 3-14).

If the surge exceeds Vge(off), a false ignition occurs at IGBT2.

This can be prevented by setting IGBT off voltage to a negative value (-5 to -10V) as described on p. 2, which will increase Rg.

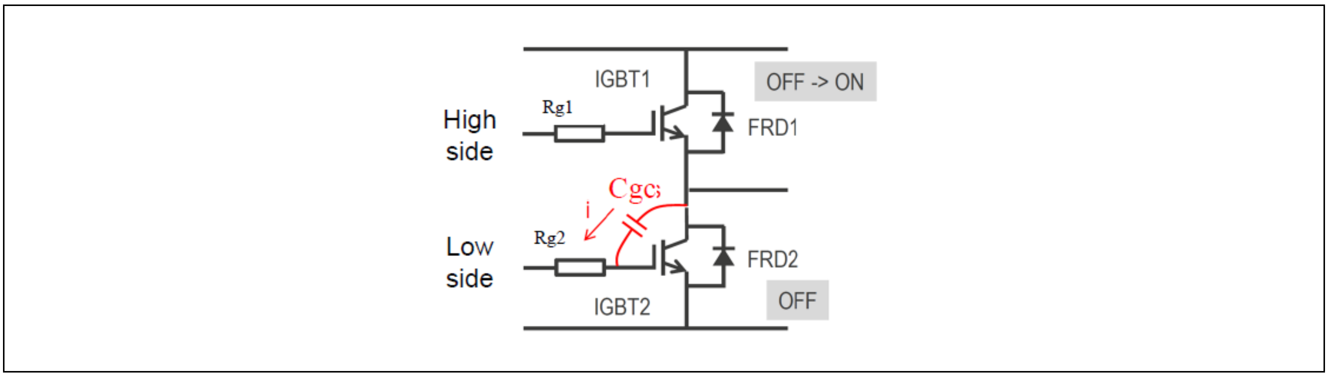


Figure 3-13 Parasitic capacitance during upper/lower arm operation

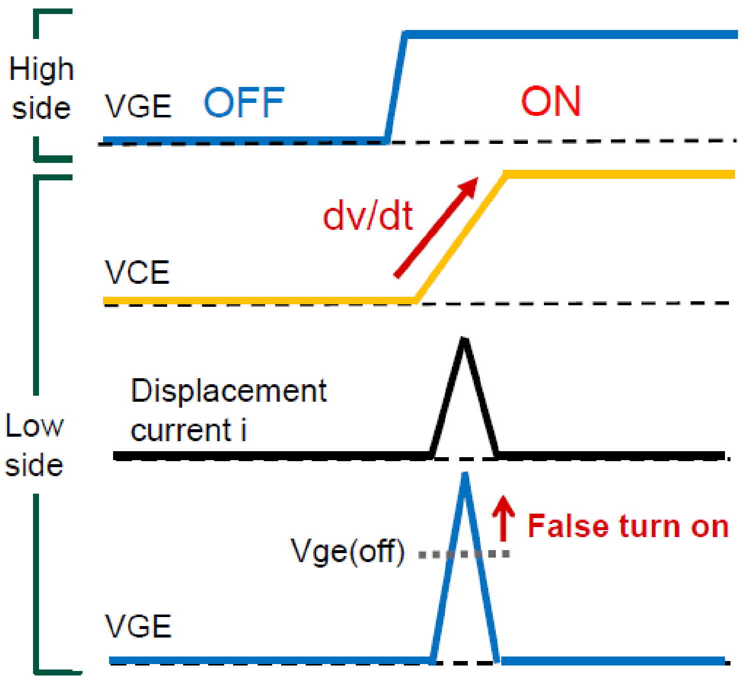


Figure 3-14 Surges during upper/lower arm operation

3.7 Ringing

3.7.1 Ringing and other noise (parasitic component)

Noise such as ringing may occur during switching if wiring inductance and other parasitic components of an IGBT circuit are high.

Ringing may be suppressed by increasing gate resistance.

In paralleled usage, suppress ringing by connecting individual gate resistors.

Click Usage Notes for Paralleled IGBT for more information.

Renesas offers a lineup of anti-ringing products with the built-in rg shown in Figure 3-15.

See individual product data sheets for more details.

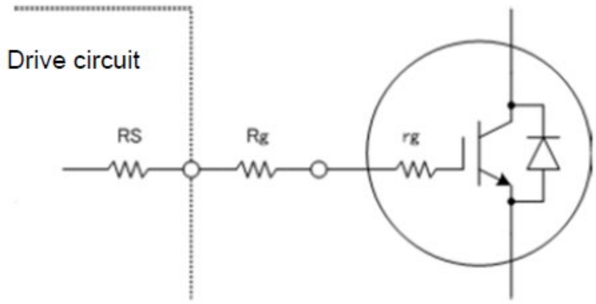


Figure 3-15 Drive circuit resistance components

3.7.2 Ringing (FRD recovery operation during low current)

Figure 3-16 shows low-current recovery waveforms for competitor products. In the FRD recovery operation at low current, the recovery current tends to decrease faster, while the simultaneous steep surge voltage may cause ringing.

Ringing can be suppressed by increasing Rg. Renesas AE4 and AE5 FRDs boast an advantage here, as Rg_on can be suppressed to a smaller value than that of competitor products. (Figure 3-17)

Ultimately, Rg must be set based on EMI noise considerations.

Condition: VCE = 400 V, IF = 5 A, VGE = 0 to 15 V, Tc = 25 degC Inductive load

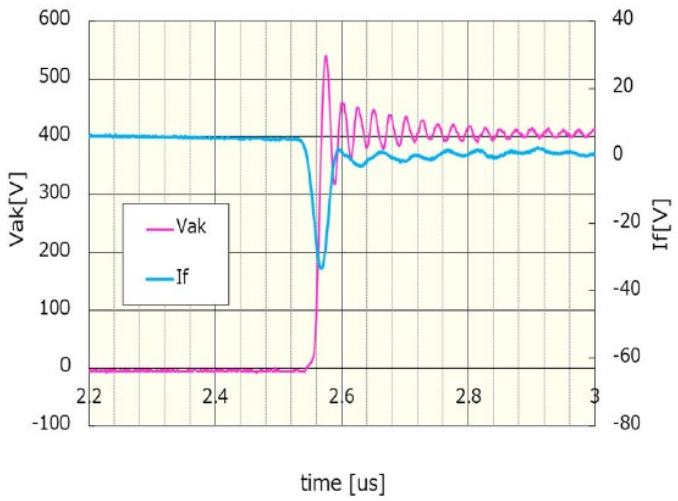


Figure 3-16 Low-current recovery surge for competitor products

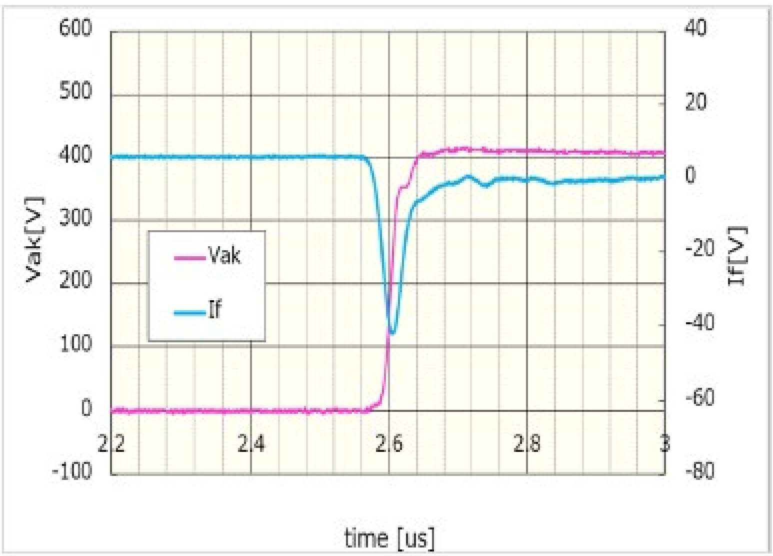


Figure 3-17 Low-current recovery surge for AE4 and AE5 FRDs

Appendix: Definitions

Gate charge

Like MOSFETs, IGBTs have a parasitic capacitance component.

The capacitance component shown in Figure 4-1 is an important parameter determining drive current and driver circuit power loss.

- Qge charge period
  Qge is required to charge VGE (Cge), which is required for the collector current to flow.
  Qgc charge period
  Qgc is required to charge Cgc. During this period, the Miller effect causes the apparent capacitance to increase, while VGE change appears flat.
  VCE decreases to VCE(sat) during this period.
- Qg charge period
  Qg is the ultimate amount of charge required to bring VGE to 15V.
  It is the amount of charge required to turn on the IGBT completely.

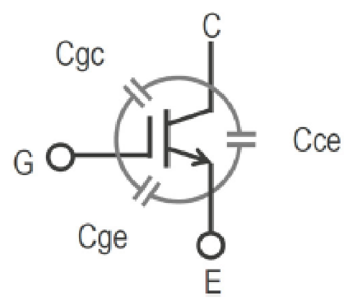


Figure 4-1 Target parasitic capacitance

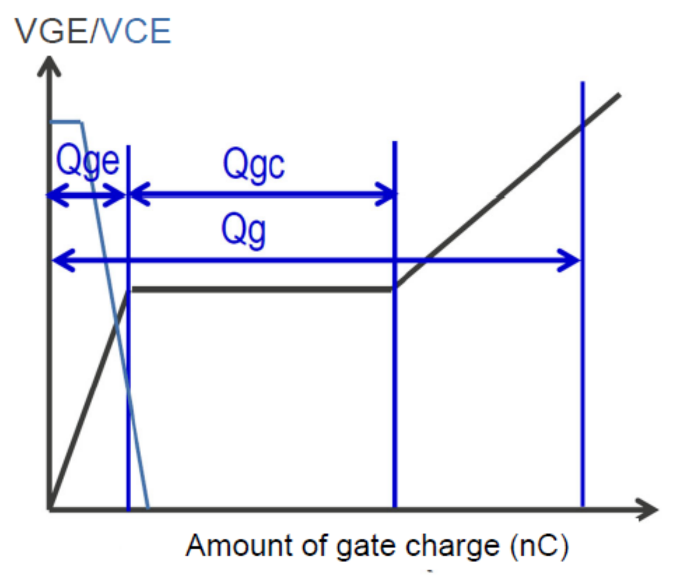


Figure 4-2 Relationship of gate charge and VGE/VCE

Switching characteristics

IGBTs are used as switches in power conversion.

Switching characteristics are measured using the switching characteristic measurement circuit shown in Figure 4-3.

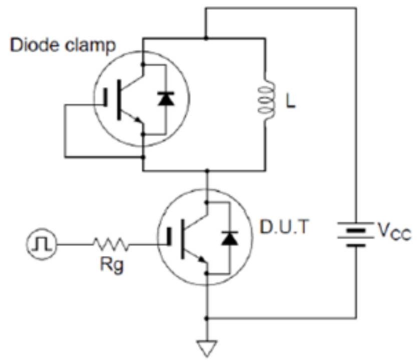


Figure 4-3 Switching characteristic measurement circuit

Important parameters in switching characteristics are described on the following page.

Switching characteristics (switching time)

- td(on): turn-on delay time
  Time for the gate-emitter voltage to rise from 10% of the forward-bias voltage to 10% of the Collector current
- tr: rise time
  Time for the collector current to rise from 10% to 90%
- td(off): turn-off delay time
  Time for the gate-emitter voltage to fall from 90% of the forward-bias voltage to 90% of the collector current
- tf: fall time
  Time for collector current to fall from 90% to 10%

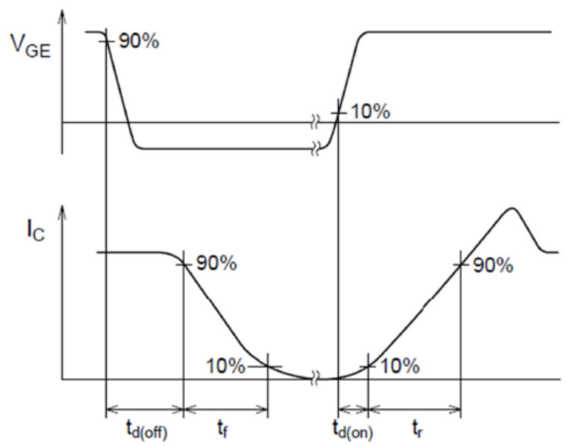


Figure 4-4 Switching waveforms

Switching characteristics (switching loss)

Switching loss is shown in Figure 4-6.

Off-period loss can be calculated as VCE x IC.

Calculating IGBT loss is extremely important for estimating the application’s power consumption and junction temperature Tj.

Turn-on loss energy	Eon	Integral value of collector loss that occurs from the start of turn-on until the collector-emitter voltage reaches the specified value
Turn-off loss energy	Eoff	Integral value of collector loss that occurs from the start of turn-off until the collector-emitter voltage reaches the specified value
Switching loss energy	Etotal	Sum of Eon and Eoff

Figure 4-5 Definition of switching loss terms

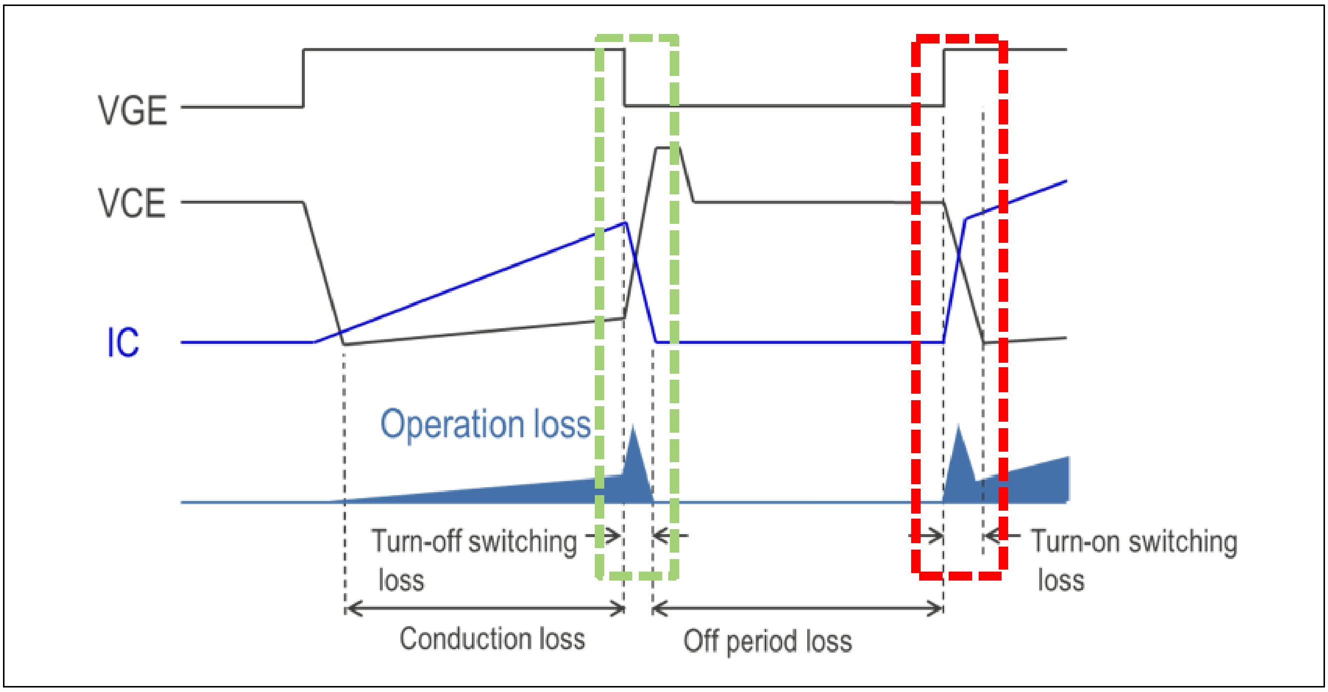


Figure 4-6 Switching loss

di/dt and surge voltage

di/dt refer to the change in current during the switching transition period.

The recovery current converges rapidly during FRD operation, while the steep di/dt causes a surge voltage at the parasitic inductance.

$$V_{surge} = L \times di/dt$$

The surge voltage caused by high voltage and high current is considerable, a key point as this can cause damage to the product if the rated value is exceeded.

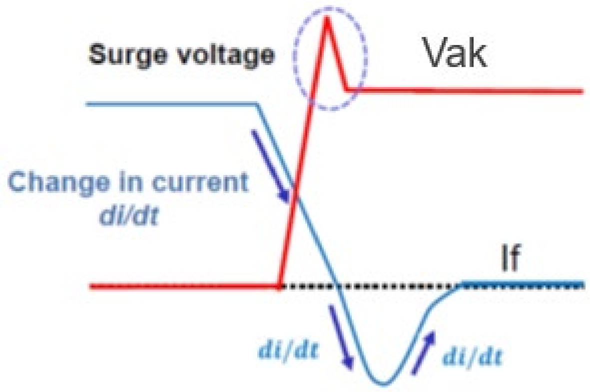


Figure 4-7 Surge voltage and di/dt

Ringing

As shown in Figure 4-8, ringing is the phenomenon in which the waveform oscillates compared to the ideal waveform.

While ringing may be caused by several factors, this document focuses on two factors: parasitic components and FRD recovery operation.

- Ringing caused by parasitic components
  Ringing can be caused by parasitic components such as parasitic inductance of conductors and the parasitic capacitance of IGBTs (Figure 4-9).
  Designing the wiring as short as possible is an essential countermeasure.
  Click Usage Notes for Paralleled IGBT for more information on ringing (gate oscillation) in paralleled operation.
- Ringing caused by FRD recovery operation at low current
  Ringing occurs due to steep current convergence caused by the recovery current during FRD recovery operation at low current (Figure 4-10).

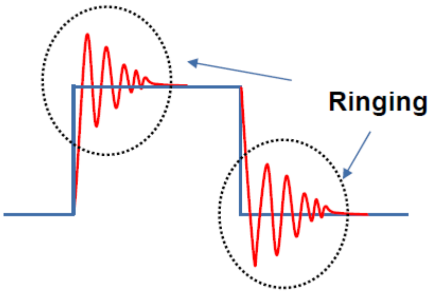


Figure 4-8 Ringing

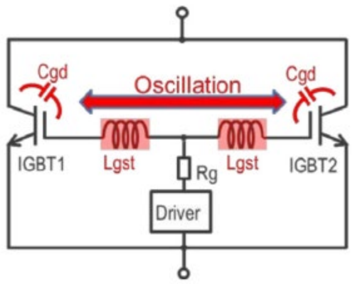


Figure 4-9 Circuit parasitic components

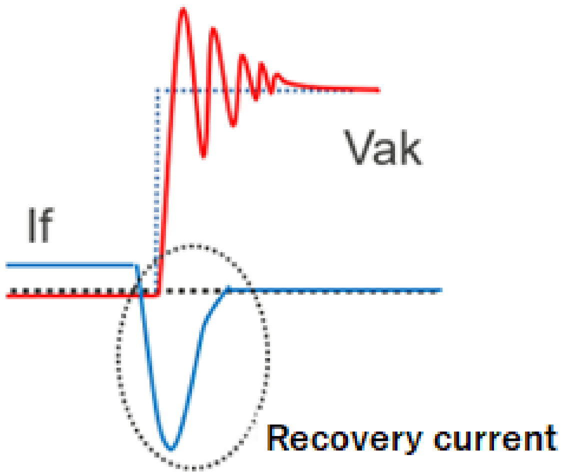


Figure 4-10 Ringing caused by recovery current at low current

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2024/10/01	-	First edition

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