M16C/63, 64A, 64C, 65, 65C, 6C, 5LD, 56D, 5L, 56, 5M, and 57 Groups

Determining Commercial Power Frequency

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Abstract

This document describes how to determine a 50 Hz or 60 Hz commercial power frequency using timer A event counter mode with the M16C/63, 64A, 64C, 65, 65C, 6C, 5LD, 56D, 5L, 56, 5M, and 57 Groups.

Products

M16C/63, 64A, 64C, 65, 65C, 6C, 5LD, 56D, 5L, 56, 5M, and 57 Groups

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

A zero-crossing signal is output using a zero-crossing detector from an AC power input voltage. The output zero-crossing signal is input to the TA0IN pin, and its rising edge is counted. Rising edges are counted for 1 second, then a 50 Hz or 60 Hz commercial power frequency is determined. Timer A0 event counter mode is used to count the number of rising edges.

Table 1.1 lists the Peripheral Functions and Their Applications. Figure 1.1 shows the Connection Example, and Figure 1.2 shows Detecting Zero-Crossing of AC Power Voltage.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
Timer (timer A0)	Counts rising edges of zero-crossing signals using event counter mode
Timer (timer A1)	Measures time to operate timer A0 (1 second)

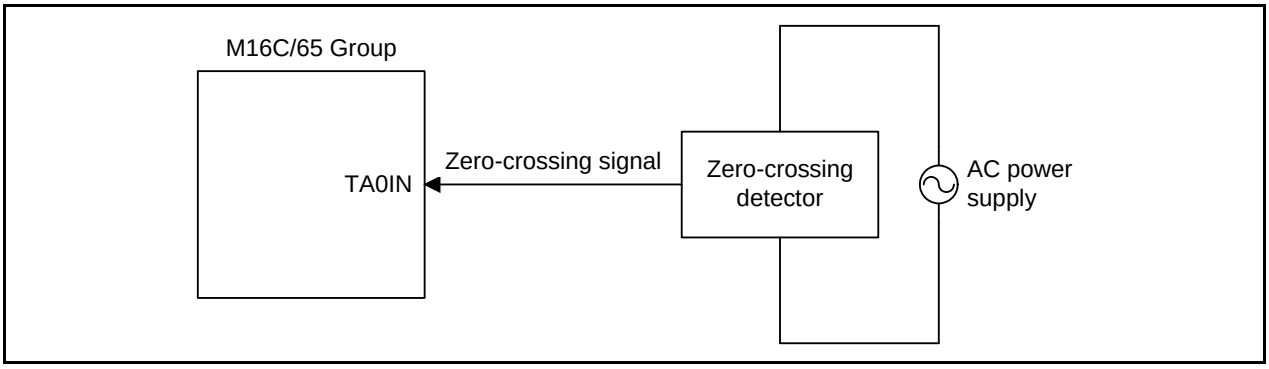

Figure 1.1 Connection Example

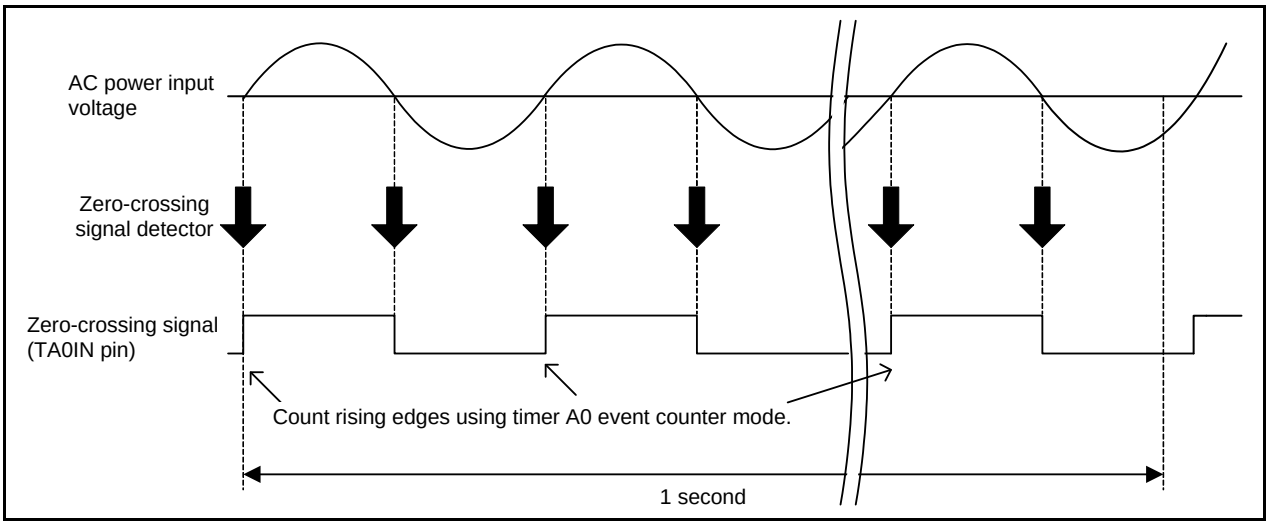

Figure 1.2 Detecting Zero-Crossing of AC Power Voltage

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	M16C/65 Group
Operating frequencies	• XIN Clock: 8 MHz • CPU clock: 32 MHz (PLL operation mode: divided by 2, multiplied by 8)
Operating voltage	5 V (available between 2.7 to 5.5 V)
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.09
C compiler	Renesas Electronics Corporation M16C Series/R8C Family C Compiler V.5.45 Release 01
	Compile options -c -finfo -dir "$(CONFIGDIR)" (The default setting is used in the integrated development environment.)
Operating mode	Single-chip mode
Sample code version	Version 1.00

3. Hardware

3.1 Pin Used

Table 3.1 lists the Pin Used and Its Function.

Table 3.1 Pin Used and Its Function

Pin Name	I/O	Function
P7_1/TA0IN	Input	Inputs zero-crossing signals from the zero-crossing detector

4. Software

Timer A0 (event counter mode) and timer A1 (timer mode) are used in the sample code. Count the rising edges of zero-crossing signals for 1 second, and determine whether commercial power frequency is 50 Hz or 60 Hz according to Table 4.1.

Table 4.1 Frequencies and Determinations in the Sample Code

Number of Edges Counted for 1 Second	Determination
Less than or equal to 44	Error
More than or equal to 45, and less than or equal to 54	50 Hz
More than or equal to 55, and less than or equal to 64	60 Hz
More than or equal to 65	Error

Setting conditions for timers A0 and A1 are listed below.

Table 4.2 Timer A0 Setting Conditions

Item	Setting
Operation mode	Event counter mode
Count source	External signal that is input to the TA0IN pin (rising edges)
Count operation	Increment
TA0IN pin function	Count source input

Table 4.3 Timer A1 Setting Conditions

Item	Setting
Operation mode	Timer mode
Count source	f64TIMAB
Count operation	Decrement

4.1 Operation Outline

(1) Initialize the CPU.
Set the PLL clock divided by 2, and multiplied by 8 as the CPU clock.
(2) Initialize timers A0 and A1.
Set timer A0 to event counter mode, and timer A1 to timer mode.
(3) Start counting timers A0 and A1.
(4) Count rising edges of zero-crossing signals for 1 second.
Measure 1 second with timer A1, and count the rising edges of input zero-crossing signals for 1 second with timer A0.
(5) Determine commercial power frequency.
Determine commercial power frequency using the timer A0 register value.

Figure 4.1 shows the Operation Outline.

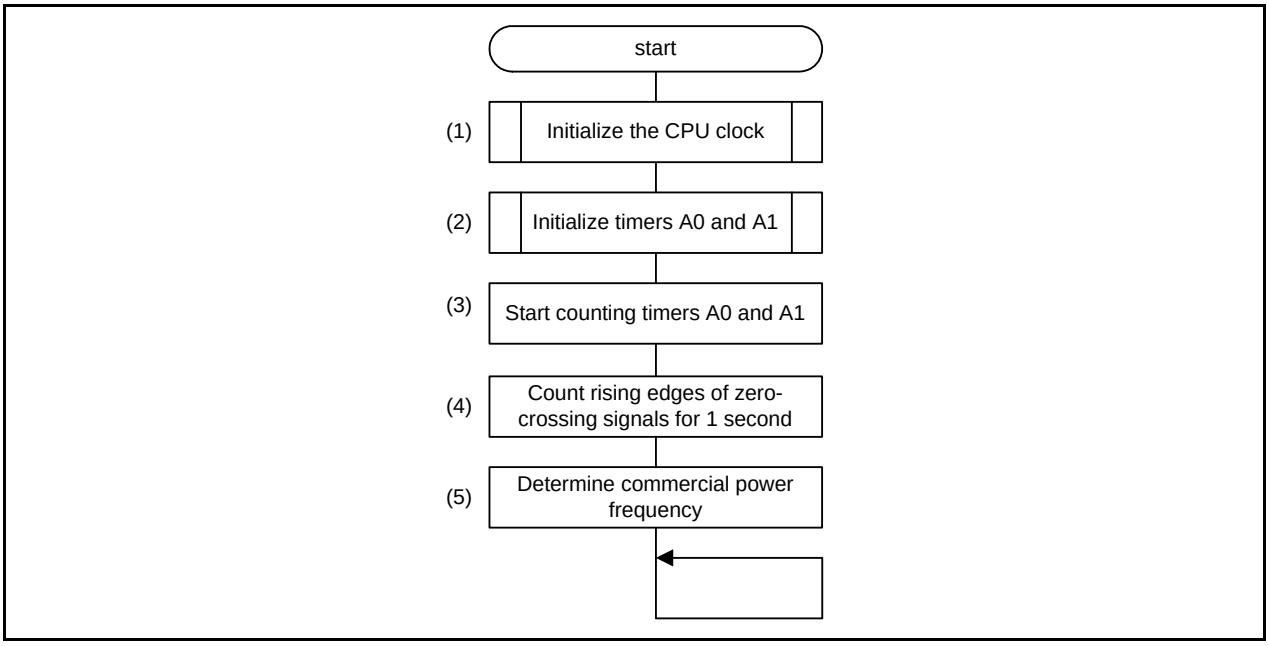

Figure 4.1 Operation Outline

4.2 Required Memory Size

Table 4.4 lists the Required Memory Size.

Table 4.4 Required Memory Size

Memory Used	Size	Remarks
ROM	239 bytes	In the r01an0806_src.c module
RAM	4 bytes	In the r01an0806_src.c module
Maximum user stack usage	10 bytes	
Maximum interrupt stack usage	18 bytes	

The required memory size varies depending on the C compiler version and compile options.

4.3 Constants

Table 4.5 lists the Constants Used in the Sample Code.

Table 4.5 Constants Used in the Sample Code

Constant Name	Setting Value	Contents
TA1_1S	10	For measuring 1 second
TA1_100MS	(50000 - 1)	Timer A1 register setting value
HZ_JDG_ERR	FFh	The determination is an error.
HZ_JDG_50	01h	The determination is 50 Hz.
HZ_JDG_60	02h	The determination is 60 Hz.

4.4 Variables

Table 4.6 lists the Global Variables.

Table 4.6 Global Variables

Type	Variable Name	Contents	Function Used
unsigned char	cnt_ta1_100ms	100 ms counter	main
unsigned short	cnt_result	Store the timer A0 register value.	main
unsigned char	hz_jdg	Store the determination result.	main

4.5 Functions

Table 4.7 lists the Functions.

Table 4.7 Functions

Function Name	Outline
main	Main processing
mcu_init	CPU initialization
peripheral_init	Peripheral function initialization

4.6 Function Specifications

The following tables list the sample code function specifications.

mcu_init	
Outline	CPU initialization
Header	None
Declaration	void mcu_init(void)
Description	Set the PLL clock divided by 2, and multiplied by 8 as the CPU clock.
Argument	None
Returned value	None
Remark	

peripheral_init	
Outline	Peripheral function initialization
Header	None
Declaration	void peripheral_init(void)
Description	• Timer A0: Set to event counter mode. • Timer A1: Set to timer mode.
Argument	None
Returned value	None
Remark	

4.7 Flowcharts

4.7.1 Main Processing

Figure 4.2 shows the Main Processing.

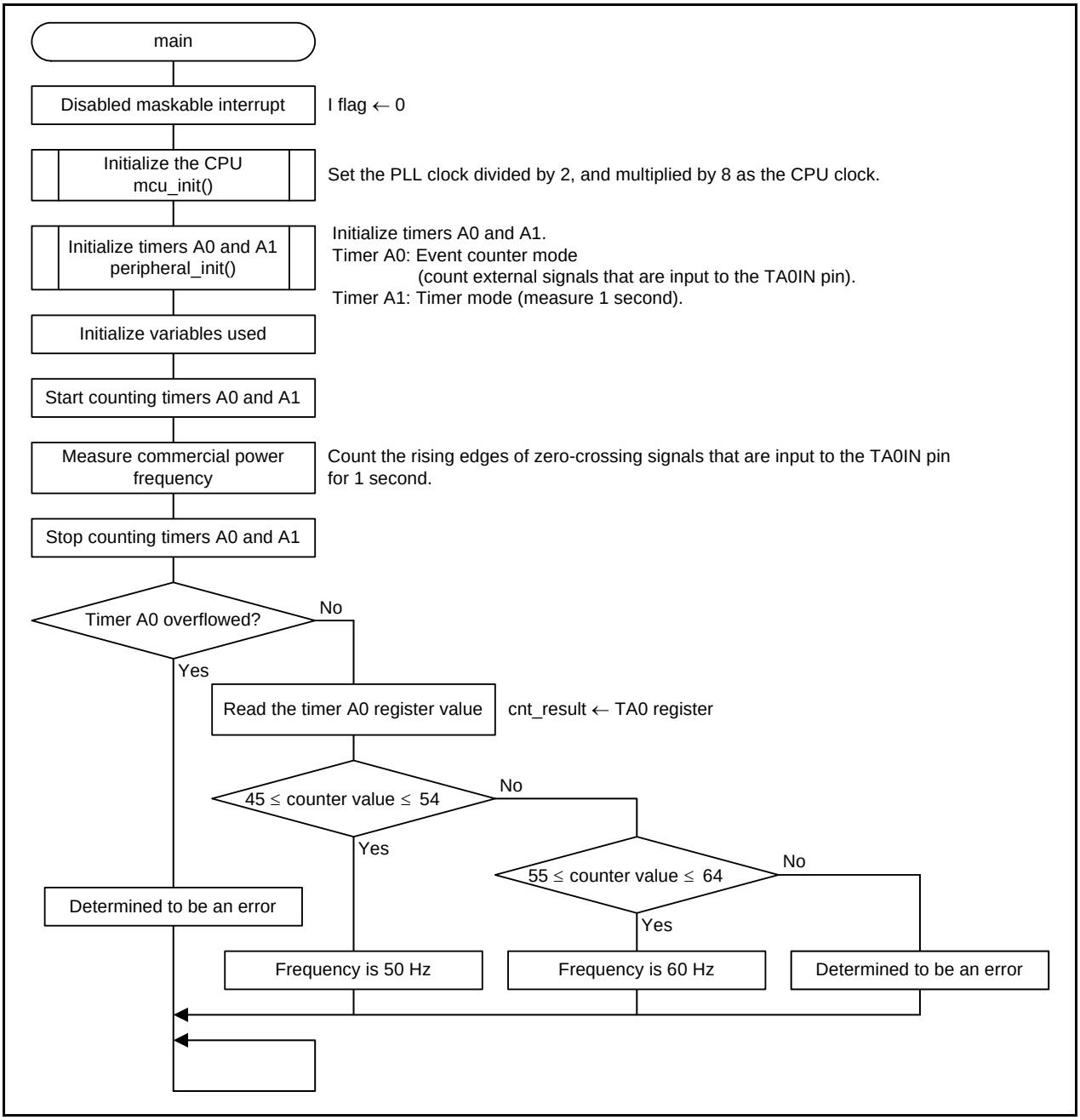

Figure 4.2 Main Processing

4.7.2 Peripheral Function Initialization

Figure 4.3 shows the Peripheral Function Initialization.

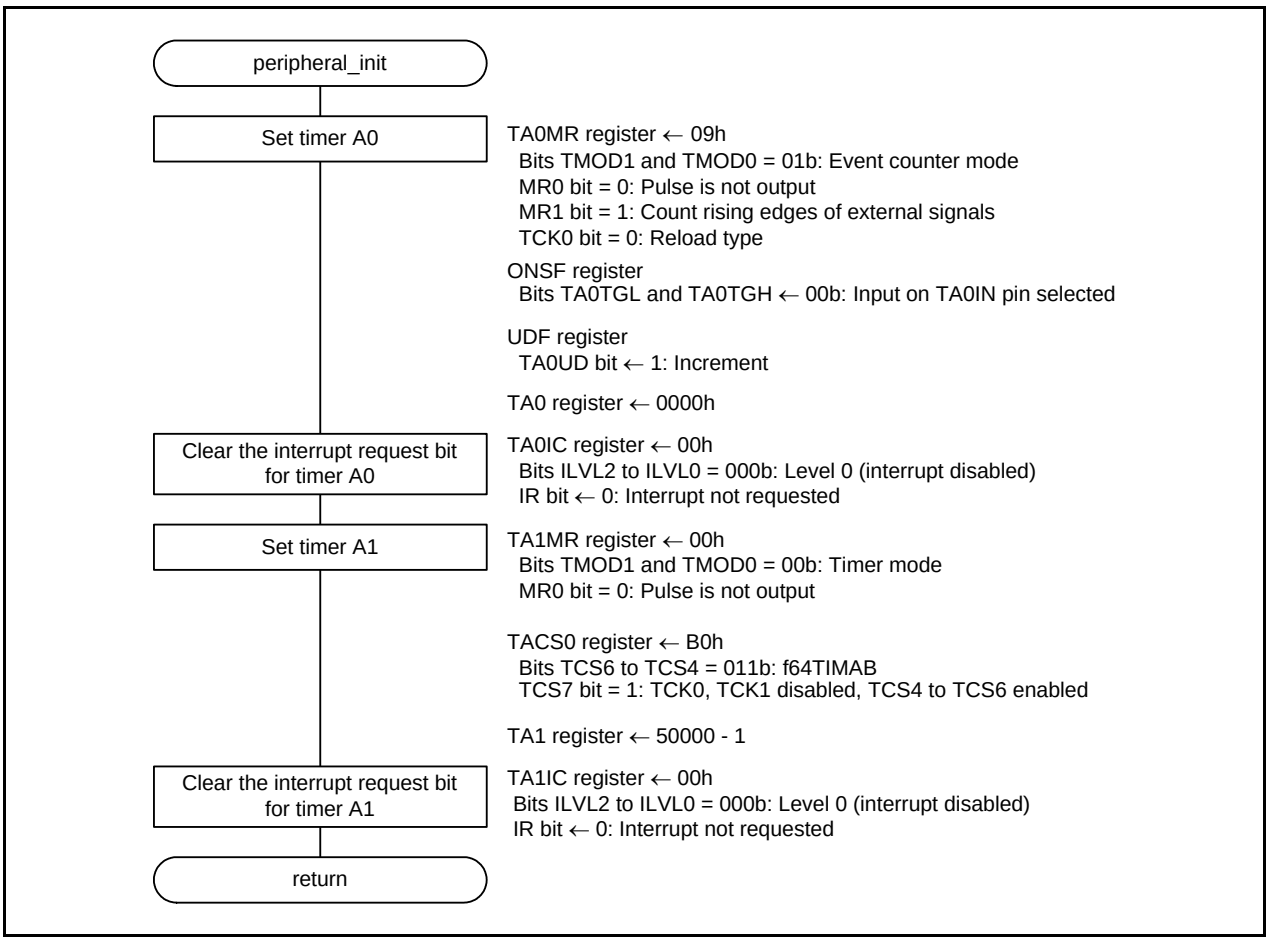

Figure 4.3 Peripheral Function Initialization

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

M16C/63 Group User's Manual: Hardware Rev. 2.00
M16C/64A Group User's Manual: Hardware Rev. 2.00
M16C/64C Group User's Manual: Hardware Rev. 1.00
M16C/65 Group User's Manual: Hardware Rev. 2.00
M16C/65C Group User's Manual: Hardware Rev. 1.00
M16C/6C Group User's Manual: Hardware Rev. 2.00
M16C/5L Group, M16C/56 Group User's Manual: Hardware Rev. 1.10
M16C/5LD Group, M16C/56D Group User's Manual: Hardware Rev. 1.10
M16C/5M Group, M16C/57 Group User's Manual: Hardware Rev. 1.10
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
M16C Series/R8C Series C Compiler Package V.5.45
C Compiler User's Manual Rev. 2.00
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Revision History	M16C/63, 64A, 64C, 65, 65C, 6C, 5LD, 56D, 5L, 56, 5M, and 57 Groups Determining Commercial Power Frequency

Rev.	Date	Description	
		Page	Summary
1.00	Nov. 30, 2011	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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