RA4M1 Group

Notes on RA4M1 Group High-Temperature Operation

Introduction

Renesas provides RA4M1 Group microcontrollers that operate in high-temperature environments. These products are guaranteed to operate within the stipulated range. However, the reliability of a semiconductor device is influenced greatly by the environment in which it is used. That is, even for products with the same quality level, if one is operated in a more severe environment, its reliability will be reduced. Conversely, if one is used in a less severe environment, its reliability will increase. For example, a device used under extremely severe conditions, such as those used for lifetime testing, may exhibit wear-out failures, even if the environment is within the maximum ratings.

This application note presents notes on operating environments under which RA4M1 Group microcontrollers are used in high-temperature applications.

Target Device

RA4M1 Group

Contents

1. Relationship between Actual Usage Environments for RA4M1 Group Microcontrollers and Reliability

1.1 Approaches to microcontroller reliability

We strongly recommend that customers follow the items described in this document to assure device reliability when using RA4M1 Group microcontrollers.

Semiconductor device reliability is indicated by the failure rate curve (bathtub curve). This curve is divided into three regions:

- The early failure region, in which failures occur at a relatively early time after device use (operation) is first started.
- The random failure period, during which, after the early failure period, failures occur randomly across the relatively long period during which the device is used,
- The wear-out failure period (end of service life), during which failures increase with the elapsing of the time that is inherent life of the device. (See the Reliability Handbook, Revision 2.50 (R51ZZ0001EJ0250) for further details on the bathtub curve.)

Of these regions, it is the wear-out failure region that is most strongly influenced by the thermal environment in which the semiconductor device is used. The concept of derating is critical to assuring that RA4M1 Group microcontrollers do not reach the wear-out failure region.

1.2 Derating

Derating is defined under JIS Z 8115 as the systematic reduction of load for the sake of improved reliability.

Derating is commonly applied to product groups, such as discreet components and power ICs, where concern is required regarding the junction temperature due to the relationship between the generated power, ambient temperature, and heat sink characteristics. Concern is required even if, in addition to the usage conditions having wide ranges, operation is within those usage conditions (for example, voltage) from the standpoint of the problem of heat generation, and, furthermore, adjustment is required between usage conditions such as ambient temperature, junction temperature, current, and power, which have mutual relationships.

See section 5.2.3, Derating, in the Reliability Handbook, Revision 2.50 (R51ZZ0001EJ0250) for further details on derating.

This application note presents temperature profiles expected for representative high-temperature applications and derating examples that RA4M1 Group microcontrollers can support.

2. Thermal Characteristics Term Definitions

- Ta (ambient temperature): Ta is the temperature at a place that is not affected by heat sources and is based on measurement methods stipulated by JEDEC (figure 2-1 and figure 2-2). See the EIA/JEDEC Standard 51-2 for details. Also see the product and package information that Renesas provides on its website.

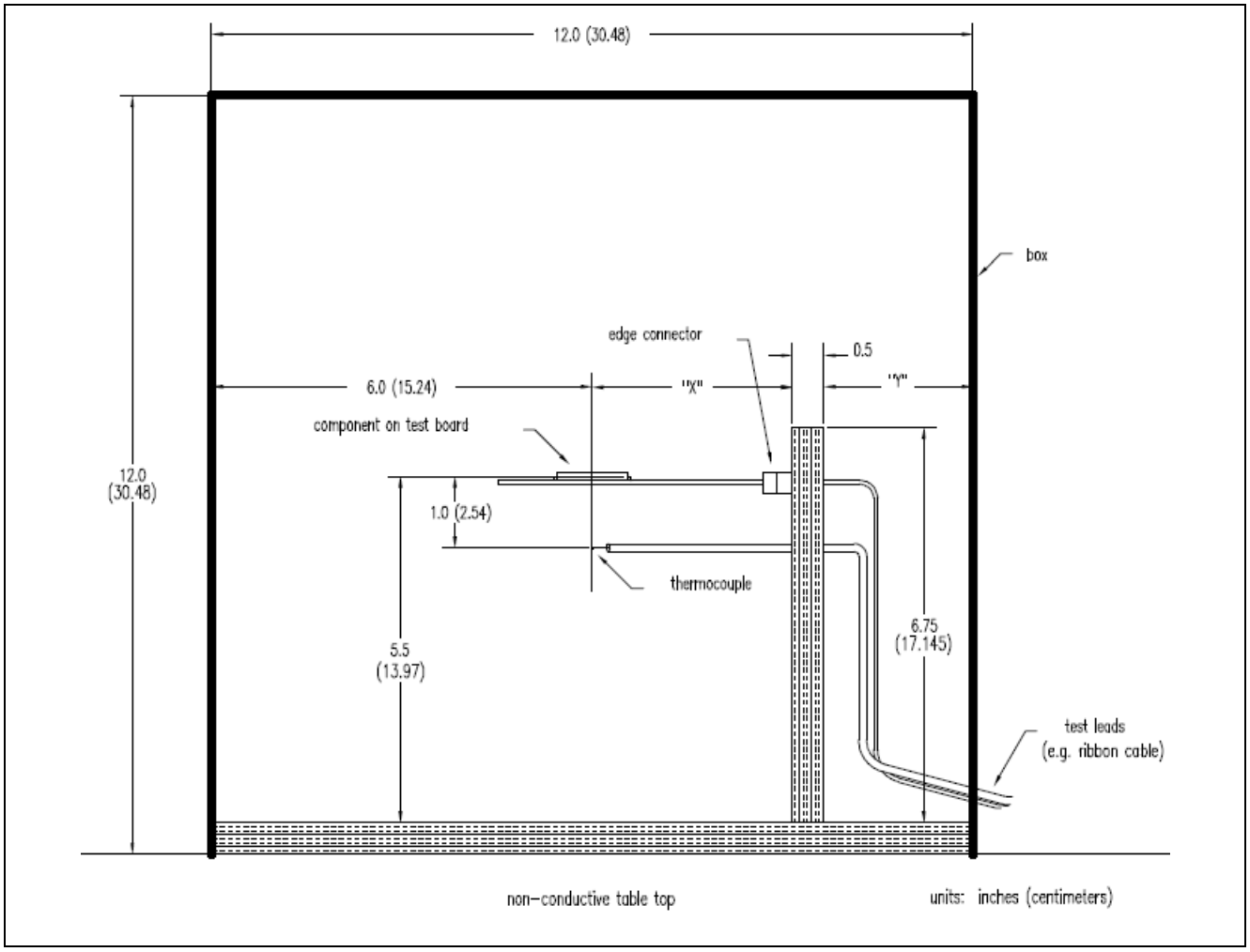

Figure 2-1 Ta measurement position (from the EIA/JEDEC 51-2 Standard)

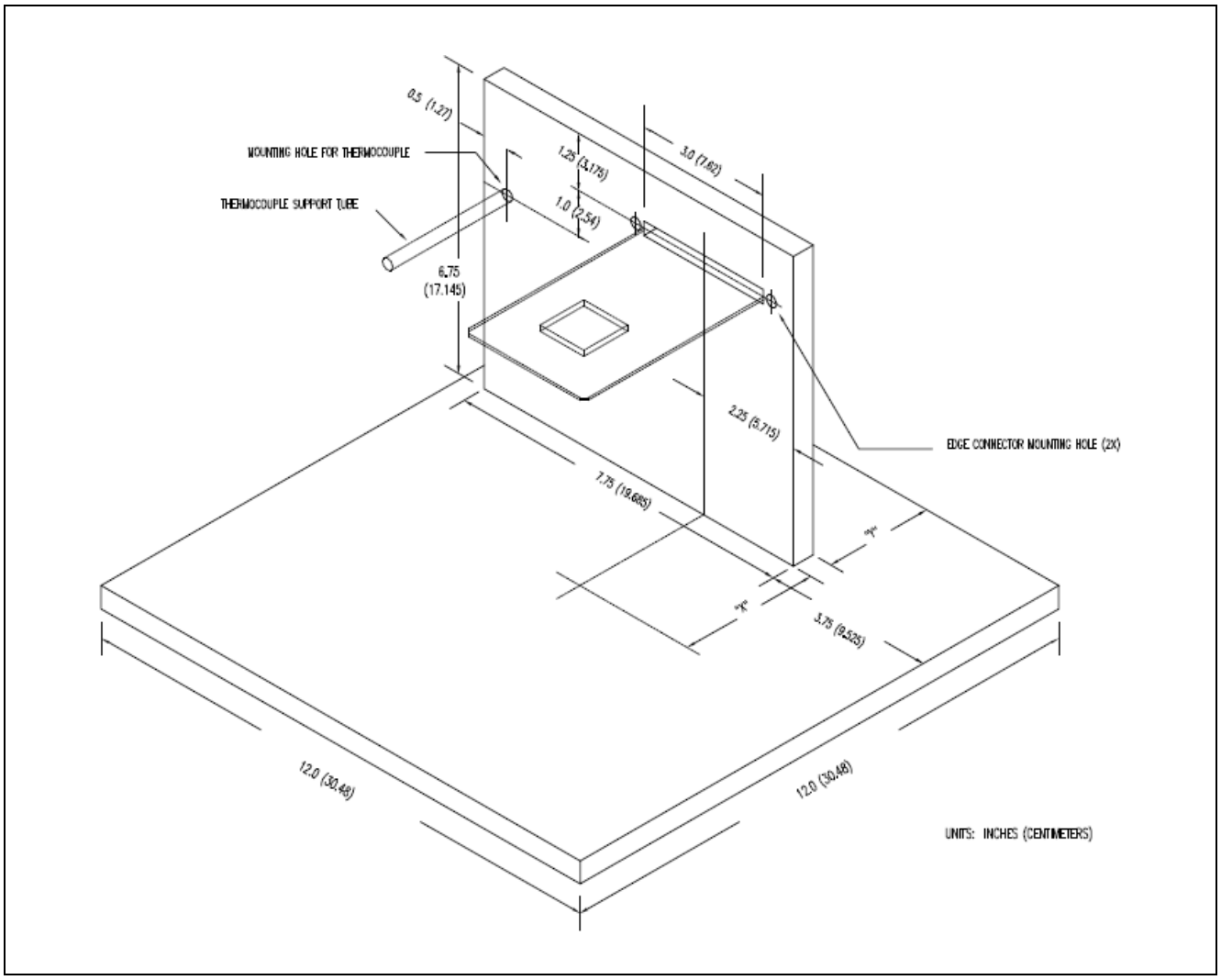

Figure 2-2 Ta measurement position - bird's Eye View (no chassis) (from the EIA/JEDEC 51-2 Standard)

The mounting board is a 76.2 × 114.3 × 1.6 mm 4-layer board. See the EIA/JEDEC Standard 51-7 for details.

3. Thermal Characteristics

3.1 RA4M1 Group thermal resistances

RA4M1 Group supports Tjmax as 112℃. Enclosure environment and printed wiring board (PWB) environment are as described in

Table 3.1.

For additional details, refer to the following URL:

https://www.renesas.com/us/en/support/technical-resources/packaging/characteristic/heat-dissipation.html

Table 3.1 RA4M1 Group thermal resistances

Package	Enclosure Environment	PWB Environment	θja[℃/W]
100-pin LQFP PLQP0100KB-B	304.8*304.8*304.8mm (JESD51-2 compliant)	4 layers (JESD 51-7 compliant)	45.2
64-pin LQFP PLQP0064KB-C	304.8*304.8*304.8mm (JESD51-2 compliant)	4 layers (JESD 51-7 compliant)	44.6
48-pin LQFP PLQP0048KB-B	304.8*304.8*304.8mm (JESD51-2 compliant)	4 layers (JESD 51-7 compliant)	52.2
64-pin QFN PWQN0064LA-A	304.8*304.8*304.8mm (JESD51-2 compliant)	4 layers (JESD 51-7 compliant)	26.1
48-pin QFN PWQN0048KB-A	304.8*304.8*304.8mm (JESD51-2 compliant)	4 layers (JESD 51-7 compliant)	28.0
40-pin QFN PWQN0040KC-A	304.8*304.8*304.8mm (JESD51-2 compliant)	4 layers (JESD 51-7 compliant)	30.7

4. Derating Examples for Representative High-Temperature Applications

Table 4.1 lists temperature profiles expected for representative high-temperature applications and recommended temperature profiles for derating.

The corresponding packages are the LQFP 100, 64, 48-pin packages, HWQFN 64,48,40-pin packages. And the package codes are PLQP0100KB-A, PLQP0064KB-C, PLQP0048KB-B, PWQN0064LA-A, PWQN0048KB-A, and PWQN0040KC-A/. Table 4.2 lists the specific corresponding products.

The customer should select the example that is the most similar to the intended application. Contact your Renesas representative if none of these examples are applicable. Except for No.5, derating assumes a 10-year life time.

The recommended temperature profile is calculated based on the total power dissipation and the thermal resistance (Θja) determined from the thermal characteristics definitions assumed for the environment described in section 2 and section 3. For example, if Tj=112℃ in No.1, then the total power dissipation for LQFP 48-pin devices will be around 130 mW or lower, users should use these products while maintaining either the thermal resistance assumed in section 3, section 4 or environment with an even lower thermal resistance.

Table 4.1 Representative High-Temperature Applications

No.	Main Applications	Assumed Temperature Profile	Recommended Temperature Profile for Derating
1	Cooking equipment (kitchen stoves, IH heaters)	An operating time of 3 hours/day in a high-temperature environment. Standby or stopped at other times.	Tj ≤ 112°C for 3 hours/day. At other times, standby or stopped at Tj ≤ 97°C
2	Appliance motors, power tools	Used for 3 hours/day in a high-temperature environment. Used for 3 hours/day in a non-high-temperature environment. Standby or stopped at other times.	102°C < Tj ≤ 112°C for 3 hours/day. Tj ≤ 102°C for 3 hours/day. At other times, standby or stopped at Tj ≤ 97°C
3	EV chargers	Used for 8 hours/day in a high-temperature environment. Standby or stopped at other times.	102°C < Tj ≤ 112°C for 4 hours/day. Tj ≤ 102°C for 4 hours/day. At other times, standby or stopped at Tj ≤ 92°C
4	Smart meters, power converters, and equipment that may be installed outdoors (24-hour operation)	Used for 4 hours/day in a high-temperature environment. Used for 4 hours/day in a non-high-temperature environment. Also operating at other times.	102°C < Tj ≤ 112°C for 4 hours/day. ≤ Tj ≤ 102°C for 4 hours/day. At other times, operating at Tj ≤ 87°C
5	PC and server power supplies (24-hour operation)	Used continuously for 5 years in an environment that includes high-temperature periods.	102°C < Tj ≤ 112°C 15,000 hours Tj ≤ 102°C 30,000 hours
6	Industrial motors (24-hour operation: example 1)	Used continuously in a high-temperature environment.	89°C < Tj ≤ 99°C 80% Tj ≤ 89°C 20%
7	Industrial motors (24-hour operation: example 2)	Used continuously in an environment that includes extreme high-temperature periods.	97°C < Tj ≤ 112°C 5% 92°C < Tj ≤ 97°C 75% Tj ≤ 92°C 20%

Note: The ambient temperature (Ta) should be between -40°C and 105°C.

Table 4.2 Corresponding Products

Product	Package	Code flash	Data flash	SRAM
R7FA4M1AB3CFP	PLQP0100KB-B	256KB	8KB	32KB
R7FA4M1AB3CFM	PLQP0064KB-C			
R7FA4M1AB3CNB	PWQN0064LA-A			
R7FA4M1AB3CFL	PLQP0048KB-B			
R7FA4M1AB3CNE	PWQN0048KB-A			
R7FA4M1AB3CNF	PWQN0040KC-A			

5. Reference Documents

Semiconductor Reliability Handbook Rev. 2.50 (R51ZZ0001EJ0250), January 2017

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jul.10.23	All	First edition issued.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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