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April 1<sup>st</sup>, 2010  
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## M16C/65 Group

### Operation of Timer A (timer mode)

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#### 1. Abstract

In timer mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

#### 2. Introduction

This application note is applied to the M16C/65 group microcomputers.

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

### 3. Setting example

Table 1. Setting example

Item	Description	
Count source	<input type="radio"/>	Internal count source (f1TIMAB/f2TIMAB/f8TIMAB/f32TIMAB/f64TIMAB/foco-F/foco-s/fc32)
Pulse output function	<input type="radio"/>	No pulse output
	<input type="checkbox"/>	Pulses output
Gate function	<input type="radio"/>	No gate function
	<input type="checkbox"/>	Performs count only for the period in which the TAIIN pin is at "L" level
	<input type="checkbox"/>	Performs count only for the period in which the TAIIN pin is at "H" level
Output polar control	<input type="radio"/>	Output waveform "H" active
	<input type="checkbox"/>	Output waveform "L" active (output reversed)

Note: i = 0 ~ 4

### 4. Operation

- (1) Setting the count start flag to "1" causes the counter to perform a down count on the count source.
- (2) If an underflow occurs, the content of the reload register is reloaded to the counter, and the count continues. At this time, the timer Ai interrupt request bit goes to "1".
- (3) Setting the count start flag to "0" causes the counter to stop and to hold its value.

Figure 1 shows the operation timing.

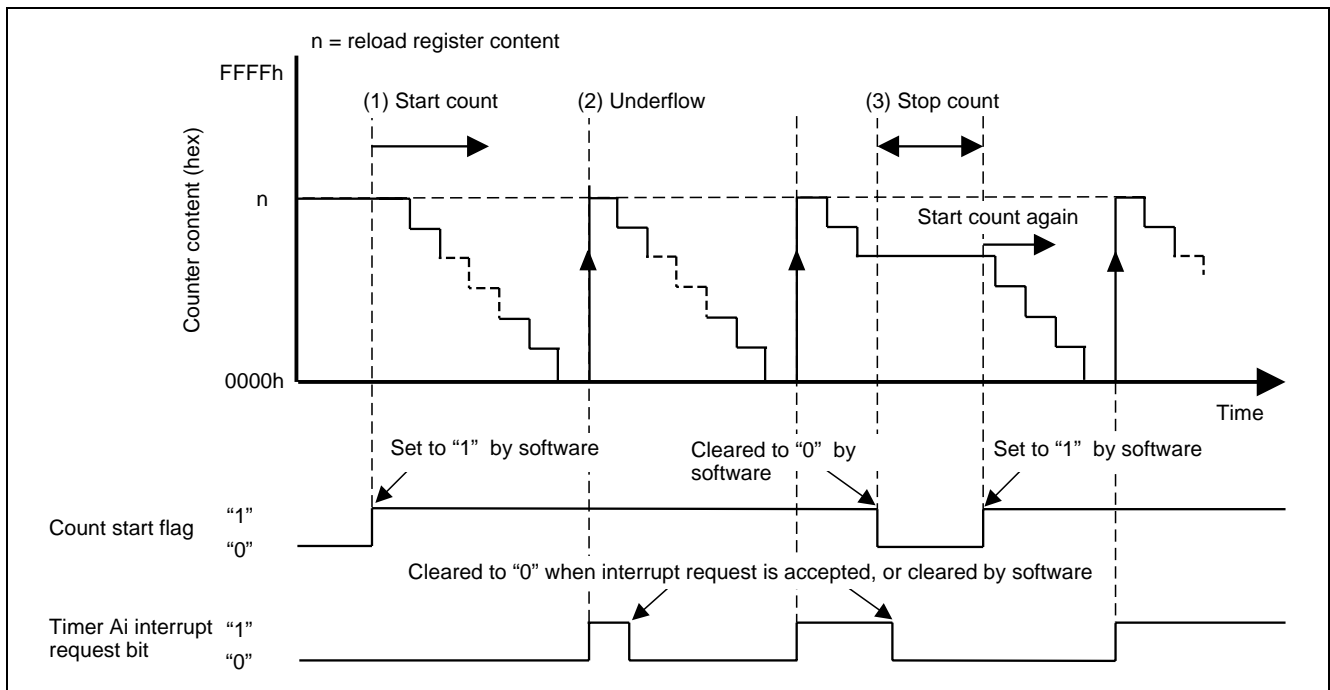


Figure 1. Operation timing of timer mode

## 5. Set-up procedure

Table 2 shows Timer A count source, Figure 2 shows block diagram of Timer A count source in timer mode.

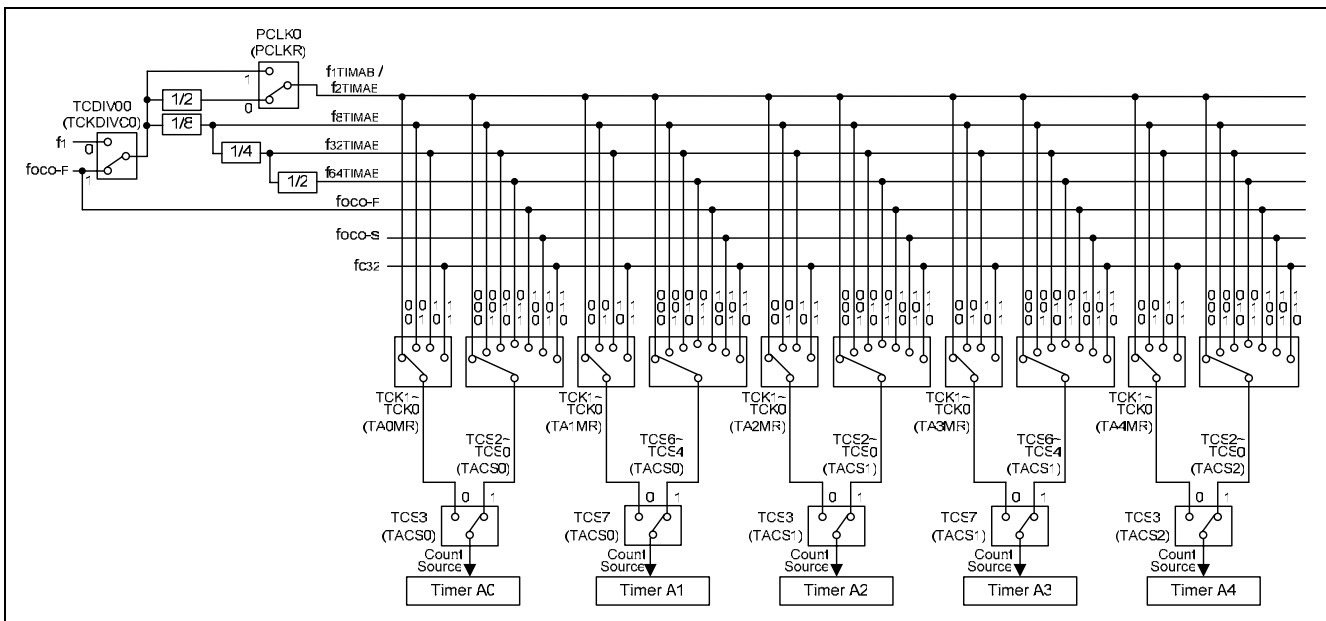
**Table 2. Count Source Selection of Timer A**

TCDIV00 register (Note 1)	TACSj register (Note 2)				TAiMR register		Count source	Count source period
	TCS3/ TCS7	TCS2/ TCS6	TCS1/ TCS5	TCS0/ TCS4	TCK1	TCK0		
0	0	-	-	-	0	0	f1TIMAB/ f2TIMAB (Note 3)	f(XiN):20MHz f(XciN):32.768kHz f(oco-F): about 20MHz f(oco-s): about 125kHz
0	0	-	-	-	0	1	f8TIMAB	50ns/100ns
0	0	-	-	-	1	0	f32TIMAB	400ns
0	0	-	-	-	1	1	fc32	1600ns
0	1	0	0	0	-	-	f1TIMAB/ f2TIMAB (Note 3)	976.56µs
0	1	0	0	1	-	-	f8TIMAB	50ns/100ns
0	1	0	1	0	-	-	f32TIMAB	400ns
0	1	0	1	1	-	-	f64TIMAB	1600ns
0	1	1	0	0	-	-	foco-F	3200ns
0	1	1	0	1	-	-	foco-s	about 50ns
0	1	1	1	0	-	-	fc32	about 8µs
0	1	1	1	0	-	-	fc32	976.56µs
1	1	0	0	0	-	-	f1TIMAB/ f2TIMAB (Note 3)	about 50ns/100ns
1	1	0	0	1	-	-	f8TIMAB	about 400ns
1	1	0	1	0	-	-	f32TIMAB	about 1600ns
1	1	0	1	1	-	-	f64TIMAB	about 3200ns

Note 1: TCDIV00 bit is clock select prior to timer AB division bit. Set the TCDIV00 bit before setting other registers associated with timer A. After changing the TCDIV00 bit, set other registers associated with timer A again.

Note 2: TCS3~TCS0 bits of TACS0 register correspond to Timer A0 count source selection, TCS7~TCS4 bits of TACS0 register correspond to Timer A1 count source selection, TCS3~TCS0 bits of TACS1 register correspond to Timer A2 count source selection, TCS7~TCS4 bits of TACS1 register correspond to Timer A3 count source selection, and TCS3~TCS0 bits of TACS2 register correspond to Timer A4 count source selection.

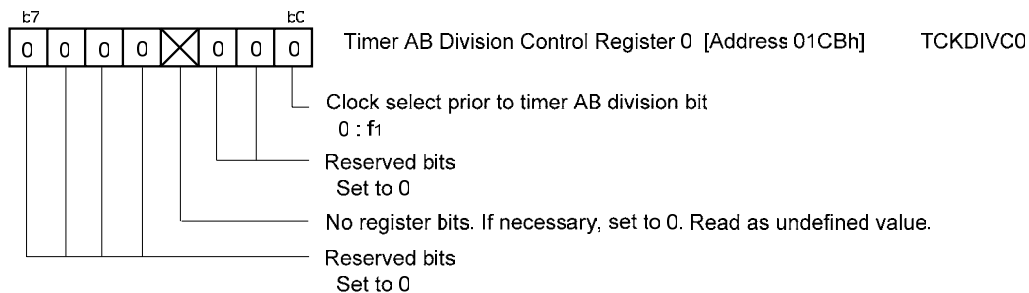
Note 3: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f1TIMAB. When the PCLK0 bit is "0", the selected clock source is f2TIMAB.



**Figure 2. Count source of Timer A**

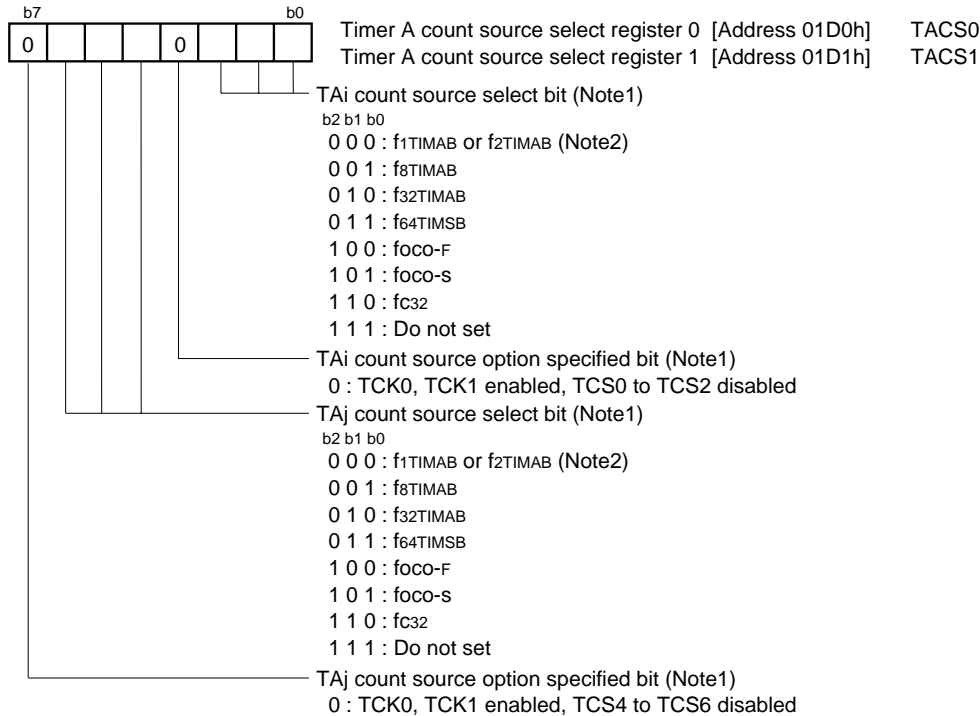
### Selecting a clock used prior to timer AB frequency dividing

(Set the TCDIV00 bit before setting other registers associated with timer A. After changing the TCDIV00 bit, set other registers associated with timer A again.)



### Selecting timer count source

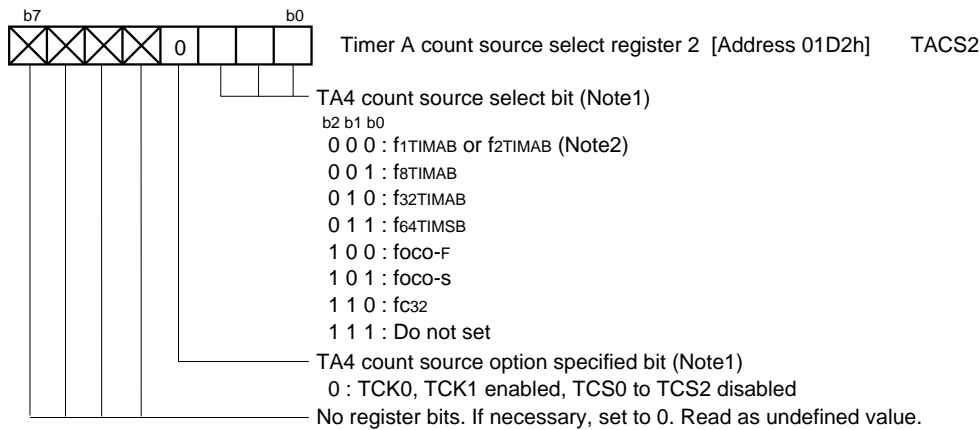
TACS0 register can select Timer A0 and Timer A1 count source, TACS1 can select Timer A2 and Timer A3 count source, and TACS2 can select Timer A4 count source.



TACS0 register: i = 0, j = 1, TACS1 register: i = 2, j = 3

Note 1: About the count source period, please refer to Table 2.

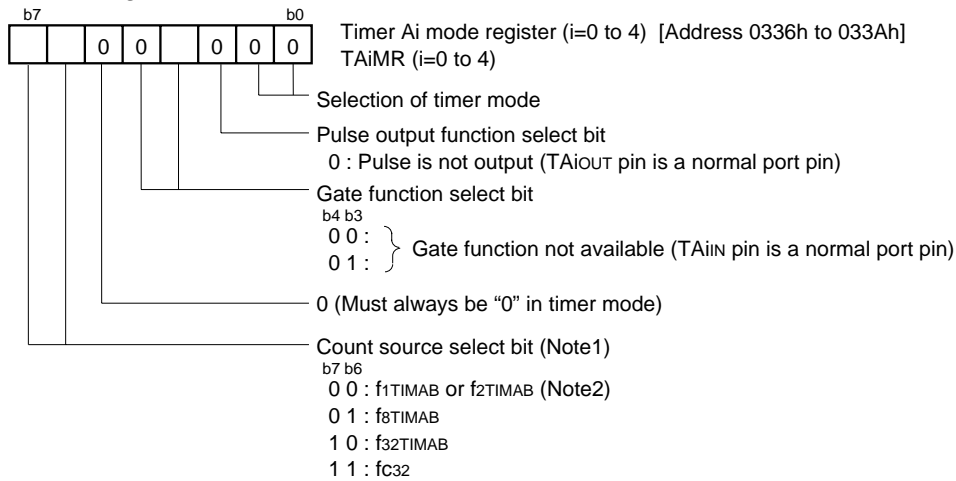
Note 2: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f1<sub>TIMAB</sub>. When the PCLK0 bit is "0", the selected clock source is f2<sub>TIMAB</sub>.



Note 1: About the count source period, please refer to Table 2.

Note 2: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f1<sub>TIMAB</sub>. When the PCLK0 bit is "0", the selected clock source is f2<sub>TIMAB</sub>.

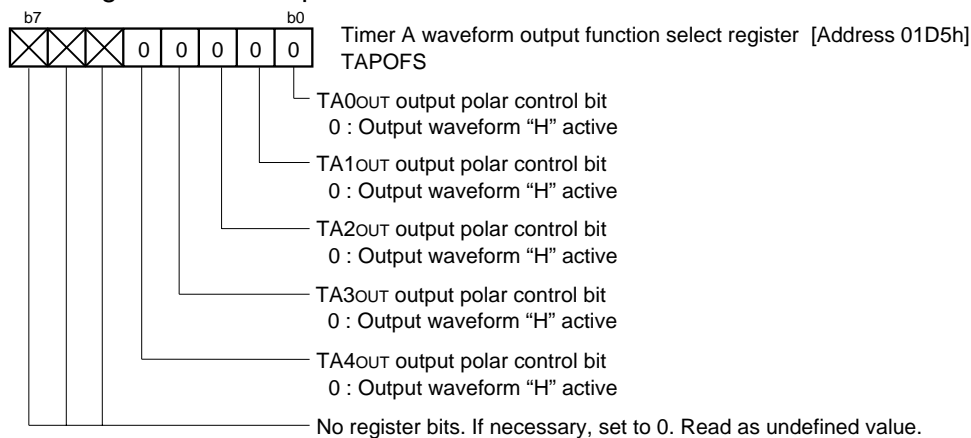
Selecting timer mode and functions



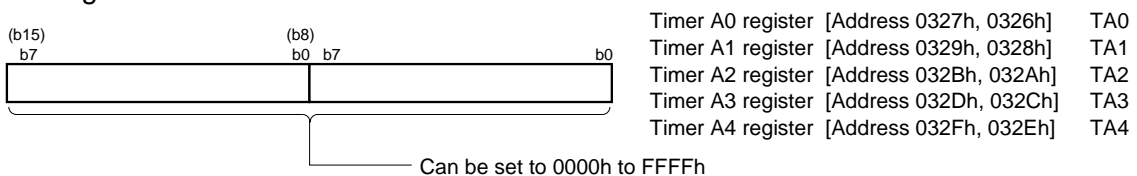
Note 1: Valid when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0, TCK1 enabled). About the count source period, please refer to Table 2.

Note 2: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f1TIMAB. When the PCLK0 bit is "0", the selected clock source is f2TIMAB.

Selecting waveform output function



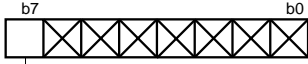
Setting counter value





Setting clock prescaler reset flag

(This function is effective when fc32 is selected as the count source. Reset the prescaler for generating fc32 by dividing the X<sub>CIN</sub> by 32.)



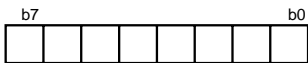
Count prescaler reset flag [Address 0015h]  
CPSRF

Clock prescaler reset flag

0 : No effect

1 : Prescale is reset (When read, the value is "0")

Setting count start flag



Count start flag [Address 0320h]  
TABSR

Timer A0 count start flag

Timer A1 count start flag

Timer A2 count start flag

Timer A3 count start flag

Timer A4 count start flag

Start count

## 6. Reference

### Hardware manual

M16C/65 Group Hardware Manual

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**Revision**

Rev.	Issue date	Revised	
		Page	Point
1.00	2009.09	-	First edition issued

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