## Contents



## List of Figures

## List of Tables

# 1. Introduction

This layout guide provides guidelines for placement and routing of the IDT P9145 PMIC, P9180/A PMIC, P91E0/A PMIC for industrial applications, P9147 DPU, and P9148/A DPUs. The sample layouts for printed circuit boards (PCB) provided below should be followed as closely as possible to ensure the highest level of device performance.

The PMIC and DPUs are manufactured in several different packages. The package options for each device are shown in Table 1.

**Table 1. PMICs and DPUs Package Types**

| | | NAG100 | NQG100 | NHG100 | NRG12 |
|---|---|---|---|---|---|
| PMIC | P9145 | ✓ | ✓ | | |
| | P9180 | | ✓ | ✓ | |
| | P9180A | | ✓ | ✓ | |
| | P91E0 | | | ✓ | |
| | P91E0A | | | ✓ | |
| DPU | P9147 | | | | ✓ |
| | P9148 | | | | ✓ |
| | P9148A | | | | ✓ |

The name and the dimensions of each package are given in Table 2. For detailed package information, such as footprint, package dimensions, tape and reel information, refer to the IDT web page for the package type given in the table:

**Table 2. Package Type Information**

| Package | Dimensions (mm) | Link |
|---|---|---|
| **NAG100 (HLA)** | 9.0 × 9.0 × 0.9 | http://www.idt.com/package/NAG100 |
| **NQG100 (VFQFPN)** | 8.0 × 8.0 × 0.77 | http://www.idt.com/package/NQG100 |
| **NHG100 (VFQFPN)** | 9.0 × 9.0 × 0.85 | http://www.idt.com/package/NHG100 |
| **NRG12 (DFN12)** | 4.0 × 3.0 × 0.9 | http://www.idt.com/package/NRG12 |

For new PMICs, the NAG (9 × 9 mm HLA) has been replaced by the NHG (9 × 9 mm VFQFPN) package option.

The NHG (9 × 9 mm VFQFPN) package solution allows Type 3 PCB design, keeping the same 100 pins available to the application, while adding only 1mm to the dimensions of the package. The package is offered together with Intel's Type 3 option for the system-on-a-chip (SoC) for low cost PCB designs where board size requirements allow a slightly larger area.

The NQG (8 × 8 mm VFQFPN) offers the advantage of high density routing and reduced PCB area. This package solution requires an HDI (Type 4) PCB (which might also be required for an SoC).

The NQG package will follow the Type 4 requirements:

- µVIAs (6 mil, laser microvias) to connect the inner pads
- Plugged vias in order to have them "inPad"
- Blind vias in order to not disturb the bottom copper fanning out for thermal dissipation

**Figure 1. PMIC Packages, Bottom View**

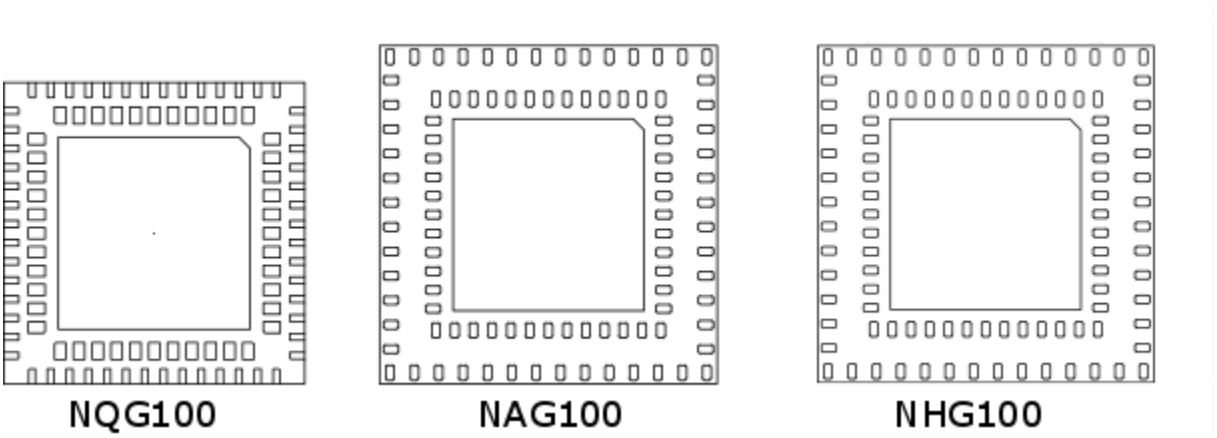
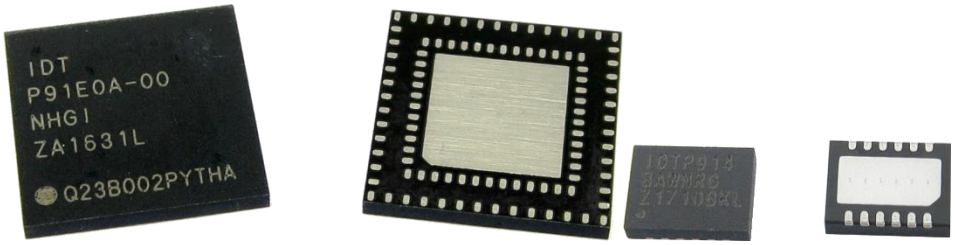



**Figure 2. Photos of P91E0A NHG100 and P9148A NRG12 Packages**




## 2. PCB Stack-up and ICs Placement

Modern devices are built with different types of PCBs. The classification presented in Table 3 divides the PCBs into four types, according to their complexity.

**Table 3. Board Types**

| Board Type | Description |
|---|---|
| Type 1 | Single-sided PCB |
| Type 2 | Double-sided PCB |
| Type 3 | Multilayer without blind or buried vias |
| Type 4 | Multilayer with blind and/or buried vias; high density interconnects (HDI) |

Typically, the PMIC and the DPUs are used in systems that have an 8-layer PCB that is either type 3 (lower cost) or type 4.

Ideally these ICs should be placed as close as possible to their load; i.e., the SoC and memory. However, this is not always possible. The PMIC and the DPUs generate heat, so care should be taken when placing them close to heat sensitive parts of the system. Although the design of the PMIC and DPU allows cooling using only the PCB, it is beneficial to have some airflow around the PMIC and DPUs.

Figure 3 and Figure 4 give examples of the location of IDT's PMIC and DPUs. Figure 3 shows the case where the DPUs are placed closer to the PMIC. This is the case when powering primarily the SoC and DDR. Figure 4 presents another case where the DPUs are placed far away from the PMIC, but closer to their load. The PMIC and DPUs communicate via a high-speed 2-wire digital bus, allowing the distance between them to be up to 4 in (10cm). Such distributed placement makes the high current routing easier, has fewer EMI problems, and provides better heat distribution.

**Figure 3. Example 1 of Placement of PMIC and DPUs**

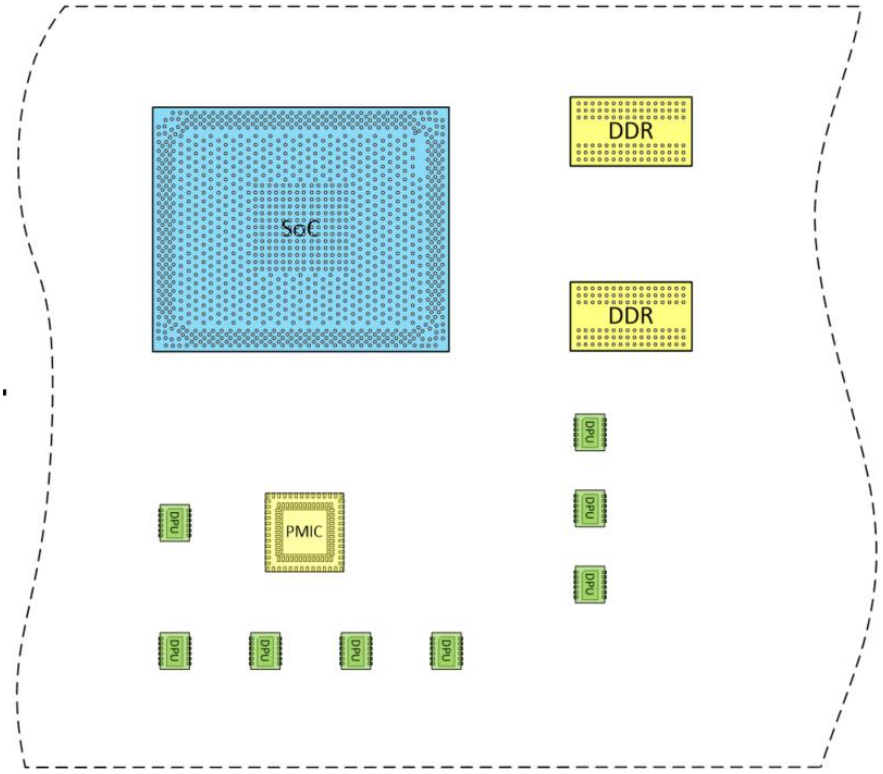
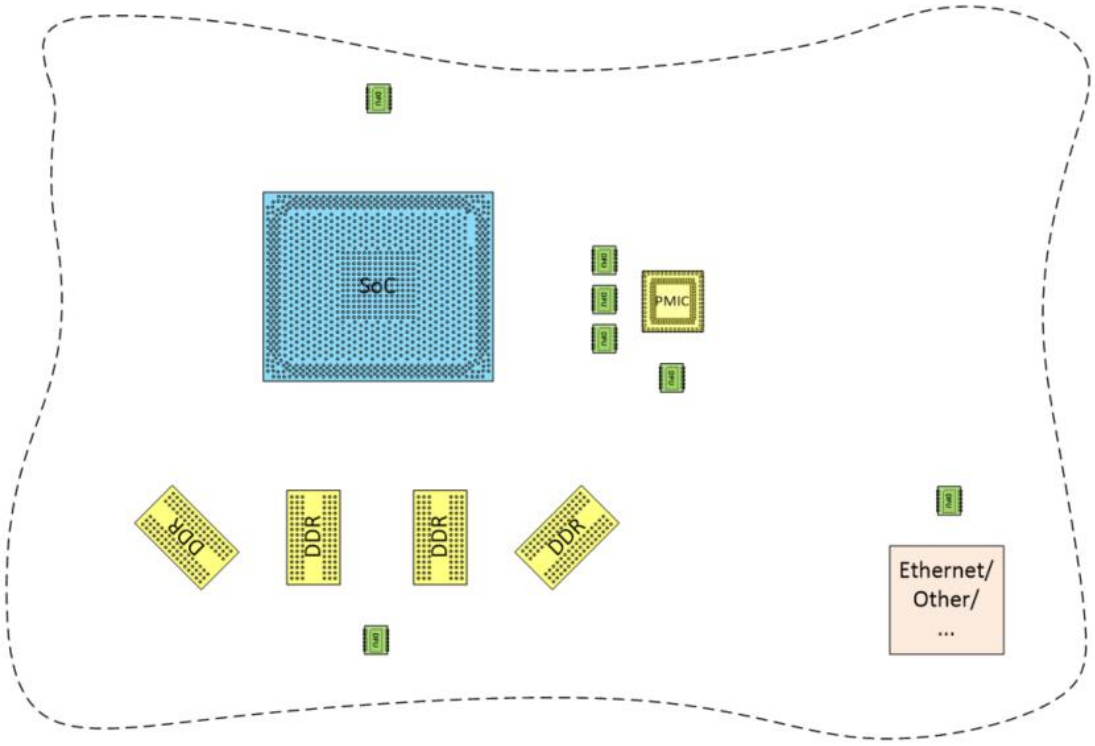


**Figure 4. Example 2 of Placement of PMIC and DPUs**

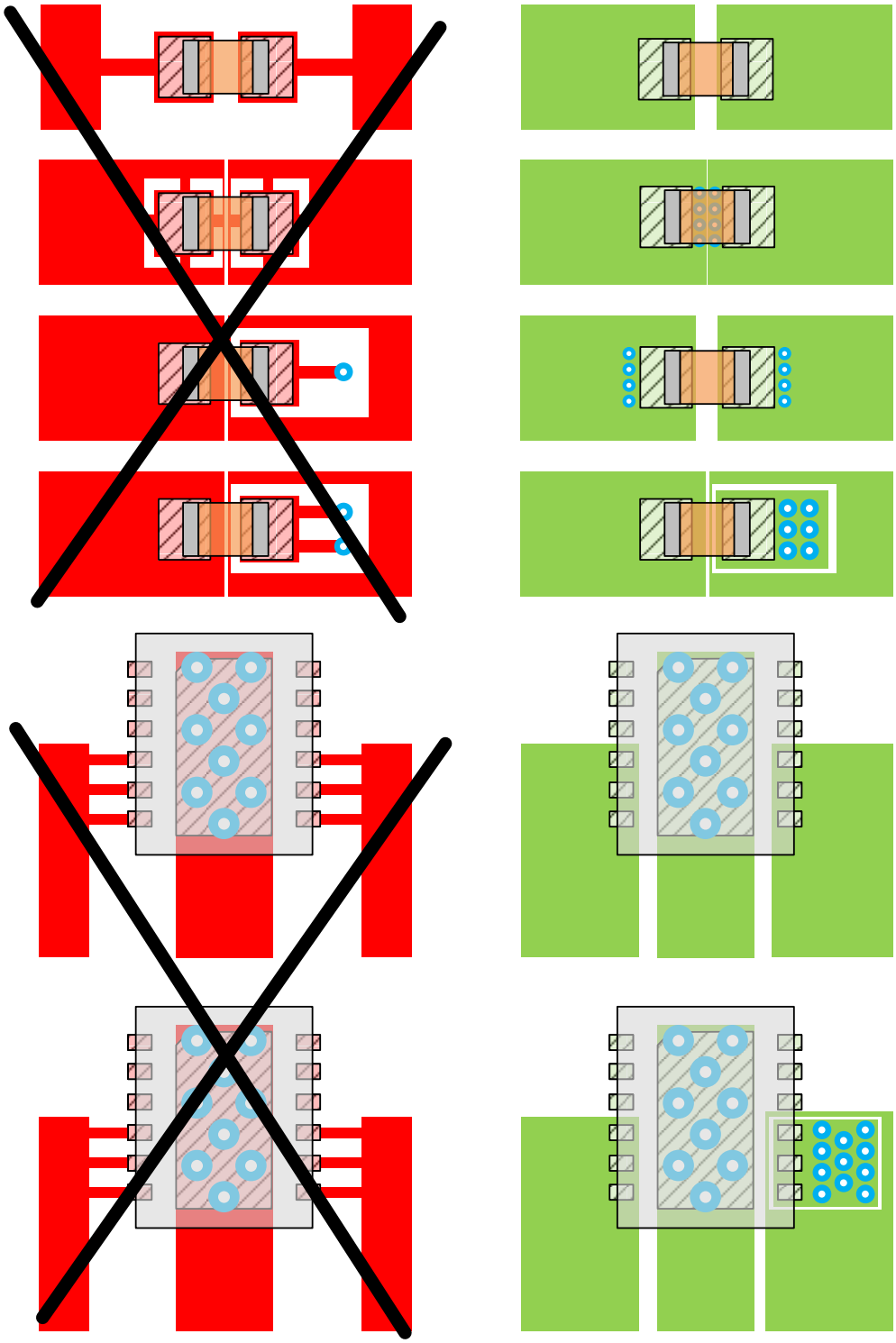


# 3. PCB Layout Design

Use the following list as starting guidelines for the layout. Additional information is also given in the datasheets for the PMIC and DPU as well.

- Output capacitors should be chosen with a proper voltage rating to avoid capacitance degrading and thus regulator instability.
- Recommendation: Use capacitors in parallel (e.g., 2 × 47µF) instead of a single capacitor (e.g., 100µF). This configuration reduces the capacitor ESR and ESL.
- The location of the capacitors on the DCDx_VIN pins for the integrated switching regulators of the PMIC is of highest importance. The fact that the DCDx_VIN pins of the switching regulators are located on the inner row of the dual-row package requires good layout practice to ensure proper operation with minimal voltage ringing caused by high switching currents. Traces must be short to reduce parasitic inductance. Wherever power planes or traces switch layers, multiple vias in parallel must be used to reduce parasitic inductance and ESR.
- Place the input capacitors $C_{IN}$ and $C_{VSYS}$ as close as possible to the PMIC/DPU input supply pins. This minimizes trace impedance and improves performance.
- Voltage feedback and sensing lines have high impedance and could be disturbed by external noise sources. Avoid routing them close to the switching node of the converters, near/under the inductors, or other noisy traces. When separate pins are available for positive and negative voltage sensing, route these traces parallel to each other.
- Use many vias for heat spreading, especially under the PMIC and DPU. They conduct the heat from the IC to the copper planes and cool the device. Always connect the exposed pad of the PMIC and DPU. It is both the IC's GND and the heat sink.
- Do not use thermal relief for power components. Some examples of proper layout are shown on Figure 5 (see green-shaded layouts).
- Use surface-mount capacitors to avoid lead inductance.
- Fill the empty spaces of the PCB with copper – this will improve the thermal performance of the board.
- Keep the inductor and output capacitor close to each other.
- Put the power components (PMIC, DPU, inductor, filter capacitor) on the same side of the PCB. This will allow shorter connections without using vias.
- Avoid using vias for power connections. If absolutely necessary, use many vias in parallel.
- Use short and thick traces for power connections. This minimizes the inductance and resistance.
- Use a low impedance connection from the switching node to the inductor (short, but wide).
- Place the majority of output capacitors as close as possible to the load, and keep one capacitor close to the inductor.
- Input and output capacitors can be connected to internal PCB layers with 6-10 vias in parallel per pin.
- Pull-up resistors can be connected with a single via. The location of these resistors is less important.

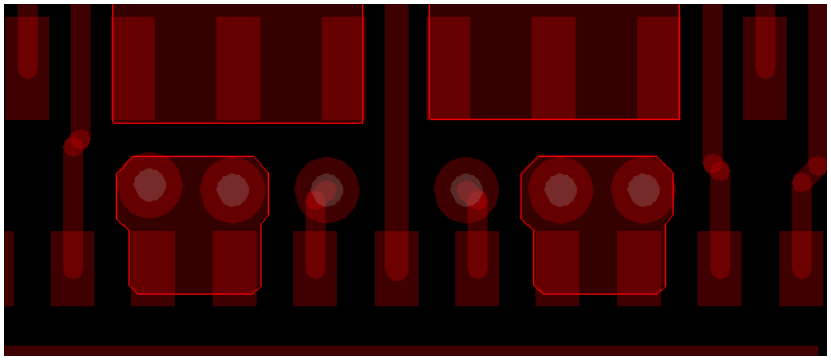
**Figure 5. Inadequate Layout (Red Shading) vs. Recommended Layout (Green Shading) for Land Patterns for Power Components**



# 4. PMIC Layout

Depending on the product (see Table 1), the P9145, P9180/A, and P91E0/A PMICs are offered with three package options: two variations of the double-row Very Fine Pitch Quad Flat Package (VFQFPN) and the Hi-Density Leadless Array (HLA) package. All of them are dual-row type packages with an exposed pad (EPAD). The HLA package is slightly larger than the NQG VFQFPN (9mm × 9mm compared to 8mm × 8mm for the VFQFPN package for P9145), but the HLA has a wider pad pitch to allow layouts on Type 3 PCBs. With the introduction of the P9180, there is also the NHG100 VFQFPN, which is pin-to-pin compatible with the HLA package. These two packages allow routing with a 4-layer, Type 3 PCB. As shown in Figure 6, there is enough space between the inner and outer row for a through-hole via which allows the placement of a 16mil (0.4mm) via to break-out signals from the inner row.

**Figure 6. Vias between Inner and Outer Rows for P9145, P9180/A, and P91E0/A in an HLA Package**



The smaller NQG100 VFQFPN package has the following requirements:

- Type 4 PCBs
- Use of via-in-pad technology
- Blind and/or buried vias.

The exposed pad of the PMIC is the power ground (PGND) of the integrated switching regulators. A solid connection with an array of at least 5 × 5 vias from the EPAD area on the top layer of the PCB to the ground plane(s) is necessary to allow the return current of the regulator to circulate back to ground.

## 4.1 NAG100 (9 × 9 mm HLA) and NHG100 (9 × 9 mm VFQFPN) Package Layout Guidelines

Figure 7 shows an example of placement of the capacitors on the DCDx_VIN pins. The P9145 datasheet recommends the use of 2 × 10µF input capacitors for the high current regulators DCD0/1/2. The input capacitors are placed on the bottom side of the PCB (the P9145, P9180/A, and P91E0/A ICs are on the top side). For example, there are two vias connecting the DCD2_VIN pins (pins B30, B31) on the top layer to the DCD2_VIN island on the bottom layer. The GND island is then connected back to the EPAD through three vias. The input capacitors are placed between the DCD2_VIN and GND islands. This configuration ensures the shortest possible trace length minimizing the DCD2_VIN-PGND loop and parasitic inductance. All other regulators should have the input capacitors placed in a similar way.

**Figure 7. Placement of the DCDx_VIN Capacitors for 9 × 9 mm VFQFPN (NHG100) and HLA (NAG100) Package (top view, bottom layer shown) – Example using DCD2_VIN**

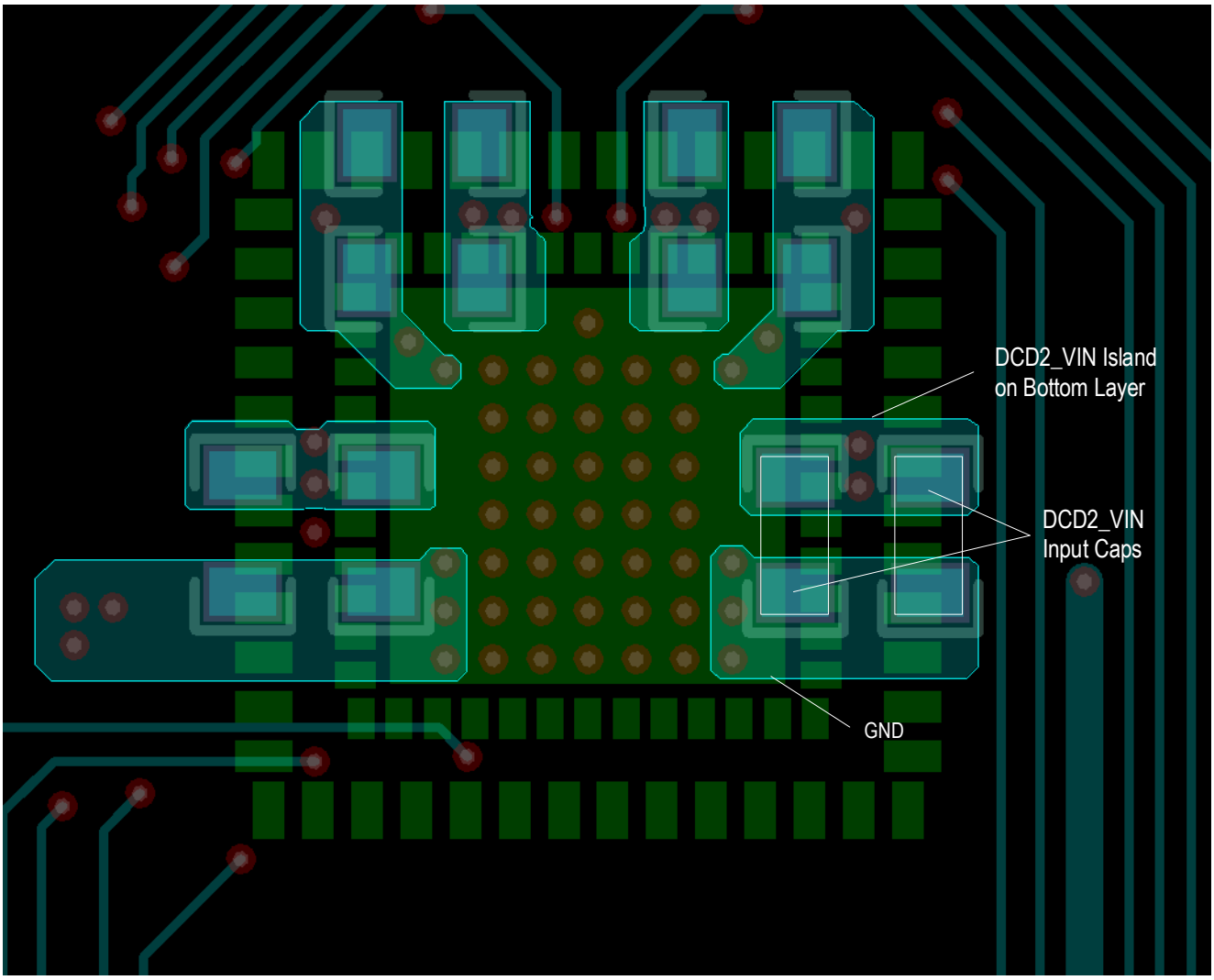
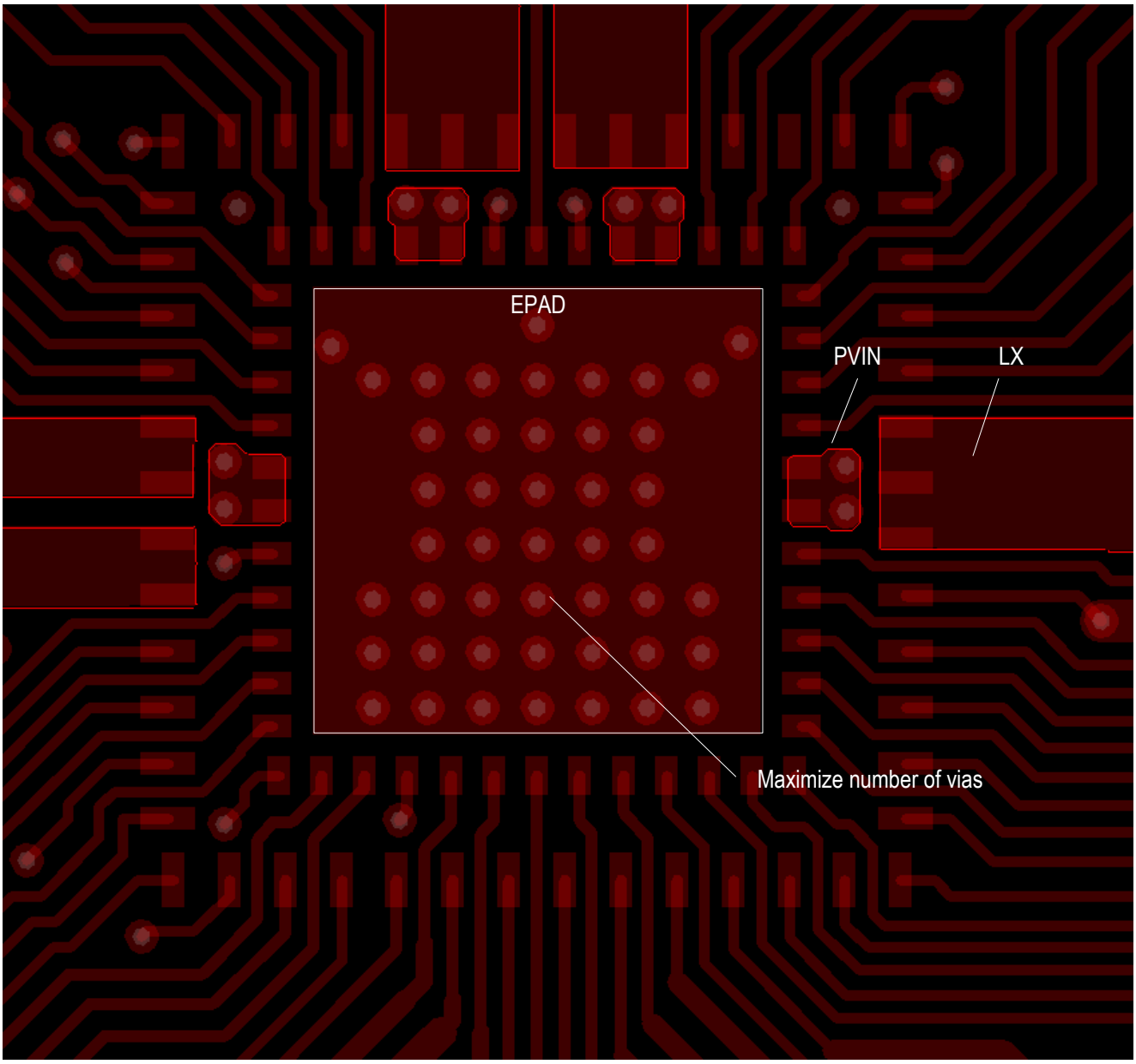


Figure 8 shows the top layer of the example P9145 layout.

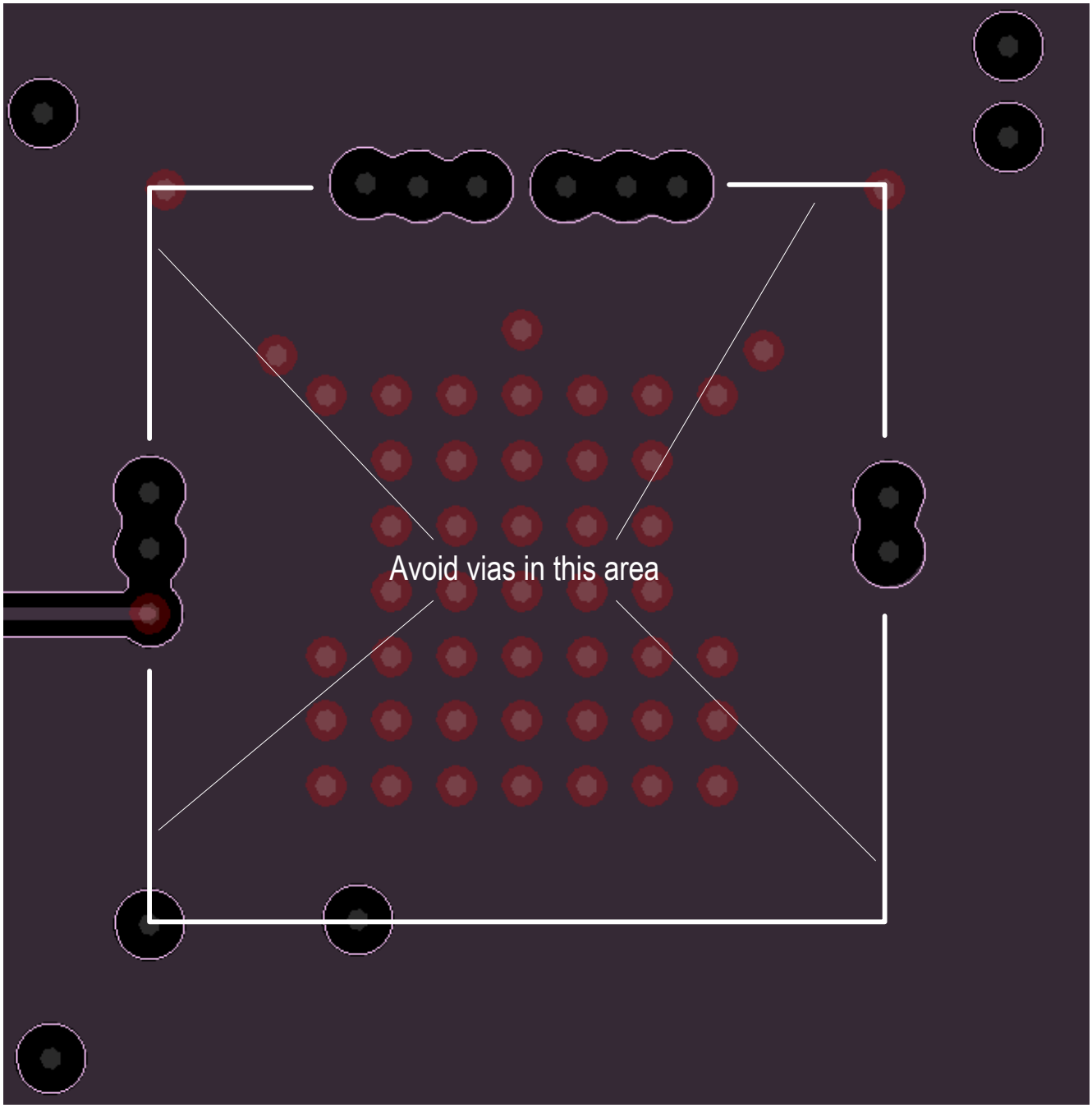
Recommendation: For proper electrical and thermal performance, use as many vias as possible to connect the top layer EPAD to the ground plane(s). An array of 5 × 5 or 6 × 6 vias, depending on design rules for minimum via diameter, can be easily accomplished and should fill the entire EPAD area.

**Figure 8. Top View of an Example Layout for 9 × 9 mm VFQFPN (NHG100) and HLA (NAG100) Package**



The ground layer of the example PCB around the PMIC is shown in Figure 9. It is important to ensure that the ground layer is not heavily perforated by vias of other nets. Those obstructions can hamper the current flow in the ground plane. This is especially true for the area around the PMIC. The EPAD is the power ground of all internal switching regulators, and proper current flow into the ground plane must be ensured.

**Figure 9. Ground Layer around the P9145, P9180/A and P91E0/A**

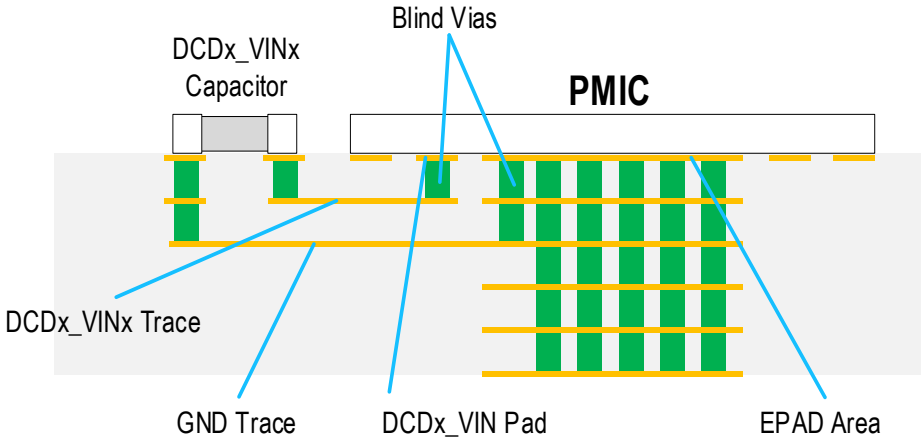


## 4.2 NQG100 (8 × 8 mm VFQFPN) Package Layout Guideline

If the P9145 or P9180/A in the NQG100 (VFQFPN) package is used, the DCDx_VIN capacitors can be placed on the top layer or bottom layer of the PCB. The EPAD should be connected through vias to the ground plane(s). Care should be taken to place the DCDx_VIN input capacitors close to the P9145 or P9180/A. Two examples of layout are presented in Figure 10 and Figure 11.

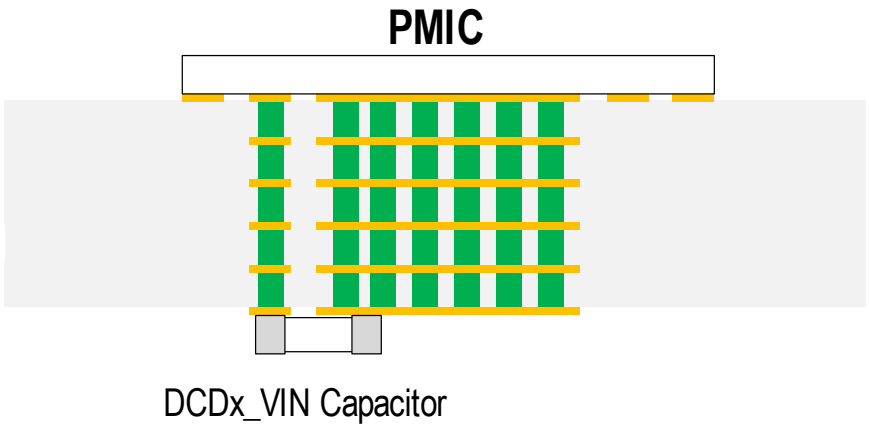
Figure 10 shows a cross section of PCB layout where blind vias are used for DCDx_VIN capacitor placement. In this case, DCDx_VIN capacitors are placed on the top layer of the PCB. A blind via in the DCDx_VIN pad connects the pad to the DCDx_VIN trace in the inner layer; then another blind via is used to connect the inner layer out to the positive terminal of the DCDx_VIN capacitor. The negative terminal of the capacitor connects to the ground (EPAD) pad in a similar way. Both the DCDx_VIN trace and GND trace should be kept short to minimize the DCDx_VIN-GND loop and parasitic inductance.

**Figure 10. DCDx_VIN Capacitor Top Layer Placement for P9145 or P9180/A in the NQG100 Package**




A cross section of another example PCB layout is shown in Figure 11. No blind vias are used for DCDx_VIN and EPAD in this case, so both DCDx_VIN and the EPAD are connected to the bottom layer through regular vias. The DCDx_VIN capacitors are placed in the bottom layer. Care should be taken to minimize the power supply traces' loop and parasitic inductance.

**Figure 11. DCDx_VIN Capacitor Bottom Layer Placement P9145 or P9180/A in the NQG100 Package**



# 5. General Recommendations Valid for all DPUs

For optimum device performance, the following guidelines should be observed. Contact IDT for Gerber files that contain the recommended board layout.

- The DIO and DIF signals transition at a controlled edge rate of 8ns (typical) with a driving impedance of 70Ω. In most applications, these lines do not need to be treated as transmissions lines, but it is recommended that trace widths for $Z_0$ be approximately 70Ω for optimum signal integrity. Since the impedance of the trace depends on several factors, it is recommended that a software tool be used for the calculation. It could be either part of the ECAD software or separate software, such as the Saturn PCB Design Toolkit.[1]
- All $C_{OUT}$ capacitors should be clustered together and placed as close to the load device as possible. The feedback voltage and ground sense lines of the host PMIC should be connected across the load capacitor bank.
- The $C_{VSYS}$ and $C_{VPG}$ decoupling capacitors should be mounted on the component side of the board, close to their respective pins. Recommendation: Do not to use vias between the decoupling capacitors and their pins and keep their PCB traces as short as possible.
- Due to the possibility of high switching currents and the high input voltage range, the $C_{PVIN}$ mounting inductance should be less than the $C_{PVIN}$ capacitor's ESL, which is approximately 1nH. This can be accomplished by placing $C_{PVIN}$ as shown in the example layouts, using only the top layer route to connect to the PVIN pins and the PGND EPAD, which will minimize inductance in the PVIN-PGND loop.
- If the PVIN plane or the ground plane is not the top layer, then vias can be used outside of the PVIN-PGND loop to connect the DPU to those planes. Since the $C_{PVIN}$ capacitor case size can easily allow a 4-via connection, this should be used. For the PGND EPAD connection, the number of vias connecting the PGND EPAD to the ground plane should be maximized for thermal consideration. It is recommended that at least 10 vias are used for this connection in typical applications.
- The package center exposed pad must be reliably soldered directly to the PCB. The center land pad on the PCB (set 1:1 with EPAD) must also be tied to the board ground plane, primarily to maximize thermal performance in the application. The ground connection is best achieved using a matrix of plated-through-hole (PTH) vias embedded in the PCB center land pad. The PTH vias perform as thermal conduits to the ground plane (thermally, a heat spreader) as well as to the solder side of the board. Recommendations for the via finished hole-size and array pitch are 0.3mm to 0.33mm (11mils to 13mils) and 1.3mm (50mils), respectively.
- The DPU's NRG12 package has an inner thermal pad, which requires blind assembly. It is recommended that a more active flux solder paste be used, such as the Alpha OM-350 solder paste from Cookson Electronics (http://www.cooksonsemi.com). Contact IDT for Gerber files that contain a recommended solder stencil design.
- The PCB design and layout can have a significant influence on the power dissipation capabilities of power management ICs. This is due to the fact that the surface mount packages used with these devices rely heavily on thermally conductive traces and planes to transfer heat away from the package. The following general guidelines will be helpful in designing a board layout for low thermal resistance:
  - PC board traces with large cross sectional areas have higher thermal conductivity. If possible, a 2oz. (70µm) copper ground plane with ample thermal vias connecting to the EPAD of the DPU is recommended.
  - Do not use solder mask or place silkscreen on the heat-dissipating traces/pads, as they increase the net thermal resistance of the mounted IC package.

[1] Product of Saturn PCB Design, Inc.

# 6. DPU Layout

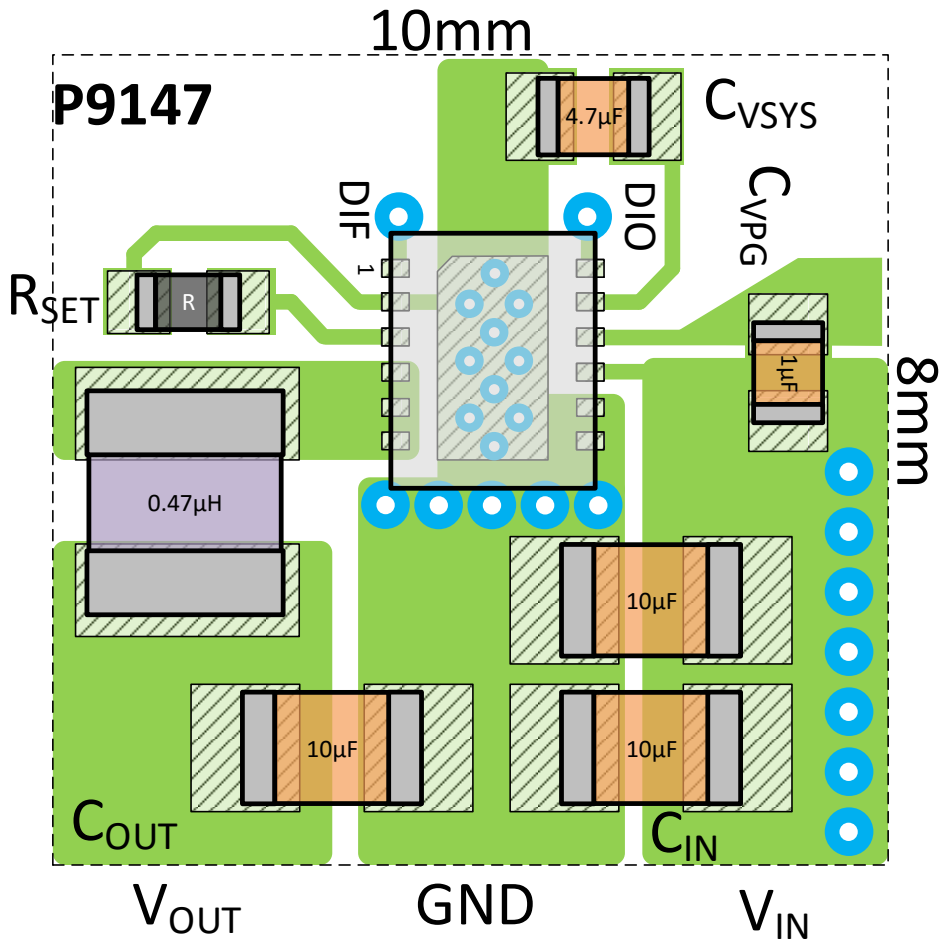
Note that in the example layouts for the DPUs presented in this section, there is a 10µF local $C_{OUT}$ configuration that is used in the case of widely separated DPU placements where the main $C_{OUT}$ capacitor cluster is located far away. The values of all components shown in the examples below are typical values. However, the value of these components depends on the specific application, so always check the datasheet of each DPU for more details on component selection.

## 6.1 Layout Recommendation for P9147

The recommended layout for a single P9147 is shown in Figure 12. All traces, planes, and components can be placed on the same side (bottom or top layer of the PCB). The exposed pad (EPAD) should be connected through vias to the ground plane(s). Care should be taken to place the PVIN input capacitors and VSYS capacitor close to the P9147, with the negative connection of the capacitor returning to the EPAD and the positive connection of the capacitor connecting with a short trace to the supply pins (PVIN and VSYS) of the P9147. The placement of the $R_{SET}$ resistor is not critical and can be on the opposite side of the board. DIF and DIO can be routed on an inner layer.

If the PVIN plane or the ground plane is not on the top layer, then vias can be used outside of the PVIN-PGND loop to connect the P9147 to those planes.

**Figure 12. P9147 Recommended Layout**

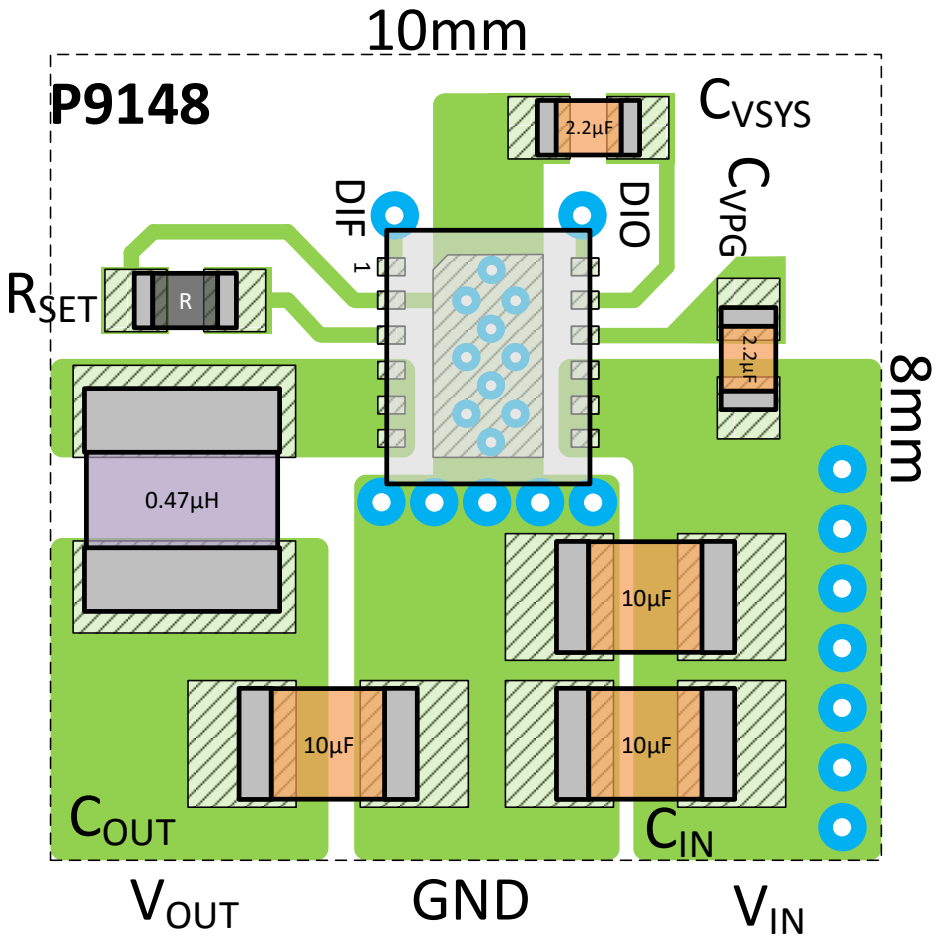



**Important:** Although the P9147 and the other DPUs discussed in this document use the same footprint and package (NRG12), they are not pin-to-pin compatible. Pins 7 and 8 of the P9147 must be connected to GND, while on the other DPUs these pins should be connected to $V_{IN}$.

## 6.2 Layout Recommendation for P9148

The recommended layout for a single P9148 is shown in Figure 13. All traces, planes, and components can be placed on the same side (bottom or top layer of the PCB). The EPAD should be connected through vias to the ground plane(s). Care should be taken to place the PVIN input capacitors and VSYS capacitor close to the P9148, with the ground connection of the capacitor returning to the EPAD and a short trace to the supply pins (PVIN and VSYS) of the P9148. The placement of the $R_{SET}$ resistor is not critical and can be on the opposite side of the board. DIF and DIO can be routed on an inner layer.

**Figure 13. P9148 Recommended Layout**

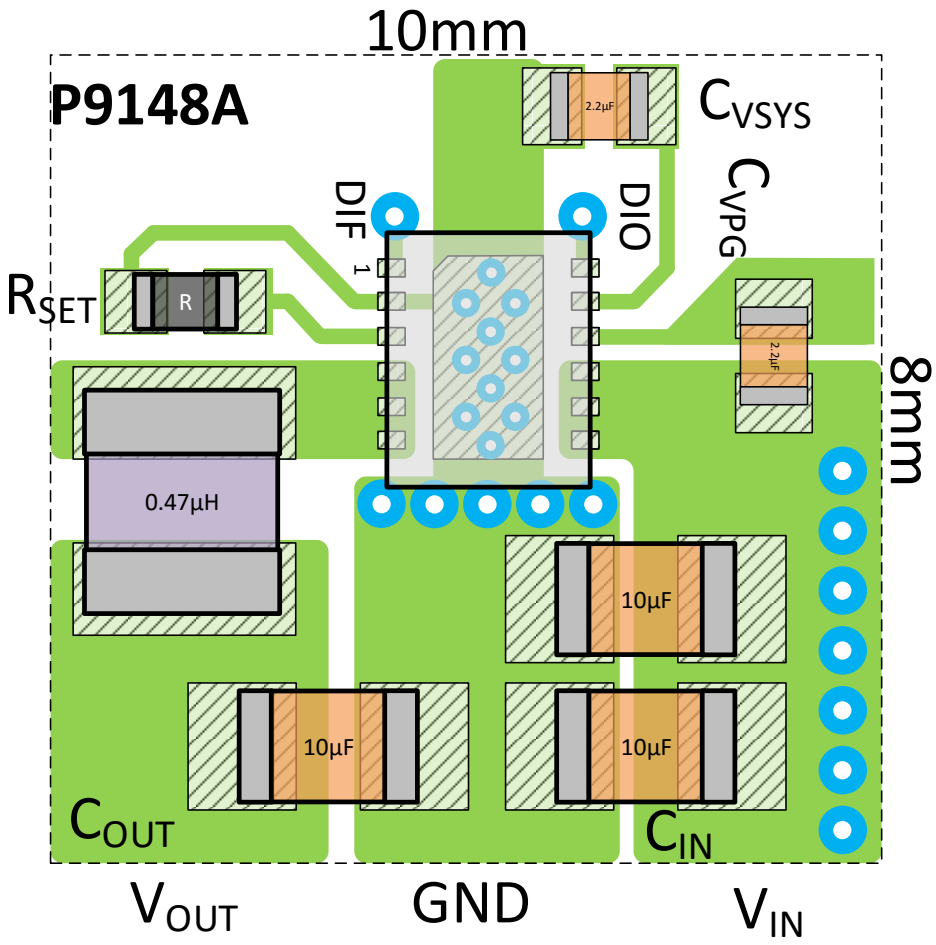



The main difference between the P9148 and the P9147 is that pins 7 and 8 are connected to $V_{IN}$ instead of GND. There is also a change in the values of $C_{VSYS}$ and $C_{VPG}$.

## 6.3 Layout Recommendation for P9148A

The recommended layout for a single P9148A is shown in Figure 14. All guidelines given for P9148 are valid here.

**Figure 14. P9148A Recommended Layout**




## 6.4 Placement of Multiple DPUs

If multiple DPUs are used, either to aggregate DCD0, DCD1, and DCD2, or in a controller configuration (DCD3/DCD4), the DPU layout for a single DPU is simply copied and placed several times on the PCB with the VOUT nodes joined together. The DPUs can be on the top or bottom layer of the PCB and if necessary even placed far away (1 to 4 inches) from each other. However, the VOUT capacitors must be placed together closely even though the individual DPUs may be separated and located on the top and bottom layer. It is important that the feedback connection is placed close to the output capacitors to ensure stable operation of the regulator. Figure 16 and Figure 17 show two example placements of multiple DPUs.

In the case when DPUs are widely distributed (e.g., at the four corners of the load device), avoid branching or using a star-connection on the DIO and DIF lines as this may cause signal degradation due to unnecessary reflections at branch points. Instead, use a daisy chain connection as shown in Figure 15.

**Figure 15. Connecting Multiple DPUs**

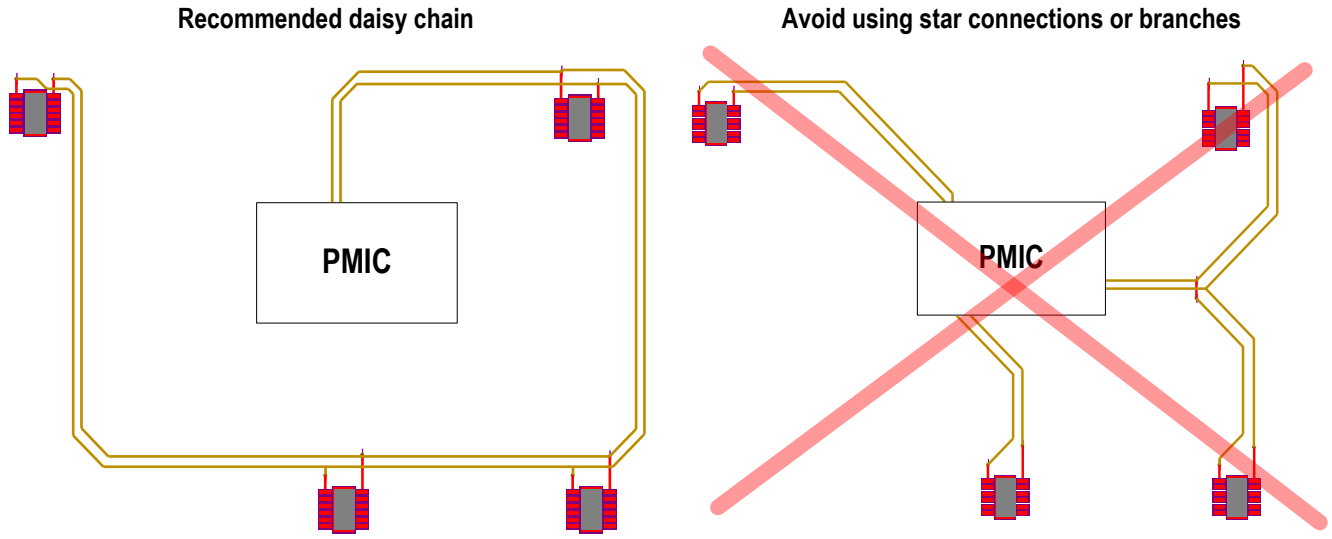



Figure 16 shows the placement of two DPUs in a controller configuration (using the DCD3/4 of the PMIC). It is important that the feedback connection is placed close to the output capacitors to ensure stable operation of the regulator.

If the DPUs are located close together, the 10µF capacitors near the DPU can be omitted.

**Figure 16. Recommended Layout for Multiple DPUs and Controller Configuration**

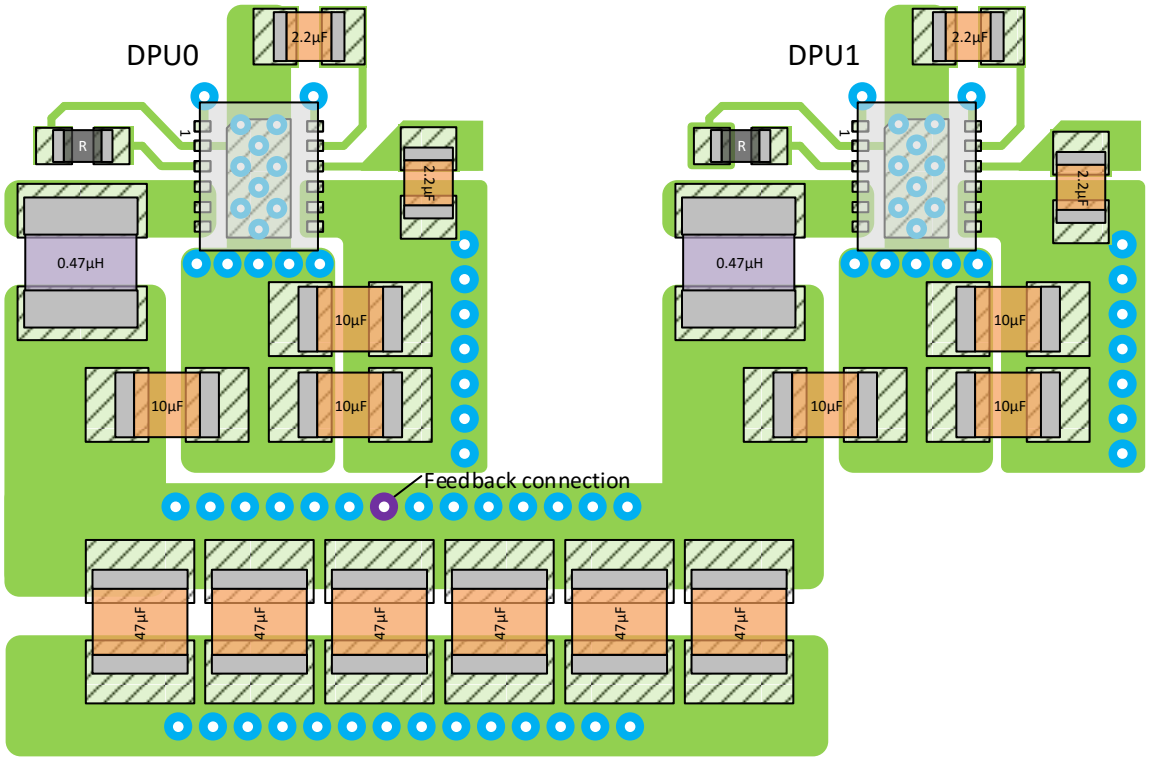
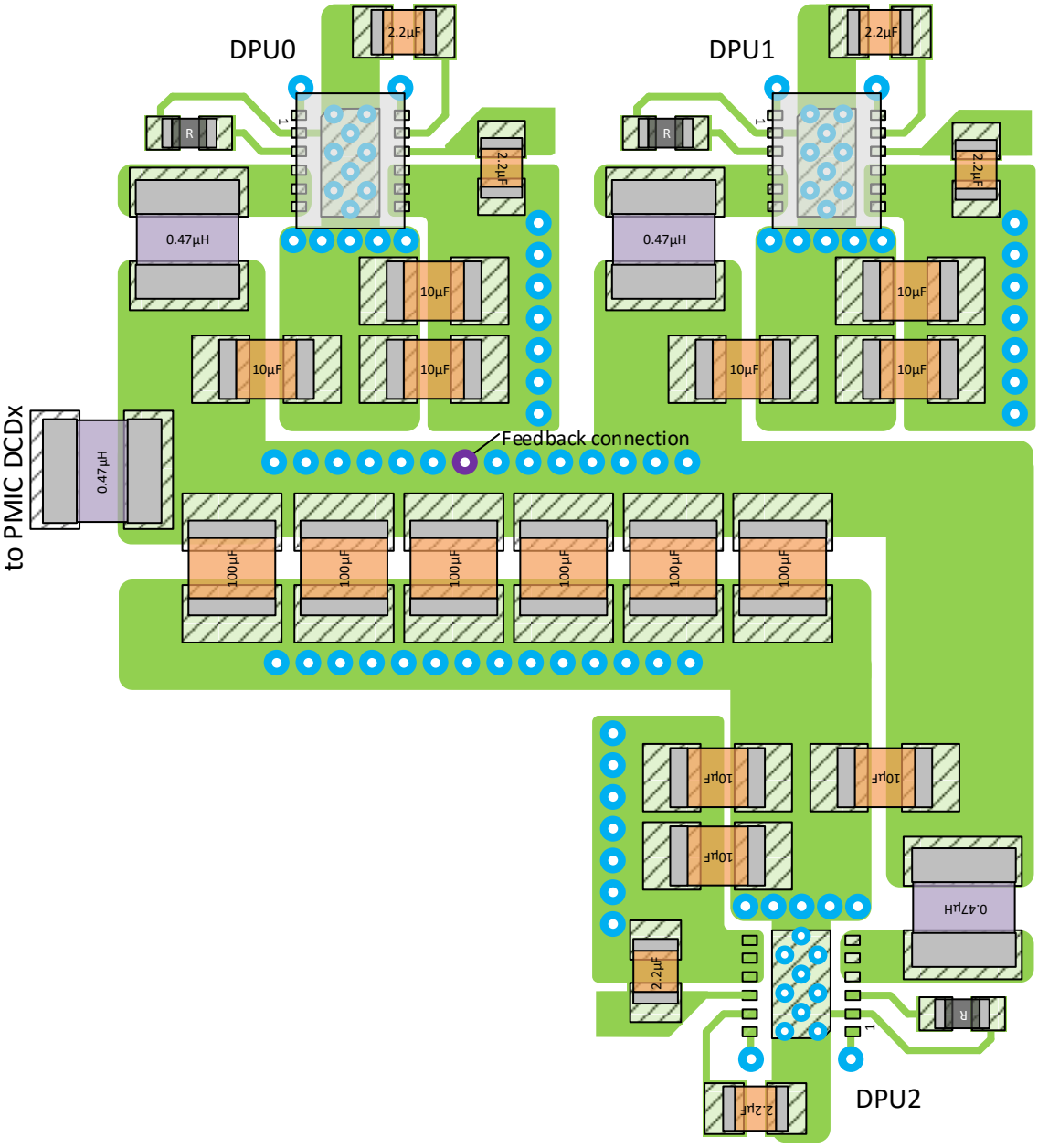


Figure 17 shows a configuration consisting of three DPUs that aggregate one of the P9145, P9180/A, or P91E0/A regulators (e.g., DCD0). This configuration can be seen as a 4-phase system. The left side of the sample layout shows the inductor of the P9145, P9180/A, or P91E0/A regulator connected to a common VOUT plane where the phases from all the other DPUs are also connected. The output capacitors are clustered together, rather than placed individually close to each DPU. The feedback signal back to the P9145, P9180/A, or P91E0/A PMIC is connected close to the output capacitors.

**Figure 17. Example Layout for 4 Phase Rail**



# 7. Examples of PMIC and DPU Layout

## 7.1 P9180/A and P91E0/A Evaluation Board

**Figure 18. Photo of the P9180/A and P91E0/A Evaluation Board Revision 3.1**

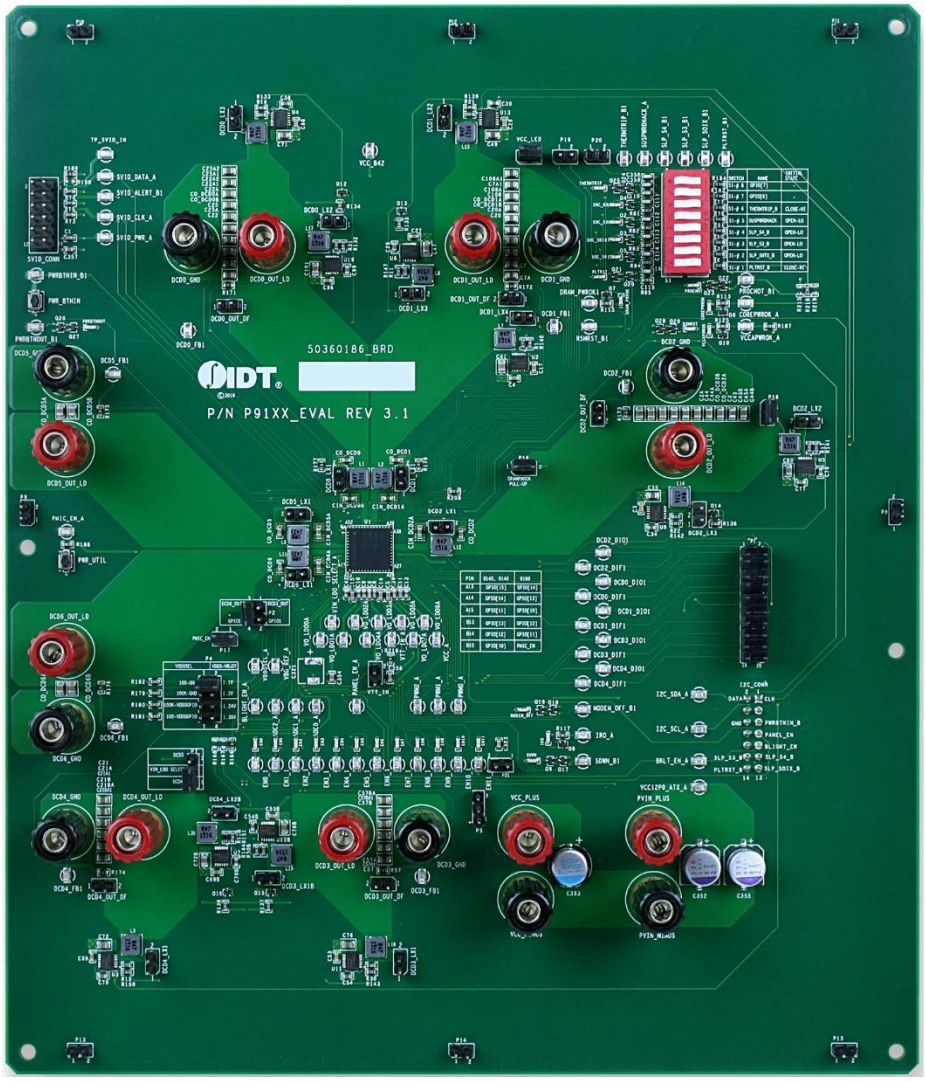
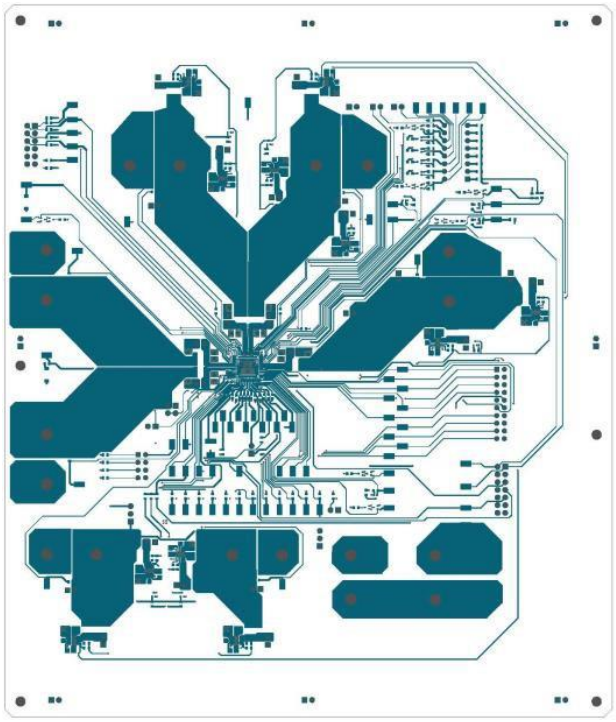
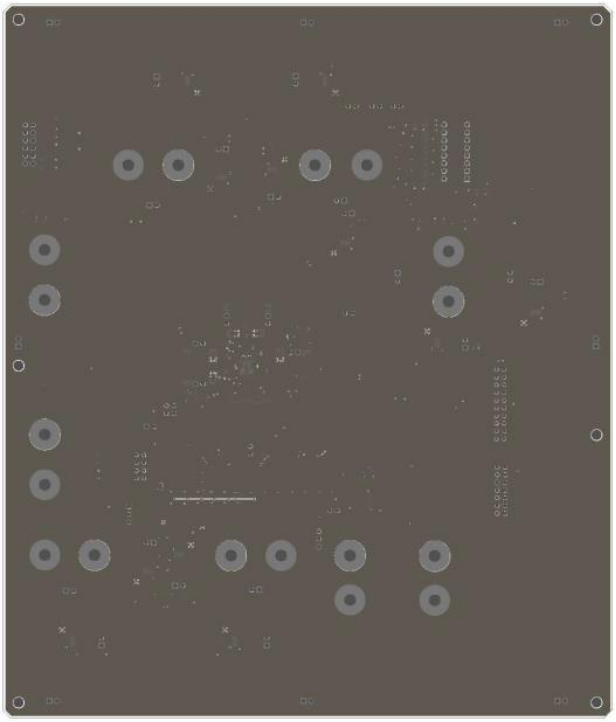


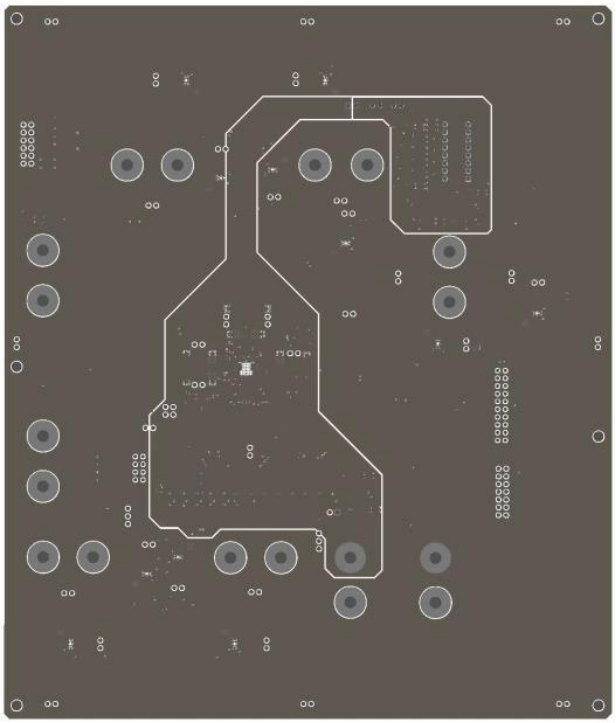
**Figure 19. Internal Layers of P9180/A and P91E0/A Evaluation Board Revision 3.1**



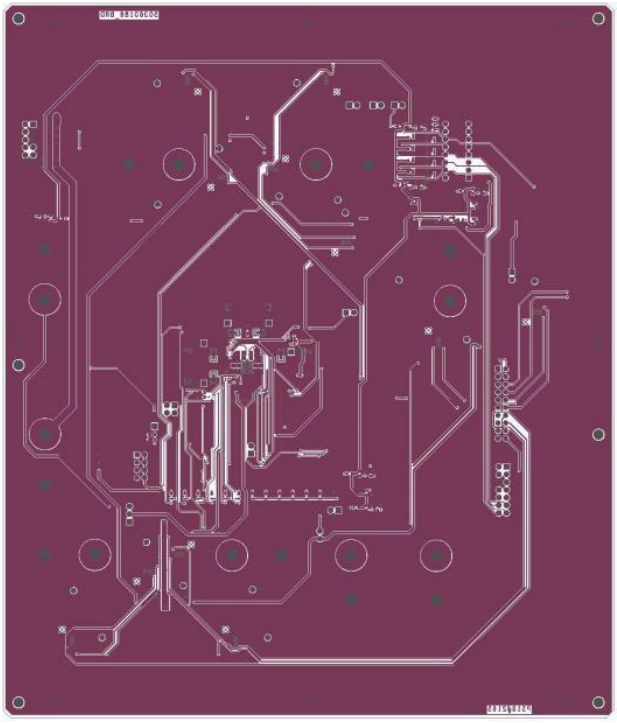
NHG100 Top Layout



NHG100 Layer 2 Layout

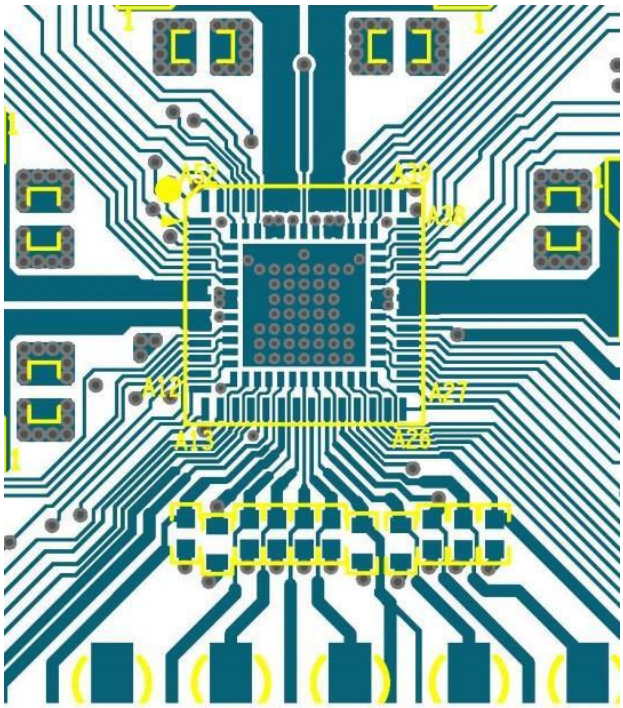


NHG100 Layer 3 Layout

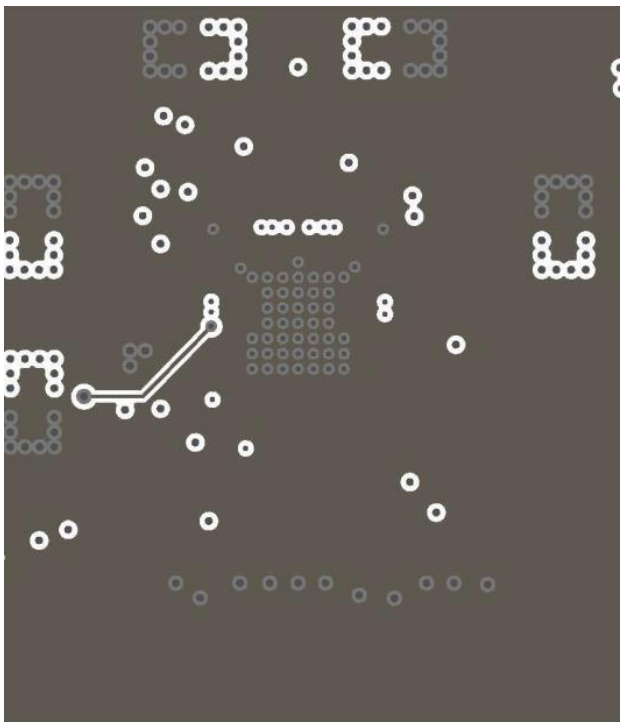


NHG100 Bottom Layout

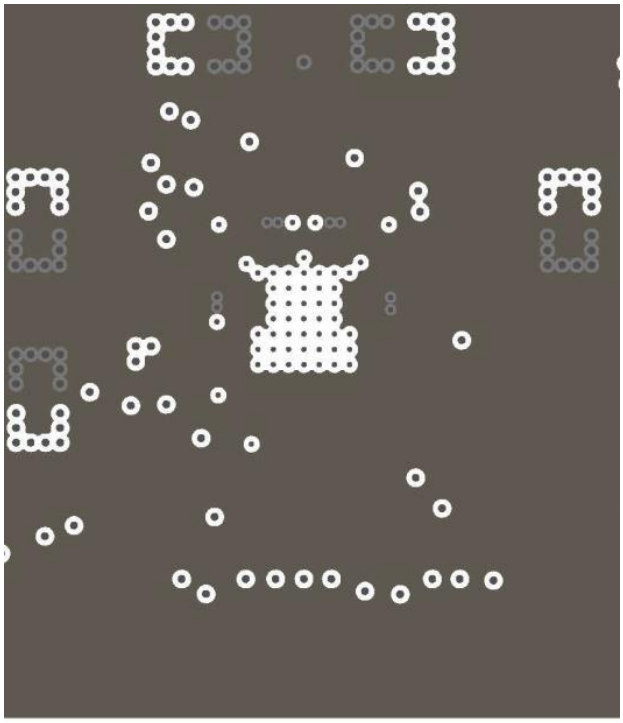
**Figure 20. Internal Layers of P9180/A and P91E0/A Evaluation Board Showing Only the PMIC Area**



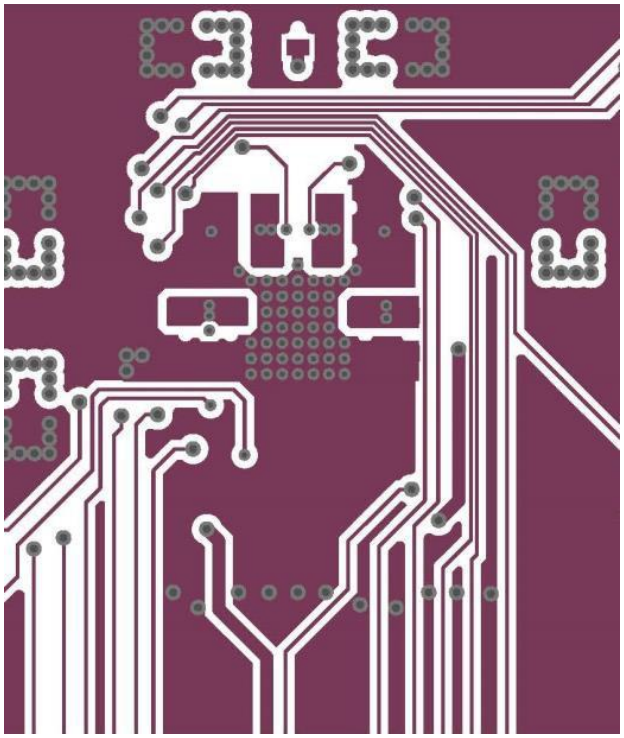
NHG100 Top Layout (IC Area)



NHG100 Layer 2 Layout (IC Area)



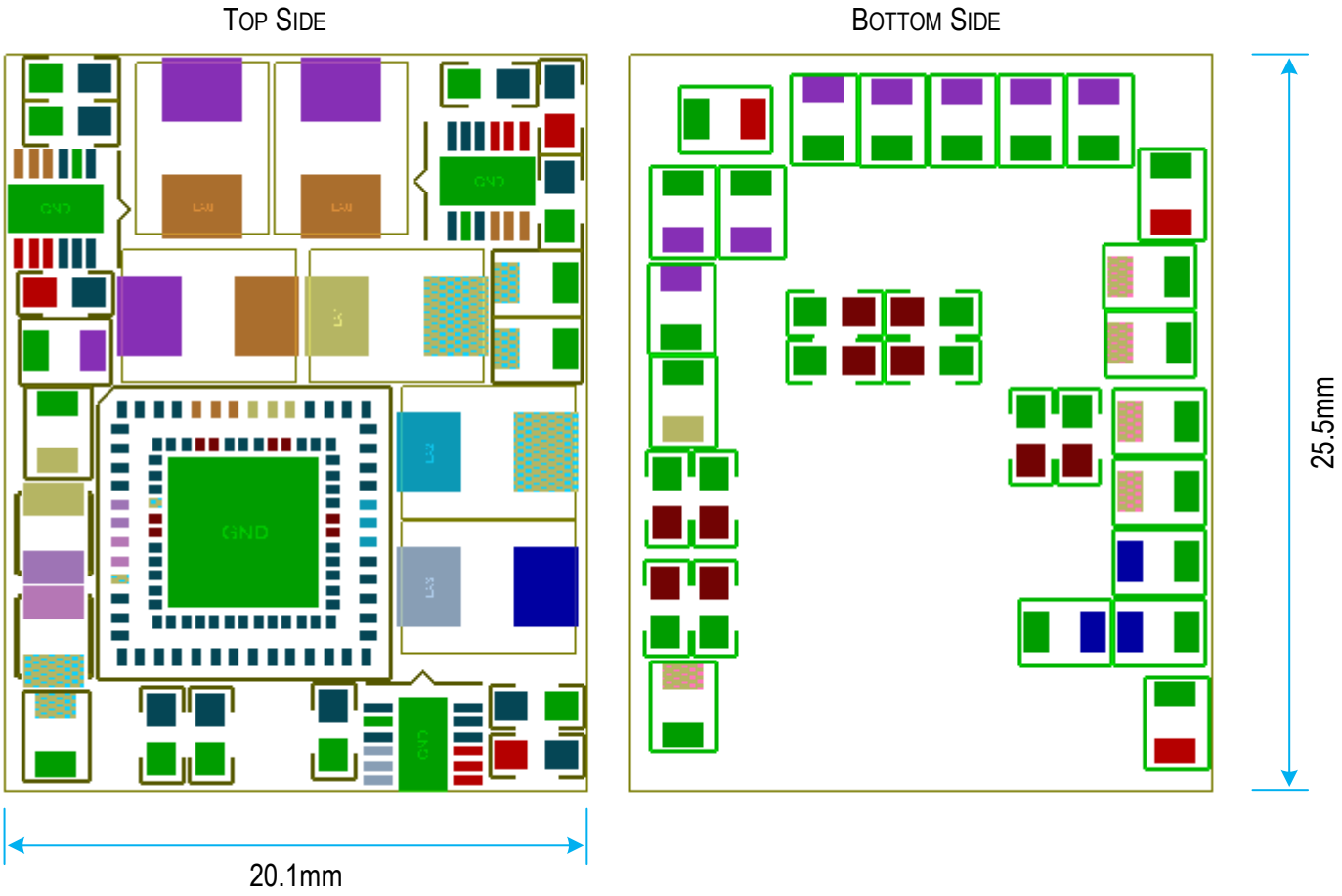
NHG100 Layer 3 Layout (IC Area)



NHG100 Bottom Layout (IC Area)

## 7.2 Example of Compact Layout with PMIC and DPUs

**Figure 21. Proposal for a Compact Layout**



# 8. Glossary

| Abbreviation | Definition |
|---|---|
| BOM | Bill of Materials |
| CRB | Customer Reference Board |
| DCDx | DC-to-DC Converter |
| DPU | Distributed Power Unit |
| ECAD | Electronic Computer Aided Design |
| EPAD | Exposed Pad |
| ESL | Equivalent Series Inductance |
| ESR | Equivalent Series Resistance |
| GND | Ground |
| HLA | Hi-density Leadframe Array |
| PCB | Printed Circuit Board |
| PMIC | Power Management Integrated Circuit |
| PTH | Plated Through Hole |
| QFN | Quad Flat No Lead |
| SoC | System-on-a-Chip |
| VFQFPN | Very Fine Pitch Quad Flat Package No-Lead |

# 9. Revision History

| Revision Date | Description of Change |
|---|---|
| September 5, 2018 | Full revision. |
| July 27, 2017 | Initial release. |

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)


### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com


### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.