

**P9412**

**Ping Detect Design Guide**

**Abstract**

This document explains the P9412 digital ping detect feature and the schematic connections needed to support Ping Detect (PDET). The Ping Detect feature enables the host Application Processor (AP) to have an interrupt driven method of determining whether the mobile device is currently placed on a valid transmitter. Many uses can be established related to knowing that a Tx is within charging distance and this information can enhance your experience. This guide explains how the feature works and the connections that are needed to implement PDET using the P9412.

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## 1. WPC Digital Ping and P9412 Ping Detect

The P9412 has integrated the ability to provide an output to the host AP to indicate detection of a valid WPC digital ping event. The digital ping is used by the Tx to establish a wireless connection with the Rx following the WPC protocol for establishing power transfer. The standard digital ping lasts for 80ms and the digital ping interval varies from transmitter to transmitter, but typically occurs every 2 seconds or less. The following are the key benefits of the P9412 type of ping detect:

- The open-drain (OD) output generates a falling edge interrupt by driving low and requires no AP polling.
- The Ping Detect solution uses an internal low-power clock and does not require any timing related components (such RC time constants).
- This Ping Detect can adapt to various digital ping intervals automatically.
- Ping detect is very low power (<1.8 $\mu$ W) when waiting for a Digital Ping detection.

The most common use of PDET is to conserve power after charging has completed. The wireless power connection to the TX can be ended using an End of Power Transfer (EPT) packet to save power while still having the option to top-off the battery periodically. The P9412 then indicates to the host Application Processor (AP) that it is still on the charging pad by using the PDET<sub>B</sub> (GPOD6 pin) and using the SW\_Inhibit pin to prevent the P9412 from connecting to the Tx pad. The PDET<sub>B</sub> pin must be externally pulled up to the host 1.8V AP power supply rail and is held low if TX PING pulses are detected (or whenever a wireless power connection is active). If a time interval of about 5s passes from the previous digital ping to the next expected digital ping, the PDET<sub>B</sub> pin is released to indicate to the host AP that the wireless device has been removed from the Tx charging pad. Otherwise, the PDET<sub>B</sub> pin is held low while the Rx is detecting incoming Ping events. Proper operation of Ping Detect also requires 1.8V applied to V1P8AP and GPOD0 pulled to GND. The remainder of this document explains the P9412 digital ping detect in more detail.

### 1.1 Ping Detect Use Cases

- Early detection of placement onto a Tx Pad:
  - PDET provides early indication that the Rx has been placed on a pinging Tx (independent of SW\_Inhibit state).
- Rx remains placed on a Tx pad:
  - Indicates Rx is currently placed on a Tx pad (independent of charging state).
- Rx removed from Tx:
  - PDET indicates Rx removed from Tx pad.
    - 1st rising edge indicates Rx lifted, 2nd rising edge confirms full removal.

1.1.1. Ping Detect Use Case: Rx Already Placed then SW\_Inhibit Toggled

- Setup: Rx already charging (PDET LOW), then SW\_Inhibit toggled high. Rx Sends an EPT, then ignores the ping events until SW becomes active by the SW\_Inhibit pin:
  - P9412 evaluation board placed on P9247 and actively charging
    - 1.8V applied to V1P8AP.
    - GPOD0 (Tied to GND, ping detect function enabled).
    - GPOD5 (SW\_INHIBIT, active low).
    - GPOD6 (PING\_DET output, active low).
    - Rx on Tx charging pad always.
- Stimulus:
  - Toggle GPOD5 from low to high and then high to low (SW\_Inhibit toggled, CH2 (OD5)).
- Behavior:
  - VRECT shuts down when SW\_INHIBIT is high by sending EPT to Tx.
  - GPOD6 always low (with ping or power transfer).
  - Digital Ping ignored until SW\_Inhibit is pulled to GND, then connection is re-established.

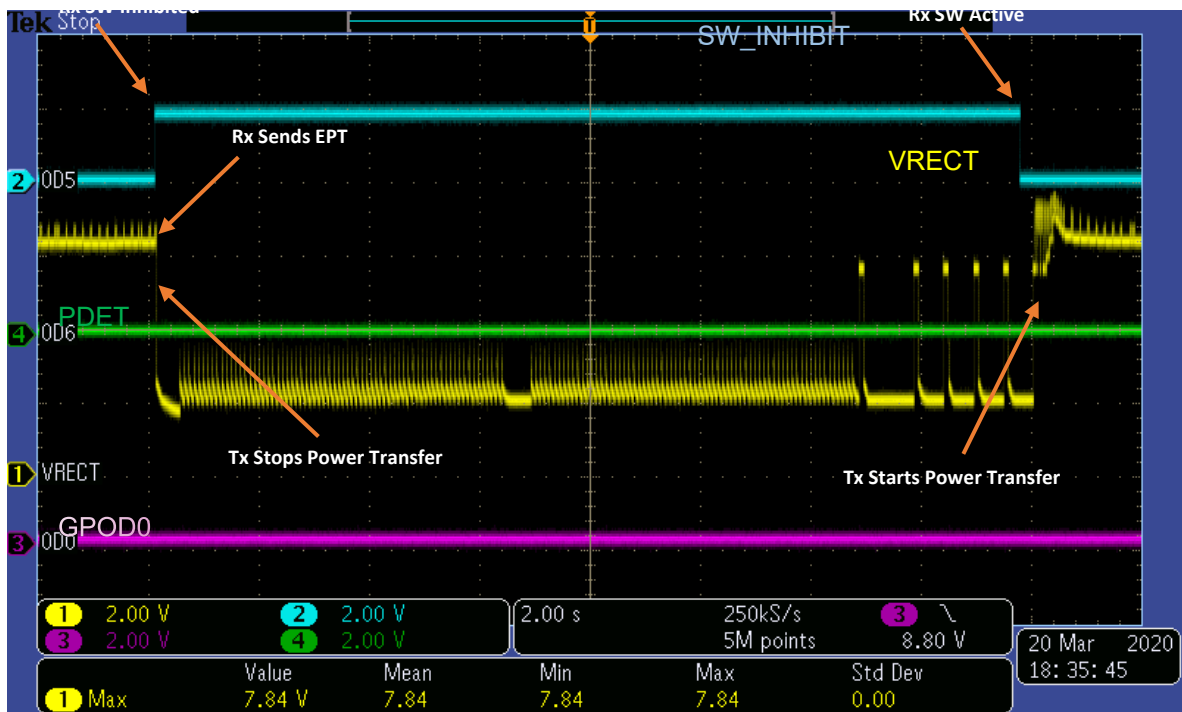


Figure 1. Waveform of PDET (OD6) Output Remaining Low During Power Transfer and Ping Phase Independent of SW\_INHIBIT State when Rx Remains Placed on a Tx Pad.

1.1.2. Ping Detect: Rx Removal and Placement with SW Active (SW\_Inhibit = GND)

- Setup: P9412 Rx placed on Pinging Tx
  - P9412 evaluation board placed on P9247 and actively charging, then removed by user
    - 1.8V applied to V1P8AP
    - GPOD0 (Tied to GND, ping detect function enabled)
    - GPOD5 (SW\_INHIBIT = GND; SW active)
    - GPOD6 (PING\_DET output, active low)
- Stimulus:
  - Rx removed and placed back on Tx pad
  - SW\_INHIBIT Low
- Behavior:
  - VRECT goes low when Rx is removed from the Tx pad.
  - GPOD6 goes high when Rx is removed to indicate to the AP that the Rx is no longer on the Tx pad.
  - GPOD6 goes low when Rx is approaching a WPC Tx pad (Ping Detected).
  - VRECT goes high from the digital ping and a wireless connection is established.

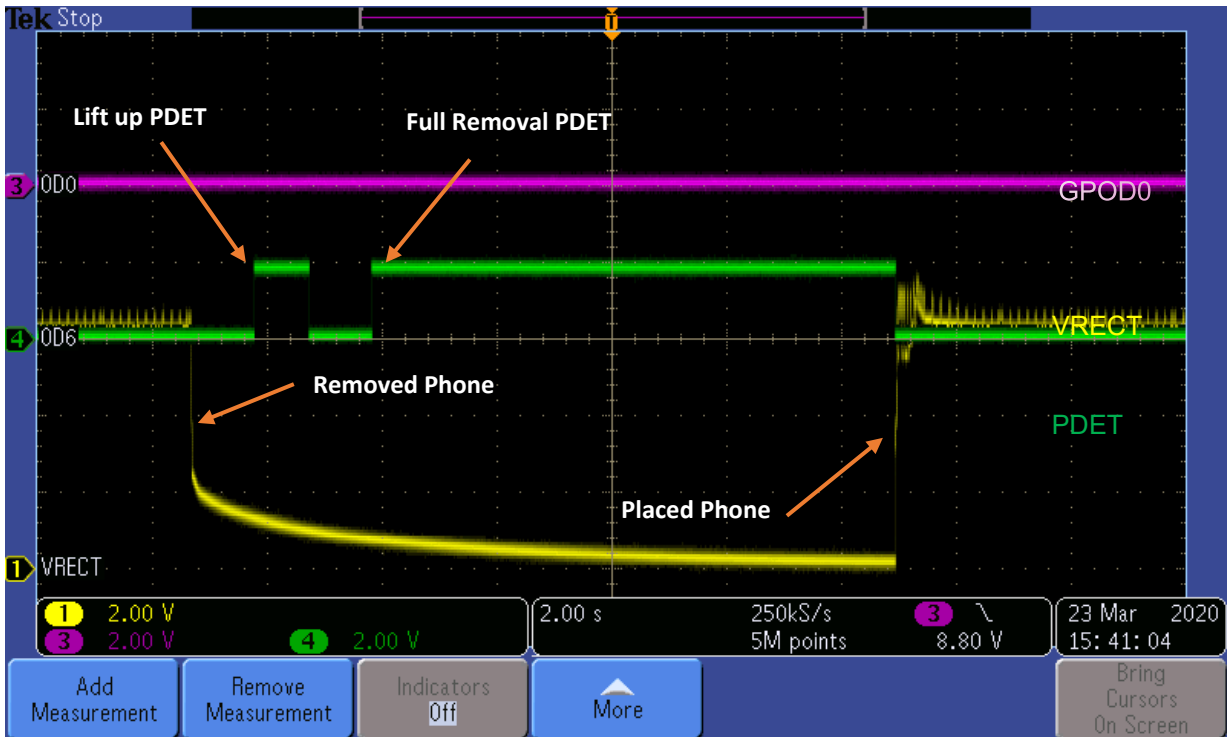


Figure 2. Waveform of PDET (OD6) Output Indicating Rx Removal and Placement onto a WPC Tx Charging Pad.

1.1.3. Ping Detect: Rx Removal and Placement with SW\_Inhibited (SW\_Inhibit = 1.8V)

- Setup:
  - P9412 evaluation board placed on P9247 and Inhibited, then removed by user
    - 1.8V applied to V1P8AP
    - GPOD0 (Tied to GND, ping detect function enabled)
    - GPOD5 (SW\_INHIBITed, set to high)
    - GPOD6 (PING\_DET output, active low)
- Stimulus:
  - SW\_INHIBIT HIGH
  - Rx removed and placed back on Tx pad
- Behavior:
  - GPOD6 goes high when Rx is removed from the Tx pad
  - GPOD6 goes low when Rx is placed on the Tx pad.



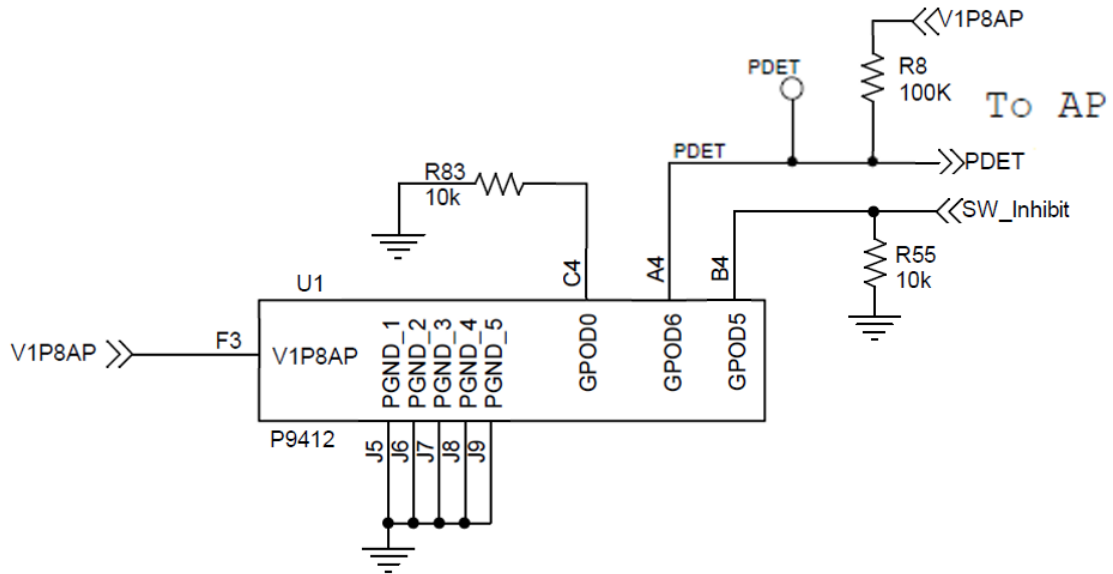
Figure 3. Waveform of PDET (OD6) Output Indicating Rx Removal and Placement with SW\_Inhibited.

## 2. Schematic Level Implementation

The schematic level implementation is based on P9412 reference schematic.

1. Ping Detect Connection diagram and description:

- a. Add a pull-down (R83) from pin GPOD0 (10kΩ) to GND to enable Ping Detect.
- b. Add a pull-up (R8) from pin GPOD6 (100kΩ) to 1.8V AP supply rail to monitor Ping Detect.
- c. Connect the 1.8V AP I/O power supply to the V1P8AP (pin F3).



### 3. Revision History

Revision	Date	Description
1.0	Jul.21.20	Initial release.

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