Application Note

PCB Layout Guidelines

AN-PM-010

Abstract

The reliability and performance of an integrated power management solution is dependent on an optimised PCB layout. This application note provides practical guidance to system designers and PCB layouters. Layout examples are illustrated based on Dialog's own reference designs.

Contents

Figures

1 Terms and Definitions

PMIC	Power Management IC
EMI	Electromagnetic Interference

2 References

[1] DA9053, Datasheet, Dialog Semiconductor

[2] DA9062, Datasheet, Dialog Semiconductor

[3] DA9063, Datasheet, Dialog Semiconductor

[4] IPC-2152, Standard for Determining Current Carrying Capacity in Printed Board Design, IPC, 2009

3 Introduction

PCB layout is a critical part of all switching power supply designs. As there are high switching currents and sensitive control signals in close proximity, control of the PCB layout is needed to ensure the correct operation of the system.

It is important to use ground and power planes with high current power management devices. Dialog recommends that you use both a ground and main system voltage plane underneath the PMIC. The input decoupling can then decouple the planes. As both VDD and GND are planes, inductive cancellation will provide a very low impedance path to the IC.

It is not possible to produce a set of rigid rules for layer construction within a PCB because each design has its own requirements: it is not appropriate for Dialog to suggest which plane should be power and which should be ground. Instead, this application note uses examples from the Dialog PCB range to illustrate practices that have been found useful.

3.1 Design Help and Guidance

In most sales regions Dialog offers to review customer schematics and PCB layouts. Use of this design-in service is recommended to ensure power management solutions are optimised for reliability and efficiency. Please contact your Dialog sales representative for service availability information.

4 General PCB Layout Guidance

Sections 4.1 and 4.2 discuss general PCB layout rules that can be applied to the whole design. Section 4.3 onwards addresses guidelines for specific parts of a Dialog PMIC, for example buck converters and LDOs.

Key layout principles include:

- Current-carrying traces are as thick as possible
- The board has a low impedance ground
- Sensitive signals are shielded from interference by noisy traces

4.1 Ground Impedance

The ground plane should have low impedance for all areas of the PCB. This will help with power control, will improve signal quality and reduce EMI.

The use of a ground layer and flooding of other layers with multiple vias are good methods to keep the impedance low.

Below are two PCB ground layers as examples of good and bad grounding.

4.1.1 Example of Layout with Poor Ground Impedance

Note the thin ground paths leading to the centre ground pads of the PMIC in Figure 1. These narrow sections of the ground plane can cause operational problems with buck converters as the ground impedance is too high.

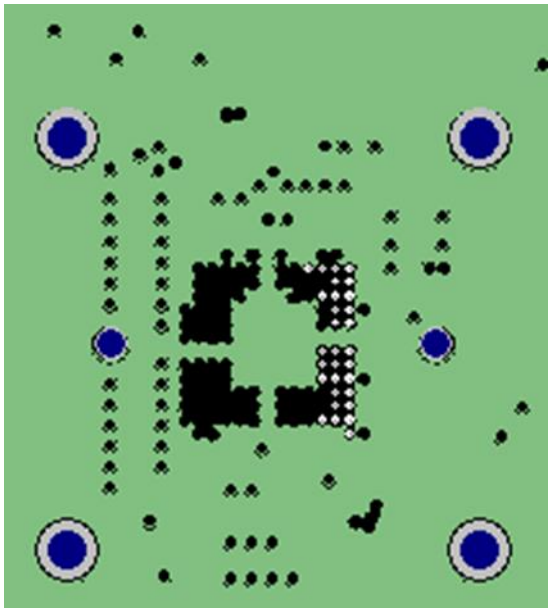


Figure 1: An Example of Poor Ground Impedance

4.1.2 Example of Good Layout with a Low Ground Impedance Layer

Note the good flooding of the ground around and under the PMIC in Figure 2. There are good low impedance paths from any location around the periphery of the PMIC into the centre ground pads.

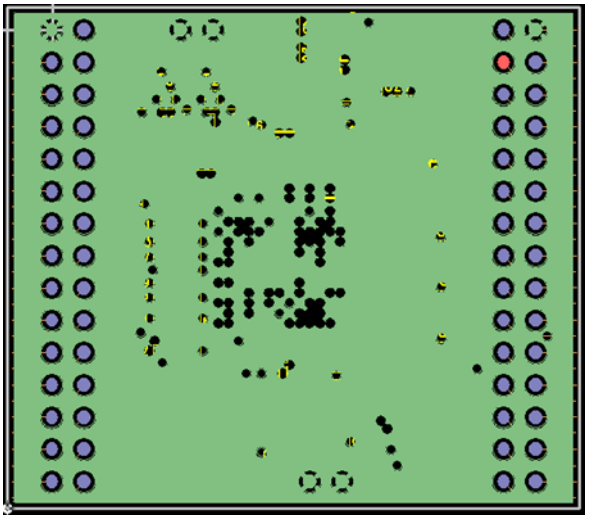


Figure 2: An Example of Good Ground Impedance

4.2 PCB Layers and Shapes

Dialog products often have a high pin count and therefore multi-layer PCBs are required. It is recommended that one of these layers is reserved for ground and one for the main power. For example, when considering a six-layer reference board from Dialog, one may typically find that the ground plane is Layer 3, and the VDD plane is Layer 4. The recommendation is that these GND and VDD planes are adjacent.

Use of plane shapes, where possible, is recommended for all high current input supplies such as VBAT, DCIN and VBUS. These are frequently used on Dialog reference boards. This has the added benefit of reducing power losses.

When reviewing the ground and power planes, ensure that the plane is not too ‘cut-up’ by vias. Consideration must be given to current flows between the layers. Examples of ground planes, via placement and plane shapes are shown in section 4.6.

Maximise the effectiveness of decoupling capacitors. To minimise the inductance between the capacitor and the power pin of any device, place the capacitor as close as possible to the device. Long, thin traces and vias have an inductive element and reduce the effectiveness of decoupling capacitors. Similarly, the capacitor should have a low impedance connection to ground to minimise the impedance of the capacitor.

Flood all unused PCB areas with ground: this further reduces ground impedance.

4.2.1 Vias

PCB vias are inductive at high frequencies and will therefore increase the ground impedance. Having multiple vias in a plane will reduce this effect as the inductances are in parallel.

Dialog recommends the use of ground-fill for the remaining layers. When using ground-fill, it is important that there are plenty of vias connecting this fill to the main ground plane. These vias must be spaced in such a way that the power plane is not excessively cut-up.

4.2.2 Star Grounding

Dialog recommends the use of a single ground star point for the different ground sections of a PCB. This should be at a point where the ground signal is at its cleanest, for example near to the power input. For optimum performance, this is also where the PMIC should be placed (Figure 3).

An ideal location for the star ground point is the main PMIC ground pins as all the system power is distributed from this device. This is often a group of ground balls in the centre of a BGA PMIC.

Daisy chaining section grounds, where the ground from one section feeds the next, should be avoided. Daisy chaining would cause each successive section to inherit ground noise from previous section (Figure 4).

Keep ground currents separate. The common grounds for analog and digital circuits must be kept separate to avoid digital noise being conducted to the analog circuits. The best way to do that is by optimising device placement. If all analog and digital circuits are placed on separate parts of the PCB, the ground currents will be naturally isolated.

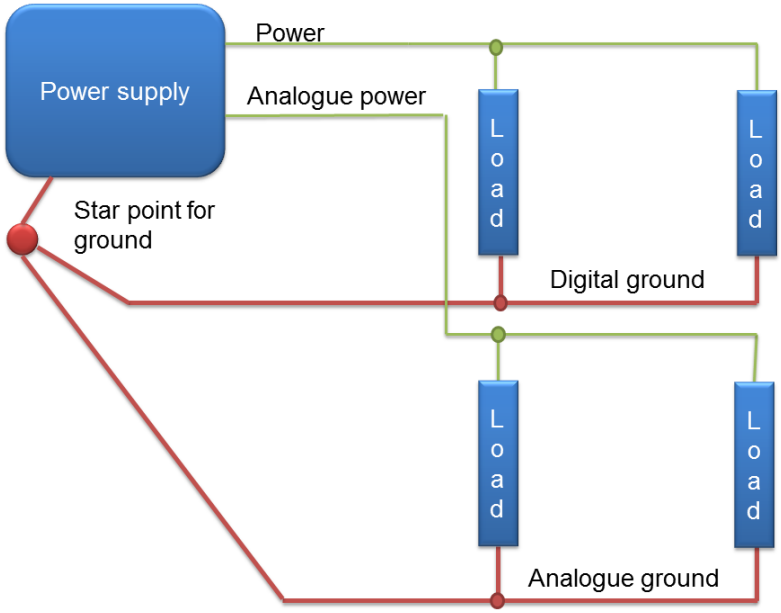


Figure 3: A Star Ground (Recommended)

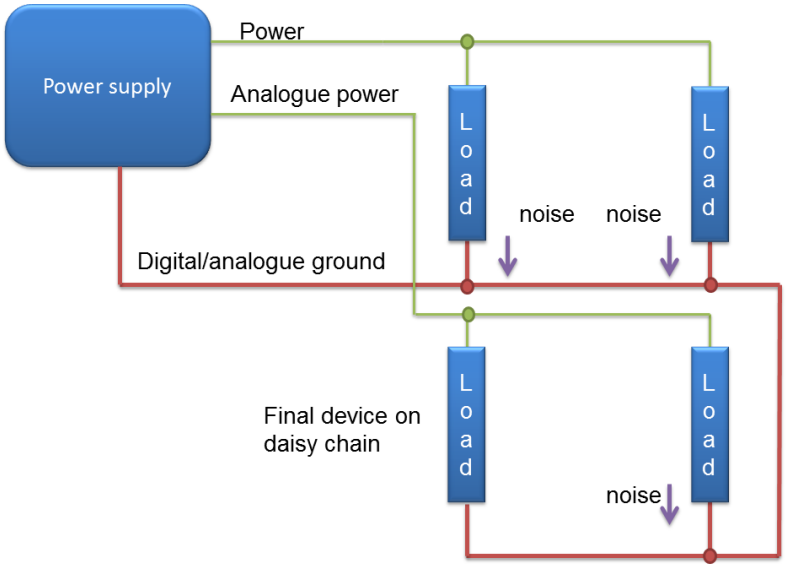


Figure 4: Daisy Chain Grounding (to be Avoided)

4.2.3 Ground Loops

A ground loop is where there is more than one return path in the ground of a load (Figure 5). Ground loops may cause several problems: firstly, impedances of the multiple paths will differ, which causes uneven current flows in the system. For example, this may result in large analog ground currents affecting more sensitive areas of the system. Secondly, the ground loop represents a single coil winding that is sensitive to magnetic fields or can emit them. This will impact EMI performance. Ground loops need particularly careful consideration during the layout of multi-layer boards as they are often difficult to identify.

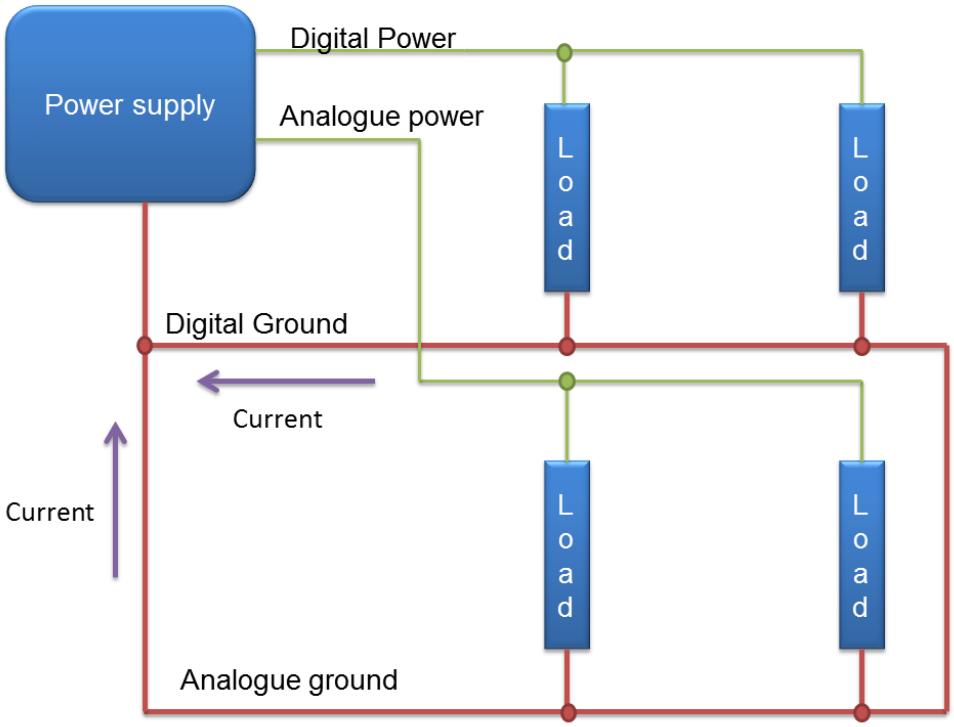


Figure 5: Example of a Ground Loop

4.2.4 Ground Zones

Ideally, the star point grounds for the analog circuit and the digital circuit should be separated. This separation should be maintained across the whole PCB design. For example, it is not a good idea to cross a sensitive analog section of the PCB with a noisy digital ground flood or shape.

4.2.5 Placement of External Components

There are critical parts of a design that need to be placed as close to each other as possible. These include switching inductors and their capacitors, and crystals with their drive-pin reference-setting components. As this is not always possible, priority should be given to the layout of sensitive parts and high current devices, because long traces would otherwise affect the performance of the system.

4.2.6 Power Supplies

As with the ground, Dialog recommends a complete layer for the main power supplies. Keeping the impedance low will reduce losses in the PCB and improve its efficiency.

4.2.7 Audio

Some Dialog products feature audio sections. These audio sections should be kept clean and away from noise. Dialog recommends using a separate star ground feed for the audio section.

4.3 Boost-, Buck-, and LDO-Specific Layout Guidelines

This section provides guidance for the layout of specific areas of a power supply.

4.3.1 Boost and Buck Converters

The switching regulators are a critical section of any design. Ideally, all connections would be as short as possible with the input decoupling capacitor placed directly at the input pin. However, priorities must be chosen because of the high level of integration in the PMIC. As discussed in section 4.2.6 above, Dialog recommends the use of a VDD power plane, with the input decoupling capacitors attached to it. These capacitors should still be placed as close as possible to the PMIC, but not at the expense of potentially more critical components such as IREF and VREF reference components.

Care should be taken not to cut up the VDD plane with plated-through holes. Using micro/laser vias for ground connections helps reduce this cut-up as they are smaller and do not affect the inner layers. Many PCB layouts feature a micro-via stitching ring around the outside of the PCB. This helps reduce EMI and ground impedance without cutting the inner ground layer.

The inductors should be placed as close as possible to the PMIC. The LX node traces from the PMIC to the inductors are a source of EMI. Larger traces produce more radiation but are more efficient as they have smaller resistive drops. The size of these traces is therefore a compromise which needs careful consideration. The Dialog reference designs have wide LX-traces as we optimise our designs for efficiency. Advice on calculating suitable trace width is described in [4].

The feedback trace should be taken directly from the output at the capacitor pad. It is also possible to take the feedback from the point of load, but this increases the risk of noise being introduced onto this trace because of the extra length it would run. Good power planes can avoid the need for such point of load feedback configuration.

The feedback trace must be shielded from all noise sources, especially the LX nodes of buck converters. Noise fed into a feedback pin often creates extra voltage ripple on the buck output. In the reference design example of section 4.6.1, the feedback traces are on the bottom layer and therefore away from the noisy LX nodes.

No signals should run on Layer 2 under the LX traces or under the inductors. On the Dialog reference design there is only a ground plane. This layout guideline must be followed as noise coupling from the LX switching currents and from the magnetic fields around the coils are likely to cause signal integrity problems.

The output capacitor is to be placed as close to the inductor as possible. Dialog recommends that the power rail is connected to a plane shape after this point if it is delivering significant power. This will ensure adequate performance of the system. It will also avoid the need to compensate for trace IR-drops by attempting to set the buck output voltage higher than the desired load voltage. Such compensation is rarely satisfactory, especially where the load varies considerably.

The above guidelines are summarised in Figure 6 as the basic principles for buck layout. An example with a buck that has differential (VSS) sensing is summarised in Figure 7.

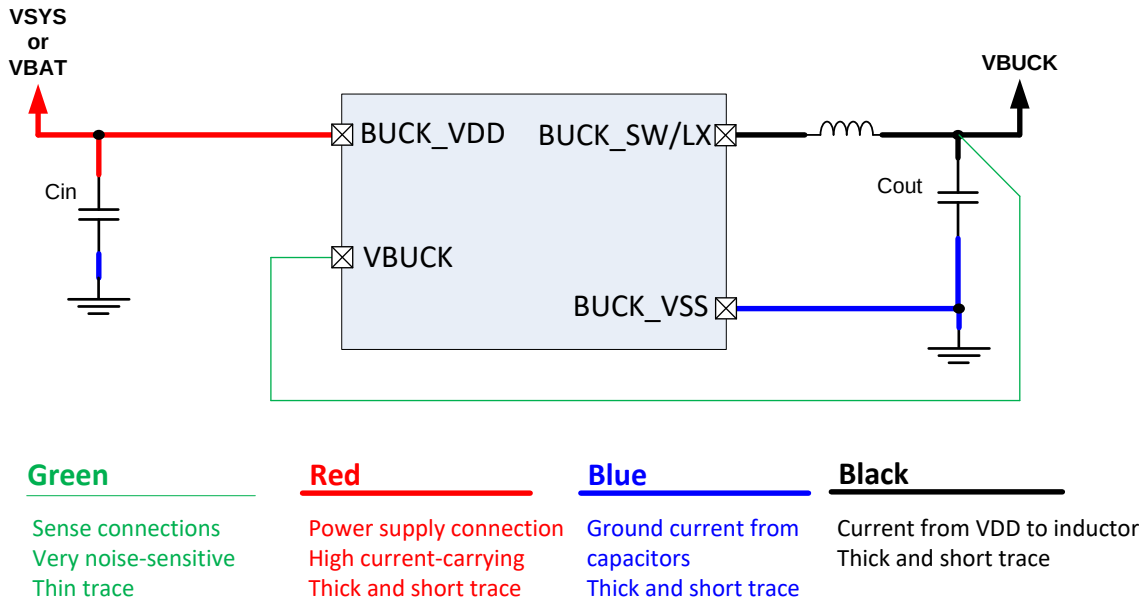


Figure 6: Buck Layout Principles

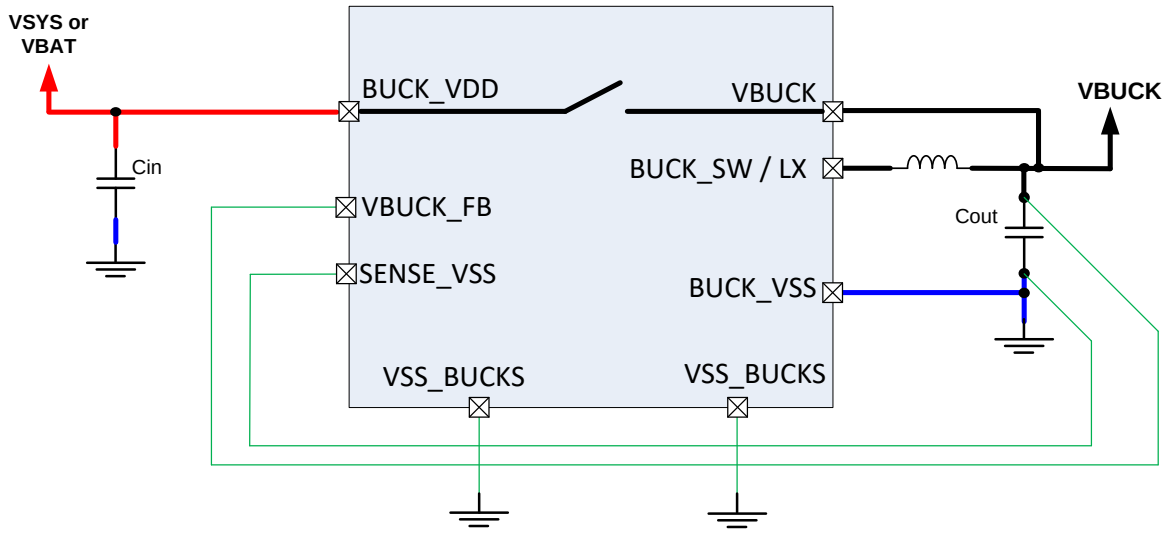


Figure 7: Buck Layout Including VSS Sense and Bypass-/Rail-Switch

4.3.2 LDOs

LDOs do not require such careful layout as buck convertors, although their performance is highly dependent on two external factors:

- Dropout: The LDO is affected directly by the impedance of its supply. Any increase in distance between its VDD supply pin and the input capacitor will introduce additional dropout. Whenever possible, the LDO ground of the PMIC should be connected directly to a low impedance ground plane. The input capacitors should then decouple to the same plane.
- Load Regulation: The load regulation can be affected by the impedance of the trace between the PMIC output pin and the load. This impedance should therefore be kept as small as possible. By default, the output capacitors of the LDOs should be placed as close as possible to the PMIC. Placing capacitors remote from the PMIC might be possible in certain circumstances, but this is at the expense of load regulation performance. Ultimately, if the trace resistance becomes too large then a risk of LDO instability will be introduced. Since remote capacitor placement requires careful design consideration, PCB layouters should only implement this scheme if there are specific instructions to do so from the system designer.

4.4 REFERENCE PINS

The reference connections should be kept noise-free, including all reference components connected to IREF and VREF. These should be placed as close as possible to the PMIC pins that they connect to. They should also be placed in a ‘quiet’ area with noisy signals neither routed on the layer below, nor too close on the same layer. Where possible, the layouter should have ground on the layer below the references.

4.4.1 IREF

IREF is a reference current for many blocks internal to the PMIC and therefore the value of the IREF resistor is critical. Handling the bare PCB in this area while the device is powered-up can cause this reference current to change and may cause the current limit control in the device to malfunction. This can result in permanent device damage.

4.4.2 32 kHz Clock

The 32 kHz crystal circuit must be placed in a quiet area. Ground guard traces should be routed on either side of the X_{IN} and X_{OUT} traces to avoid frequency shifts. Additionally, there should be a ground plane shape under these traces and under the crystal. Ensure that no noisy signals are routed close to or under this circuit. See layout examples in section 4.6.

4.4.3 ADC

A clean analog input signal is required for accurate ADC operation. ADCs have low currents and low frequencies and can therefore be given a lower layout priority than many PMIC traces, but higher priority than the GPIO and other digital pins.

4.4.4 GPIO

GPIO pins are usually unaffected by the layout and so can be given a low priority during layout.

4.5 Battery Charger

The VCENTER pin and its capacitor (highlighted in orange in Figure 8) is an important part of the charger circuit. It is the main input decoupling for the charger buck. The capacitor should have wide traces and be fitted as close to the IC as possible. The capacitor must be placed on the same side of the PCB as the PMIC.

Where the use of a Schottky diode is recommended between VSW and ground, the diode should be placed close to the device and the PCB traces kept as wide as possible. It is important that the Schottky is connected to a solid low impedance ground.

4.5.1 Power Input Lines

The VBUS and DCIN inputs are for sensing voltages and are not high current signals, whereas the VBUS_PROT and DCIN_PROT are the high current traces and should have wide traces. The decoupling of DCIN_PROT and VBUS_PROT should be fitted as close as possible to the input balls.

Where possible, it is recommended that a plane shape is used for VDDOUT. VDDOUT is the main power rail and is also the feedback for the main charger/system buck.

4.5.2 External Active Diode

The external active diode, if used (highlighted red in Figure 8), is intended to provide the lowest impedance path possible from the battery to VDDOUT and for that reason its location and tracking should take this into consideration.

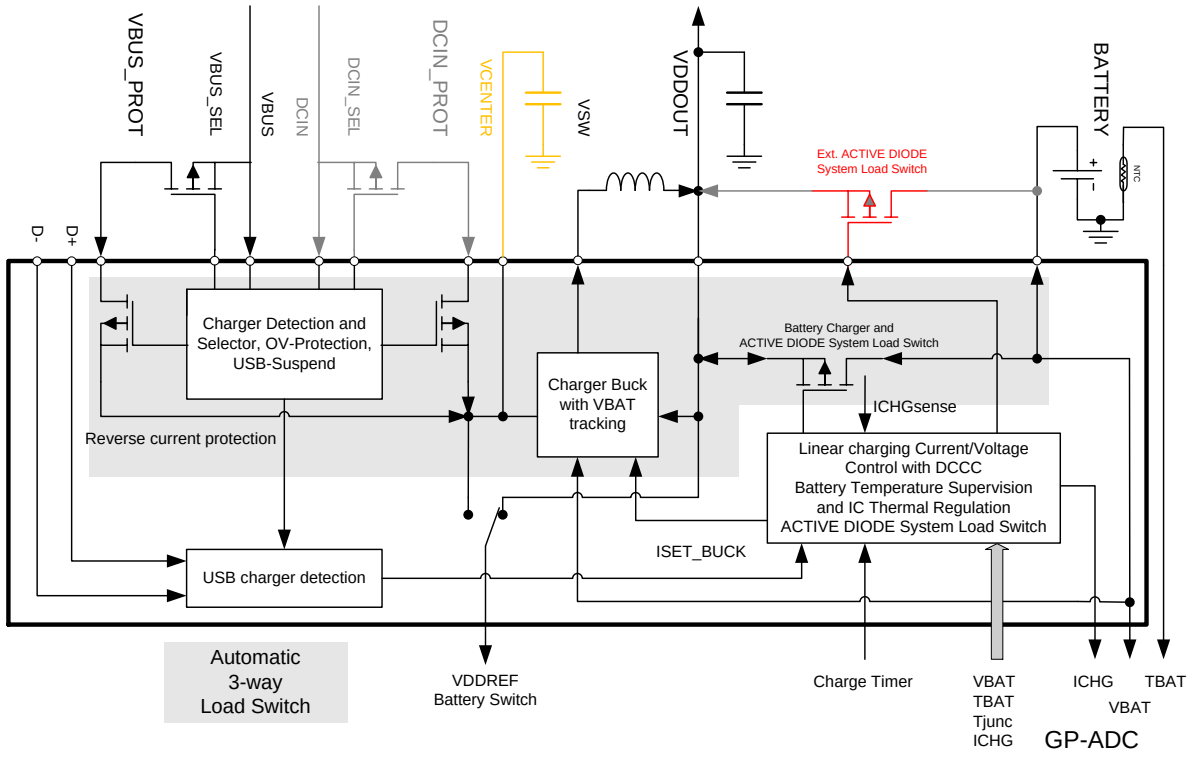


Figure 8: Charger Block Diagram

4.6 Examples of PCB Layout Used in Dialog Reference Boards

The following annotated figures illustrate the key points discussed in this application note.

4.6.1 BGA Package and Charger Buck

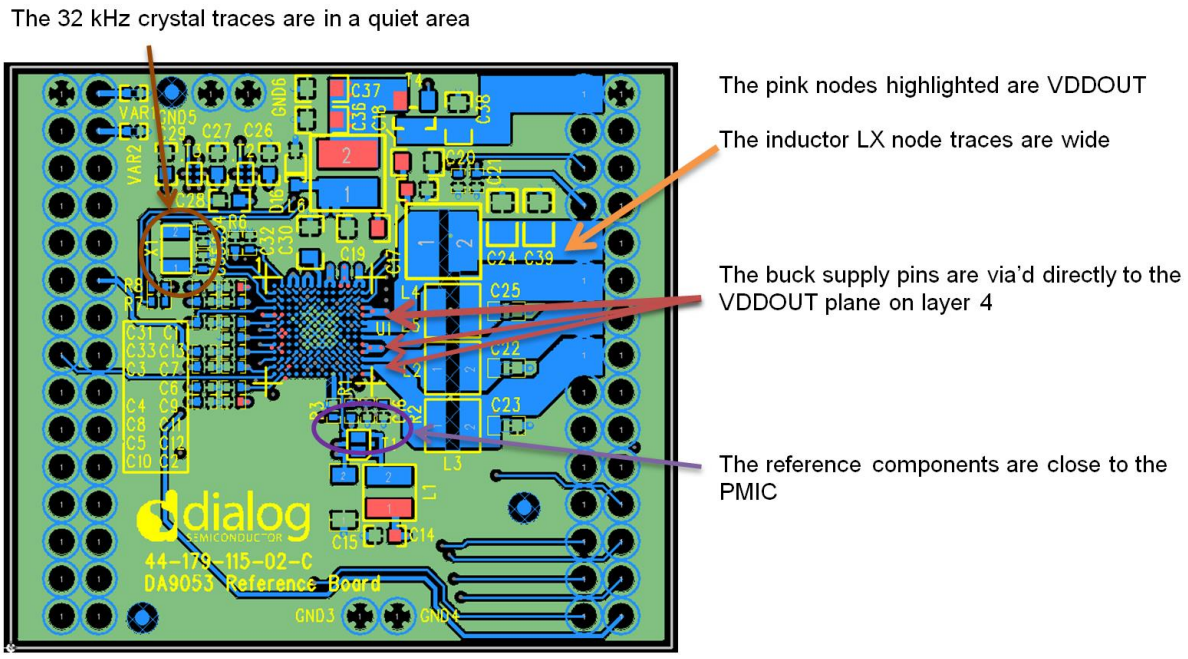


Figure 9: Layer 1 (Top Side)

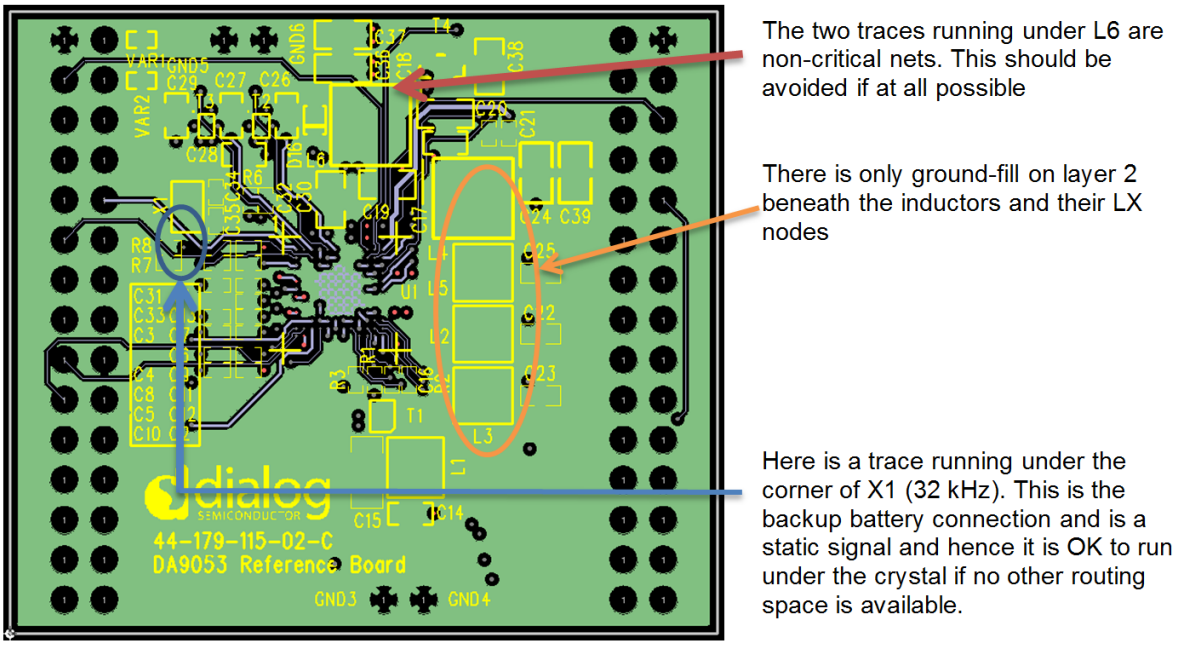
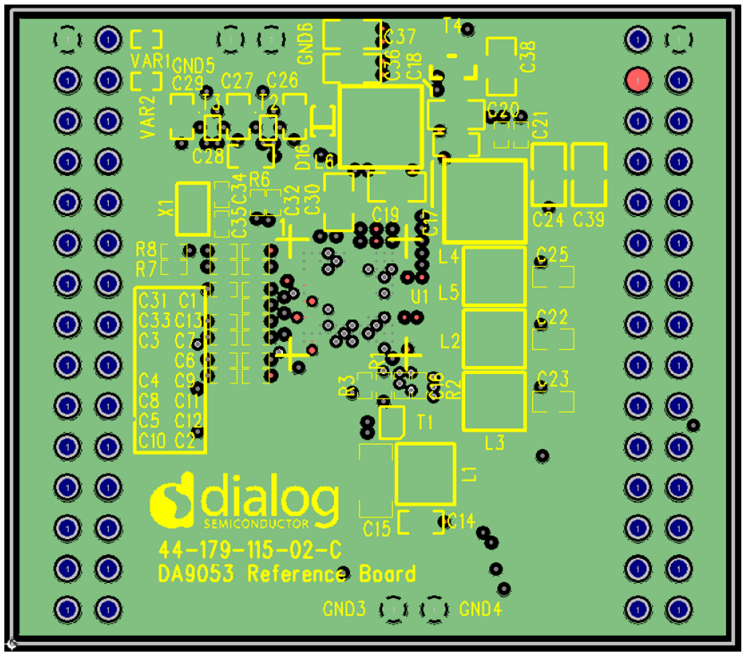
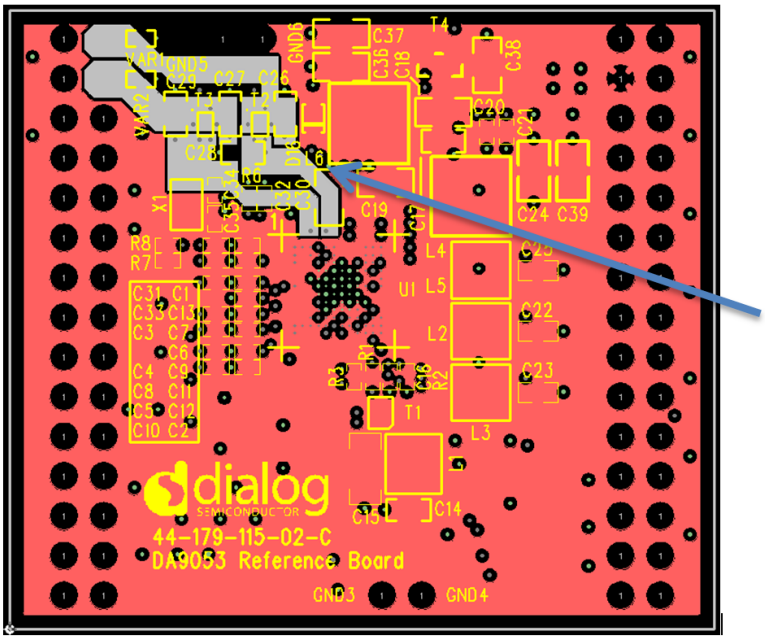


Figure 10: Layer 2



Ground layer with minimum of cut-up by through-hole vias

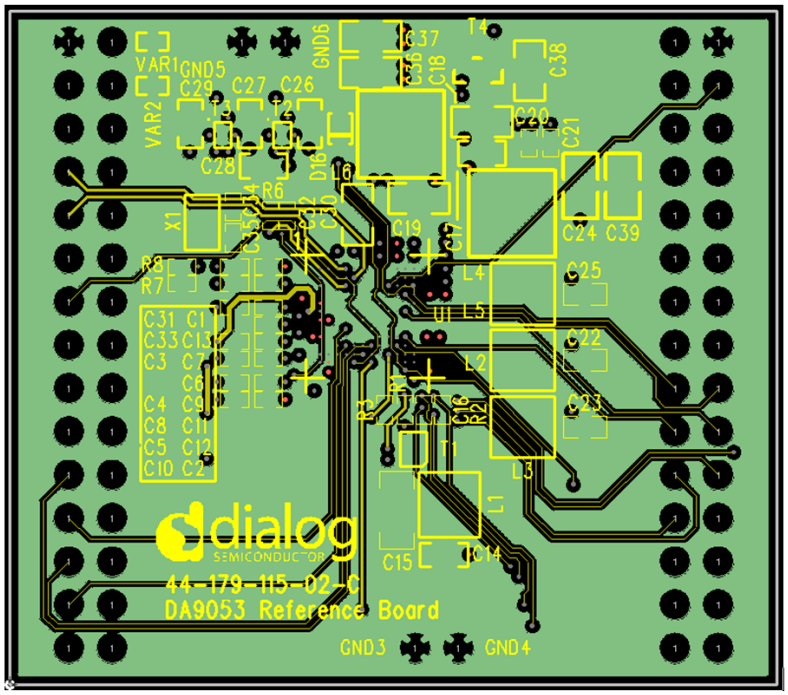
Figure 11: Layer 3



It is important that the power plane is as unbroken as possible. It is valid to have other power plane shapes on this layer as long as they do not interfere with the current flow path of main supply.

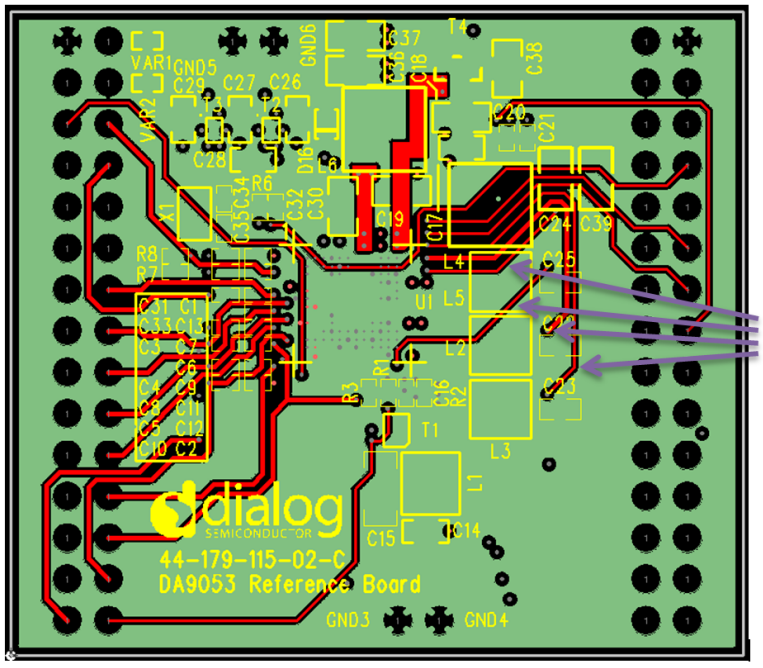
In this example, DCIN and VBUS (grey) are created as wide plane shapes. This minimises losses in the charger system.

Figure 12: Layer 4



This layer can be used as a general routing layer. Dialog has used ground-fill, although it is not specifically required for shielding purposes on this board.

Figure 13: Layer 5



This bottom layer is a general routing layer. The buck feedback traces have also been routed on this layer. It is important to keep them away from noise sources. The absolute length of these traces is not important as they are high impedance nodes, but they are very sensitive to noise. (Noise on these feedback traces can cause increased ripple on the output of the buck.) The arrows point to the four feedback traces.

Figure 14: Layer 6 (Bottom Side)

4.6.2 QFN with Quiet Ground Island

As explained in section 4.4 above, it is important to provide a quiet ground for the references. Figure 15 shows an example of a six-layer board for a PMIC in a QFN package (DA9062) where the crystal, IREF and VREF use a quite ground ‘island’ on Layer 5. The island is connected to the quiet ground on the PMIC (the VSS_ANA pin on the DA9062). Only a thin trace forms a bridge from the island to the main ground. This connection is required to ensure the ground equipotential and must not be omitted. This layout technique avoids large ground currents, especially those associated with buck switching, passing across the quiet ground area. Additionally, the other PCB layers either between or adjacent to layers 1 and 5 do not have traces that carry large switching currents in this area as significant inductive or capacitive coupling might disturb the quiet ground island or the associated sensitive signals.

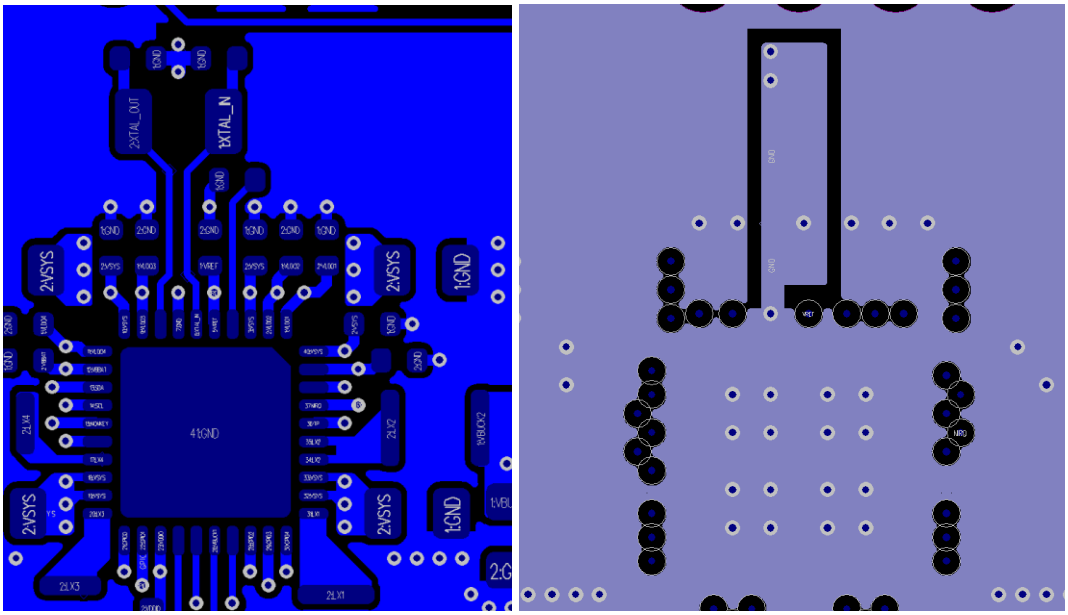


Figure 15: Layer 1 (Top) and Layer 5 (Ground)

5 Conclusions

The PCB layout for integrated power management ICs requires careful consideration if an optimised system is to be achieved. Practical guidelines have been presented together with example layouts of Dialog’s own reference boards.

Appendix A Layout Checklist

The following is a summary of common problems with a PMIC PCB layout and therefore can be used as a checklist for layouters and designers. It is not to be considered an exhaustive list. The pin names are examples only and may vary across products.

1. BUCK GROUND CONNECTIONS (BUCK_VSS)
    a. Solid (short and wide traces with plenty of vias); connection to ground plane
    b. Ideally not shared between multiple bucks
    c. Ideally not shared with the quiet analog ground (VSS_BUCK) for the buck converters
    d. Not coupled (capacitively or inductively) to sensitive analog signals

2. BUCK INPUT CAPACITORS GROUND CONNECTIONS
    a. Solid (short and wide traces with plenty of vias) connection to ground plane
    b. Ideally not shared with the quiet analog ground (VSS_BUCKs) for the buck converters
    c. Not coupled (capacitively or inductively) to sensitive analog signals

3. BUCK OUTPUT CAPACITORS GROUND CONNECTIONS
    a. Solid (short and wide traces with plenty of vias) connection to ground plane
    b. Ideally not shared between multiple bucks
    c. Not shared with the quiet analog ground (VSS_BUCKs) for the buck converters
    d. Not coupled (capacitively or inductively) to sensitive analog signals

4. BUCK SUPPLY CONNECTIONS (BUCK_VDD)
    a. Solid (short and wide traces with plenty of vias) connection to ground plane
    b. Traces to bypass capacitors ideally not shared between multiple bucks
    c. Not shared with any quiet analog power rail
    d. Not coupled (capacitively or inductively) to sensitive analog signals

5. BUCK SWITCHING NODE CONNECTIONS (BUCK_SW, LX)
    a. Solid (short and wide traces with plenty of vias) connection to inductor
    b. Not coupled (capacitively or inductively) to sensitive analog signals

6. BUCK FEEDBACK CONNECTIONS (VBUCK)
    a. Kelvin connection (non-current-sharing) to buck output
    b. Ideally thin, short and quiet trace routed on a lower (buried) layer or shielded from every possible aggressor and in particular the signals listed in 6.c
    c. Not coupled (capacitively or inductively) to any noisy signal and particularly to the LX / BUCK_SW, BUCK_VDD or BUCK_VSS traces

7. DIFFERENTIAL BUCK SENSE CONNECTION (VSS_SENSE, VBUCKCORE2)

a. Dedicated Kelvin connection (non-current-sharing) to output capacitor ground terminal
b. Ideally thin, short and quiet traces routed on a lower (buried) layer or shielded from every possible aggressor and in particular the signals listed in 7.c
c. Not coupled (capacitively or inductively) to any noisy signal and particularly to the LX / BUCK_SW, BUCK_VDD or BUCK_VSS traces

8. BUCK BYPASS SWITCH CONNECTION (VBUCK)
    a. Solid (short and wide traces with plenty of vias) connection to output capacitor pad (buck output)
    b. Not shared with the feedback sense connection

9. LDO OUTPUT SWITCH CONNECTIONS (VLDO)
    a. Adequate trace width to match the specified I_{MAX}

10. LDO SUPPLY CONNECTIONS (VDD_LDO, VDDCORE, VCORE)
    a. Solid (short and wide traces with plenty of vias) connection to power plane
    b. Adequate trace width to match the specified total I_{MAX} per VDD_LDO pin
    c. Ideally not shared between multiple VDD_LDO pins
    d. Not shared with the switching BUCK_VDD traces

11. LDO GROUND CONNECTIONS (VSS_LDO)
    a. Solid (short and wide traces with plenty of vias) connection to ground plane
    b. Adequate trace width for specified I_{MAX}
    c. Ideally not shared with the quiet analog ground

12. SENSITIVE REFERENCE CONNECTIONS (VREF, IREF)
    a. Thin, short and quiet traces routed on a lower (buried) layer or shielded from every possible aggressor (Clocked digital, switched analog, noisy supply rail, and so on)

13. SENSITIVE ADC INPUT CONNECTIONS (VBAT_S, ADC_IN)
    a. Thin and quiet traces routed on a lower (buried) layer or shielded from every possible aggressor (Clocked digital, switched analog, noisy supply rail, and so on)
    b. Not coupled (capacitively) to any reference signals
    c. Not coupled (capacitively) to any other ADC input

14. SENSITIVE CRYSTAL CONNECTIONS (XIN, XOUT)
    a. Thin and quiet traces routed on a lower (buried) layer or shielded from every possible aggressor (Clocked digital, switched analog, noisy supply rail, and so on)
    b. Not coupled (capacitively) to any reference signals
    c. Not coupled (capacitively) to any other ADC input

15. SENSITIVE ANALOG GROUND CONNECTION (VSS_ANA)
    a. Not shared with any buck switching ground or I/O ground
    b. Ideally not shared with any LDO ground

16. SENSITIVE ANALOG SUPPLY CONNECTION (VSYS, VBAT, VDDQ)
    a. Solid (short traces with plenty of vias) connection to power plane
    b. Trace to pin not shared with any buck switching supply
    c. Trace between bypass capacitor and pin ideally not shared with any LDO supply

17. NOISY DIGITAL SIGNAL CONNECTIONS (OUT_32K, SCL, SDA)
    a. Not coupled (capacitively) to any LDO or buck outputs
    b. Not coupled (capacitively) to any buck feedback or sense inputs
    c. Not coupled (capacitively) to any reference signals
    d. Not coupled (capacitively) to any ADC inputs

Revision History

Revision	Date	Description
1.32	16-Feb-2022	File was rebranded with new logo, copyright and disclaimer
1.31	13-Oct-2015	Corrected spelling and grammar.
1.3	20-Jul-2015	Additional layout examples presented. Note added regarding charger VCENTER layout. Checklist added.
1.2	25-Mar-2014	Minor revisions to text and figures.

Status Definitions

Status	Definition
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APPROVED or unmarked	The content of this document has been approved for publication.

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