
Information

This application note provides measurement results of power consumption of RZ/Five in some use cases.

Target Device

RZ/Five

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1. Power Rail Overview

The RZ/Five has several power supply domains; 1.1V, 1.8V, 1.2V and 3.3V. A power system example with a power management IC, PMIC, is depicted in the following figure. The 1.1V power supply to the core logic of this SoC is aggregated to the VDD. Thus, Current flow on the VDD changes along with computationally demands. Current flows on other power rails also change along with each function demands.

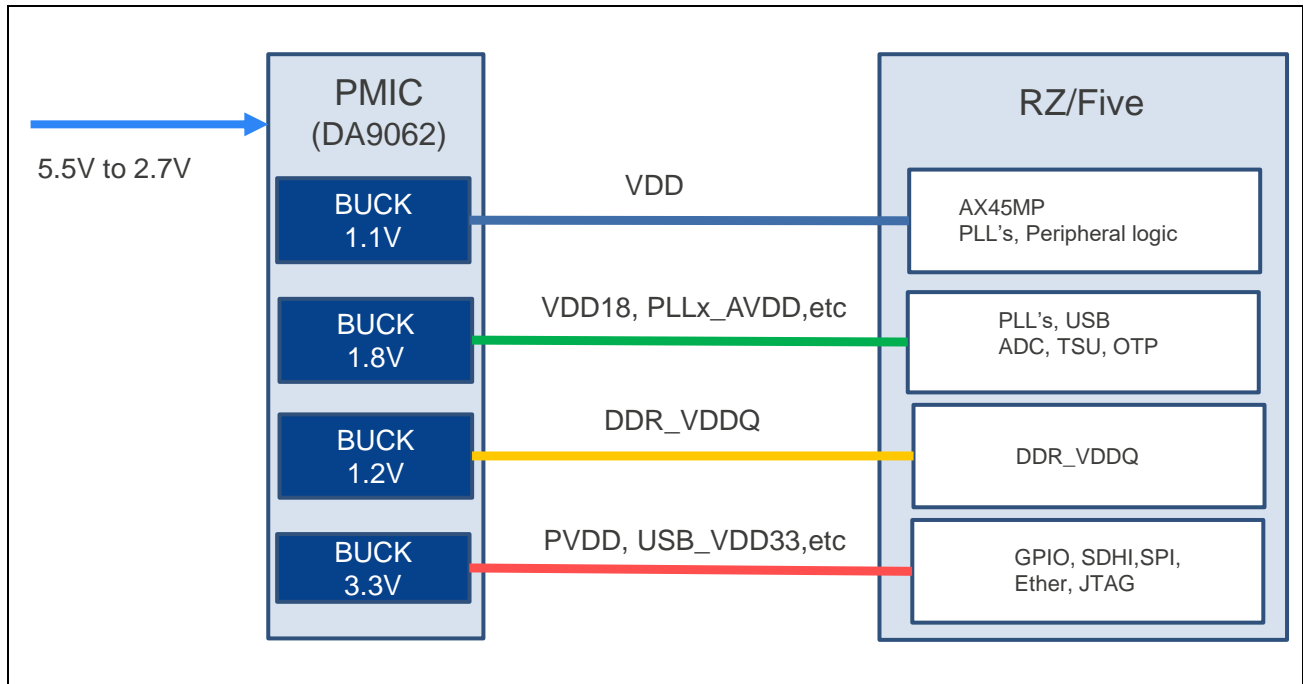


Figure 1.1 A power system example

2. Measurement Condition

- Device condition
 - Process TYP
 - VDD TYP
 - Temperature Room ($T_a \approx 25^\circ\text{C}$)
- DRAM configuration
 - One package
- Target power rails
 - Power rails for core supplies; 1.1V for VDD and 1.2V for VDDQ of a DRAM.
 - Power rails for 1.8V and 3.3V supply for not only the SoC core logic but other devices. Thus, these two supplies are not suitable for evaluation of SoC's internal power.
- Use cases
 - Linux Idle
 - IoT Edge Demo
 - 1-Core Dhrystone

3. Measurement Results

This chapter provides measurement results of power consumption in three use cases;

- Linux Idle
- IoT Edge Demo
- 1-Core Dhrystone

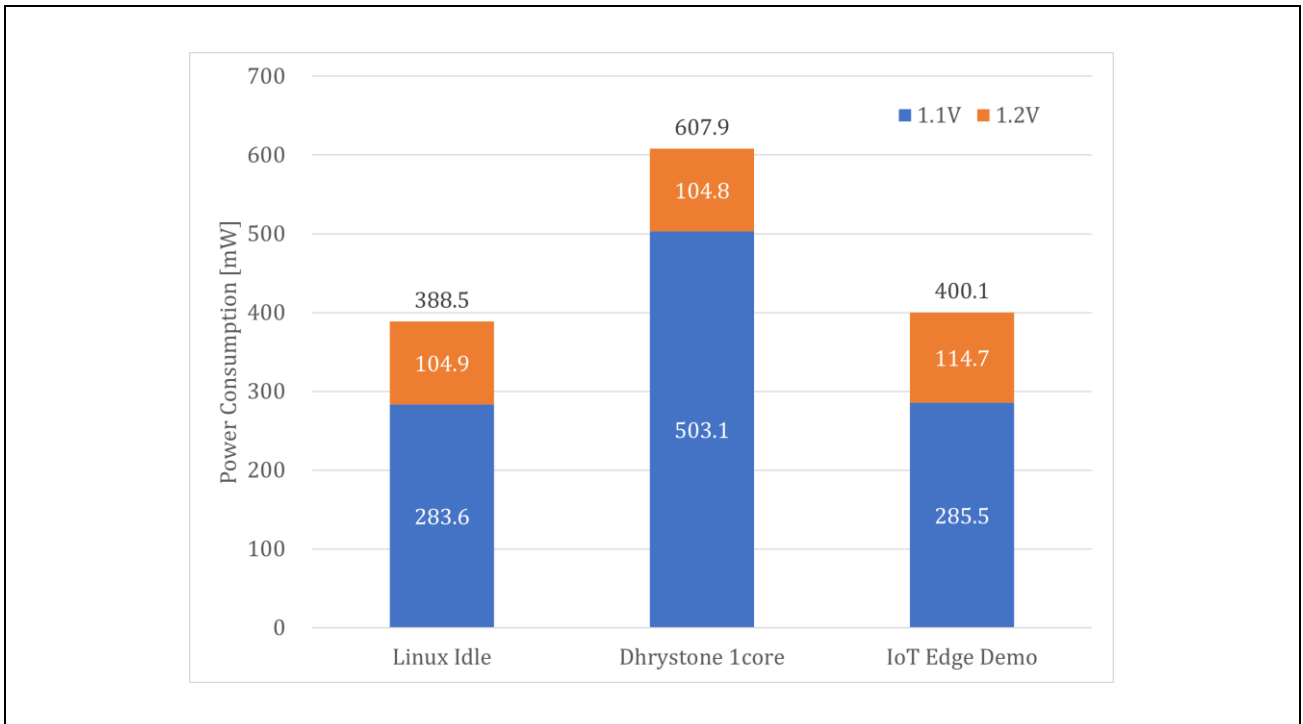


Figure 3.1 Power Consumption in Each Use Case

3.1 Linux Idle

In this use case, “Linux” is set up and no tasks are running on CPU cores with 1.0GHz clock.

Table 3.1 Measurement result in Linux Idle

Power Rail	Voltage [V]	Current [mA]	Power [mW]
VDD	1.1	257.2	283.6
VDDQ for DDR	1.2	87.4	104.9
Total Power	—	—	388.5

3.2 IoT Edge Demo

In this use case, “IoT Edge Demo” is executed on both two CPU cores with 1.0GHz clock.

Table 3.2 Measurement result in IoT Edge Demo

Power Rail	Voltage [V]	Current [mA]	Power [mW]
VDD	1.1	258.9	285.5
VDDQ for DDR	1.2	95.6	114.7
Total Power	—	—	400.1

3.3 1-Core Dhrystone

In this use case, “Dhrystone”, well-known CPU benchmark program, is executed on one core with 1.0GHz clock.

Table 3.3 Measurement result in 1-core Dhrystone

Power Rail	Voltage [V]	Current [mA]	Power [mW]
VDD	1.1	456.6	503.1
VDDQ for DDR	1.2	87.2	104.8
Total Power	—	—	607.9

REVISION HISTORY	RZ/Five Power Consumption Measurement
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Rev.	Date	Description	
		Page	Summary
1.00	Sep 28, 2022	—	First edition issued
1.10	Jan 24, 2023	4, 5	Linux Idle and IoT Edge Demo, added to the description of the use cases
		5	Figure 3.1, added
		6	Section 3.1, added
		7	Section 3.2, added
		8	The power value in Table 3.3, modified

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

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