MOSFET, IGBT, FRD

Power Device Bare Die/Wafer Products Handling Precautions

Introduction

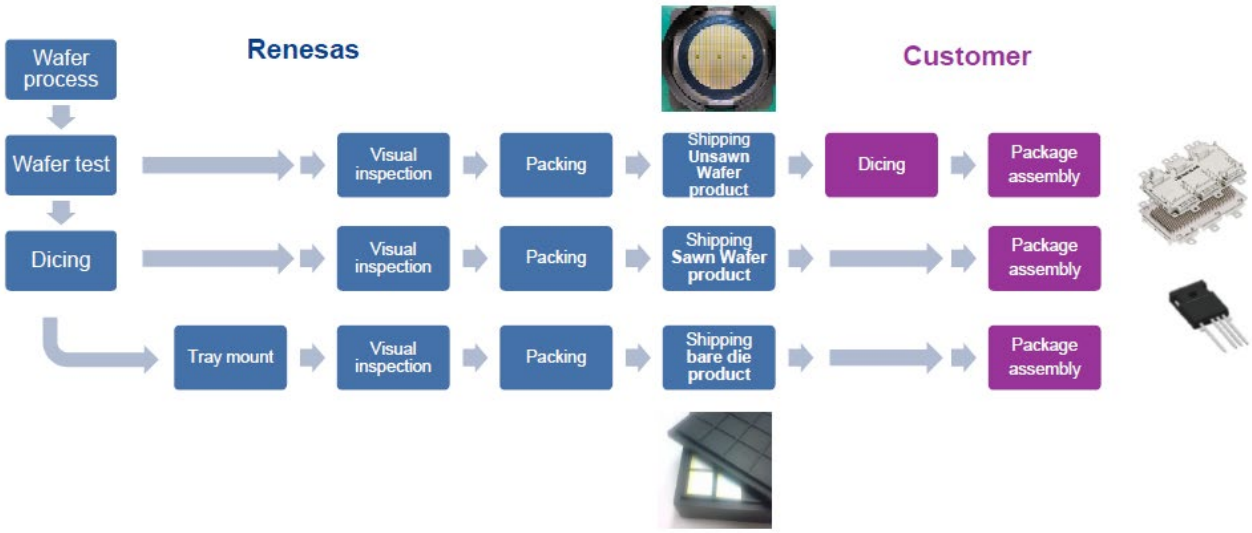
Renesas power device products are provided as bare dies and wafers. As they are semi-finished products, various handling precautions apply. This application note serves as a guide.

Contents

1. Bare Die Product Overview

1.1 Bare Chip Product Overview

Wafer and bare die products are shipped in wafer state or diced (individualized) chip state, per customer request, to enable chip mounting on a board by the customer. Renesas ships wafer products to customers in unsawn wafer form after undergoing the wafer process and probe inspection process (electrical characteristics testing); sawn wafer products following dicing with the actual wafer attached to dicing tape; and chip products shipped in trays.



1.2 Bare Chip Product Structure

The following figure shows an image of the general structure of a Renesas bare chip product.

In power devices, current flows vertically from the back side to the top side of the chip, so both the back and front sides serve as electrodes.

In the IGBT example below, the top side has openings for a gate pad and emitter pads, and the entire back side is the collector electrode. The customer is responsible for die bonding the chip and wire bonding connections from each pad to the external terminals.

- Active cells are formed in the Si under the emitter pads. Care must be taken when bonding to ensure the active cells are not damaged due to stress or other factors. Careful bonding is required to avoid active cell damage from stress.
- Internal wiring and pressure-resistant structure (chip periphery) are formed under the protective film. Careful handling is required as this film is not intended to protect against external physical stress.

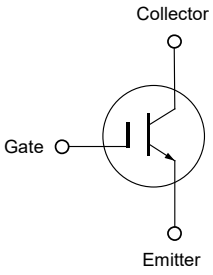


Figure 1 Chip equivalent circuit

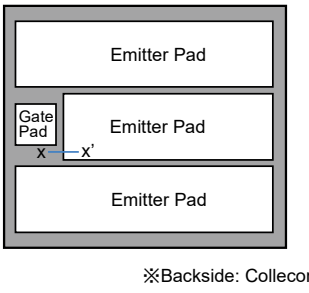


Figure 2 Chip top side

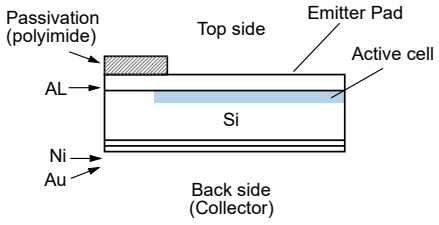


Figure 3 Chip cross-section structure (x-x')

2. Precautions for Bare Die Products

2.1 Introduction

Bare die products are shipped with the chips intact and are easily damaged if mishandled. Pay close attention to the instructions in this section to ensure the quality of bare chip products.

2.2 Bare Die Product Handling

(1) Bare chip products should be opened and mounted in a clean environment in which the wafer surface is not exposed to a contaminated atmosphere or substances. Even in a clean room, exposing bare chip products to a general work environment may cause dust or other unwanted substance to adhere to or damage the die. Caution is required to avoid contamination.

(2) Use a suction-type bare chip collet or vacuum tweezers to pick up bare chip products manually. Since general clamping type tweezers may damage the chip. If tweezers are used, select a plastic version to clamp (grip) the bare die edge, as normal clamp-type tweezers may scratch or otherwise damage the chip.

(3) To avoid scratches, minimize the contact area of tools (such as positioning jigs for mounting) on the bare die side.

2.2.2 Static Electricity

Bare die devices are sensitive to static electricity and must be handled accordingly. Pay careful attention to static electricity generated when unpacking bare chip products or by die bonding equipment, etc. When handling the product, ensure that operators are properly grounded, use neutralization apparatus (such as ionizers), implement thorough grounding and static control measures in the workspace and equipment. We recommended the control level be 100V or lower. Also, handle the chips with care to prevent scratches or damage to the top-side electrodes, protective film, and back-side electrodes. The following are some examples of measures that can be taken to prevent damage to the bare chips.

(1) Work environment

Use conductive sheets or mats on workbenches, chairs, and the work area floor for ground connection. Operators should also use anti-static wrist straps and clothing for grounding.

(2) Equipment and jig support

Make sure all equipment, jigs, etc. are grounded.

(3) Storage environment support

Containers for storing bare chip products, etc., should be made of anti-static semiconductive materials.

3. Bare Die Product Datasheet Contents

The bare die data sheet comprises the following sections:

Features, outlines, mechanical parameters, maximum ratings, electrical characteristics, die dimensions

Information on pad materials and dimensions required for customer mounting will also be provided.

Wafer dimensions will be added for wafer products.

Detailed information regarding maximum ratings and electrical characteristics is limited to package products.

Section 3.1 to 3.9 explains the content provided above.

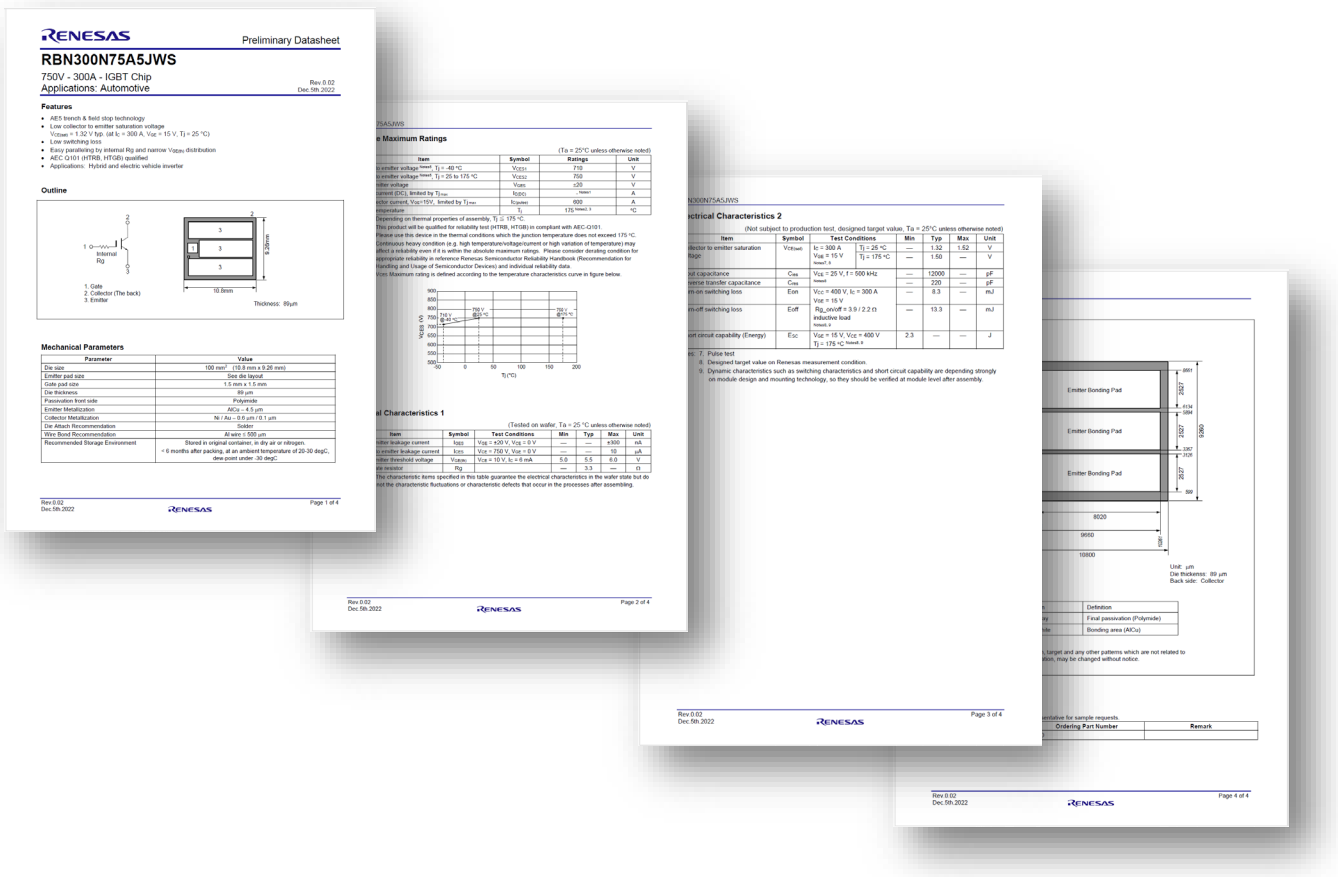
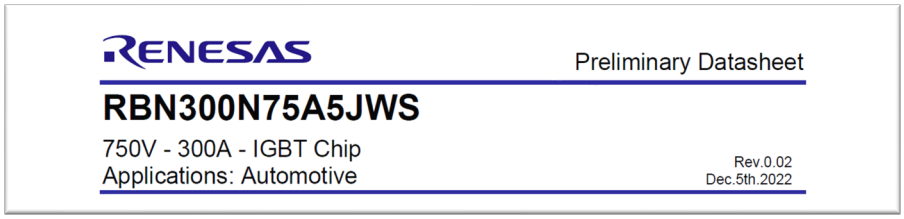


Figure 4 IGBT bare die product configuration example

3.1 Part Number

Bare die can be identified by the package code indicated by the last two digits of the part number.



- Ex. Part No.

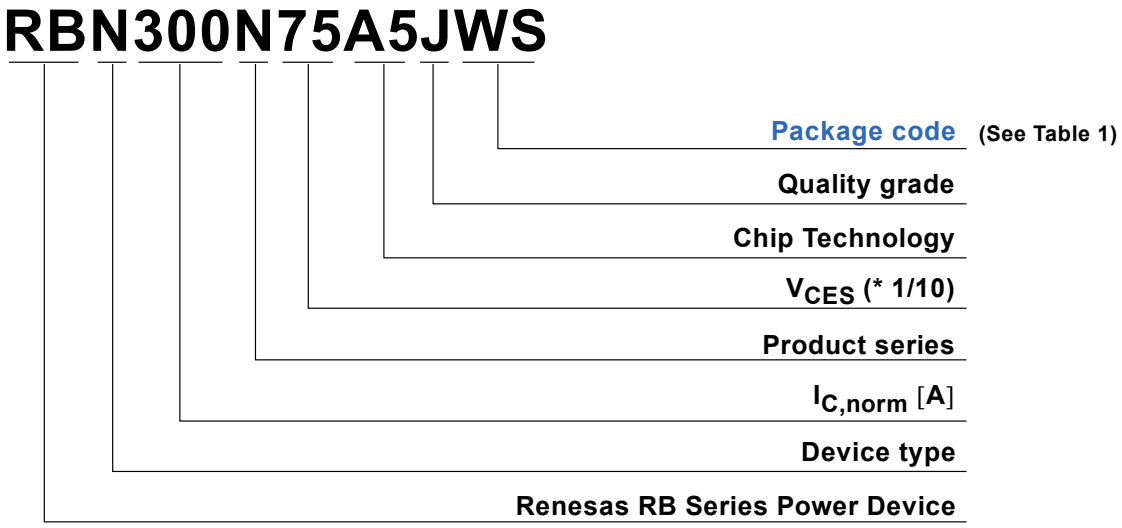
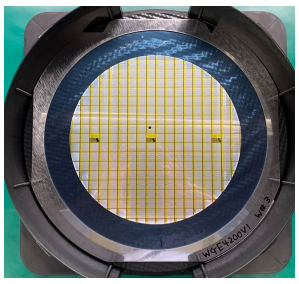


Table 1 Package Code

Package code	Delivery form
WA	Wafer (unsawn)
WS	Wafer (sawn)
WT	Chip

Sawn wafer



Chip
(ex. Mounted on tray)

Figure 5 Packing example

3.2 Features

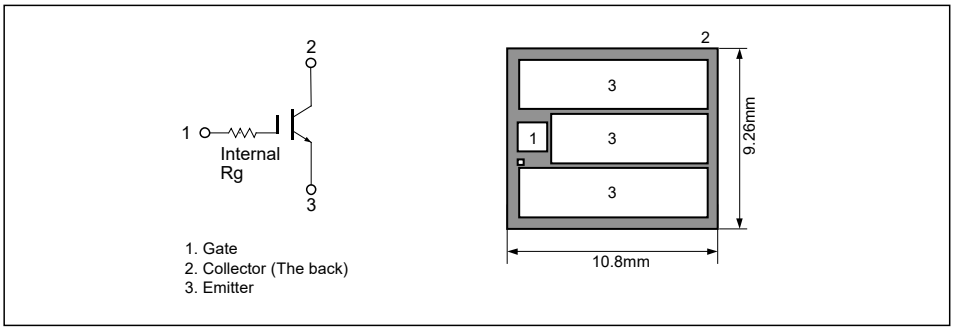
It describes the product's distinctive functions, structure, characteristics, compliant standards, recommended uses, etc.

Features

- 750V trench & field stop AE5 technology
- Low collector to emitter saturation voltage
  $V_{CE(sat)}$ = 1.35 V typ. (at I_C = 300 A, V_{GE} = 15 V, Tj = 25 °C)
- Low switching loss
- Easy paralleling by internal Rg and narrow $V_{GE(th)}$ distribution
- AEC Q101 (HTRB, HTGB) qualified
- Applications: Hybrid and electric vehicle inverter

3.3 Outline

Outline



The equivalent circuit, die size and pad layout (image) of the product.
For this IGBT example, the gate and emitter pads are located on the chip top side.
The entire back side of the chip is a collector electrode.

3.4 Mechanical Parameters

Mechanical Parameters

Parameter	Value
Die size	100 mm^2 (10.8 mm x 9.26 mm)
Emitter pad size	See Die Dimension
Gate pad size	1.5 mm x 1.5 mm

The above table shows the die size and pad size.
For more details, refer to the Die Dimensions section on the data sheet.
When designing, determine wire diameter and bonding layout according to pad size and layout.

Wafer size	300 mm
Maximum possible chips per wafer	Xxx pcs

The above table indicates wafer diameter and maximum possible chips per wafer for either unsawn wafer products or sawn wafer products.

- Wafer size is usually 150mm (6 inch), 200mm (8 inch), or 300mm (12 inch).
  Actual wafers may be slightly smaller than the indicated size. For thin wafer products, the outer periphery is trimmed during the manufacturing process.
- The maximum possible chips per wafer is the number of chips assuming 100% of the chips on the wafers are good. The actual quantity shipped will be smaller than indicated here as a certain number of defective chips are screened out during shipment inspections.

Die thickness	89 μm
Passivation front side	Polyimide
Pad Metallization	AlCu – 4.5 μm
Backside Metallization	Ni / Au – 0.6 μm / 0.1 μm

The above table lists the materials and thickness of each chip layer. Always consider the bonding method and suitable materials for pad metallization.

- Active cells are formed in the Si under the emitter pads. Care must be taken when bonding to ensure the active cells are not damaged due to stress or other factors. Careful bonding is required to avoid active cell damage from stress.
- Internal wiring and pressure-resistant structure (chip periphery) are formed under the protective film. Careful handling is required as this film is not intended to protect against external physical stress.

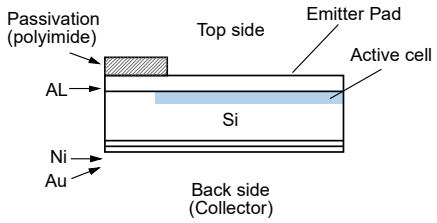
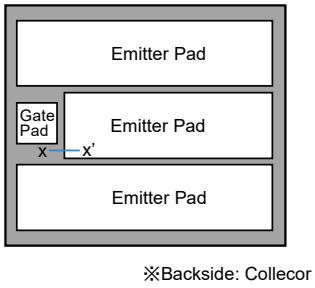


Figure 6 Chip cross-section structure (x-x')



※Backside: Collecor

Figure 7 Chip top side

Die Attach Recommendation	Solder
Wire Bond Recommendation	Al wire ≤ 500 μm

The above table shows the recommended bonding method based on pad metallization. Other methods not listed here can also be used; please contact us for more information.

Recommended Storage Environment	Stored in original container, in dry air or nitrogen. < 12 months after packing, at an ambient temperature of 20 to 30 °C, dew-point under -30 °C

To maintain chip quality, always use the product under the recommended storage conditions and expiration date. Deviations from these conditions may cause defects in package assembly, such as abnormal chip pickup and pad metallization deterioration.

Ink mark for failure die	> ϕ300 μm
Ink mark for failure die	Inkless

For sawn wafer and unsawn wafer products, failure dies detected in Renesas' shipment inspection are shipped on the wafer with the good chips. Each failure die is ink-marked so it can be identified during customer die-mounting and pick-up processes (see figure below). Take care not to use the failure die.
Some products may incorporate “inkless” marking.
In that case, an e-wafer map (*1) data is provided to identify the failure dies.

*1 Coordinate information data for failure die on wafer

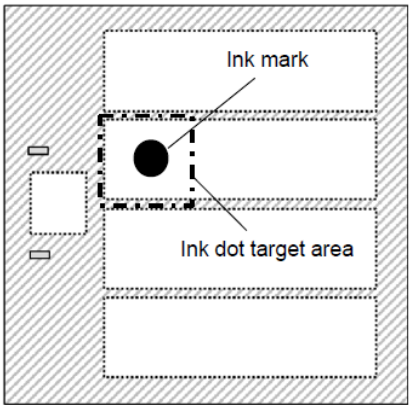


Figure 7 Ink Mark Example

3.5 Absolute Maximum Ratings

Absolute Maximum Ratings

(Ta = 25 °C unless otherwise noted)

Item		Symbol	Ratings	Unit
Collector to emitter voltage	Tj = -40 °C	V_{CES}	710 Notes1, 5	V
	Tj = 25 to 185 °C		750 Notes5	V
Gate to emitter voltage		V_{GES}	±30	V
Collector current (DC)		$I_{C(DC)}$	- Notes2	A
Pulse collector current	V_{GE}=15V, PW limited by Tj	$I_{C(pulse)}$	900 Notes1	A
Junction temperature		T_j	185 Notes3	°C

Notes: 1. Not subject to production test - verified by design/characterization.
2. Depending on thermal properties of assembly, Tj ≦ 185 °C.

The difference between bare die products and packaged products is that bare die products have no provisions for current rating or allowable power dissipation. Both are highly dependent on heat dissipation performance (thermal resistance) at the package level, but heat dissipation performance for the bare die product alone cannot be defined.
Therefore, inspection at the package level must be carried out by the customer.
The current ratings that can be read from the product overview or part number are reference values based on the chip design and are for reference only.

IGBT Application Note (renesas.com)

3.1 Collector current, Collector Dissipation

Figure 3 shows the collector dissipation temperature characteristics of RBN40H125S1FPQ.

The allowable collector dissipation is shown at different case temperatures, and the following equation holds when $T_C = 25℃$ or more.

$$Pc = \frac{(Tjmax - Tc)}{R_{th(j-c)}}$$

If $T_C = 25℃$ or less, collector dissipation is applied by the absolute maximum rating.

Collector current is specified following formula.

$$Ic = \frac{(Tjmax - Tc)}{R_{th(j-c)} \times V_{CE(sat)}}$$

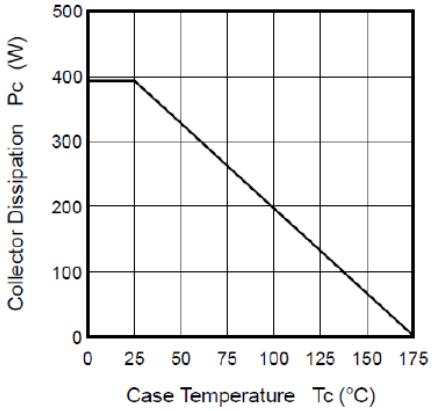


Figure 3. Collector Dissipation vs. Case Temperature

3.6 Electrical Characteristics

Electrical Characteristics 1

(Tested on wafer, Ta = 25 °C unless otherwise noted)

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Gate to emitter leakage current	I_{GES}	V_{GE} = ±30 V, V_{CE} = 0 V	—	—	±300	nA
Collector to emitter leakage current	I_{CES}	V_{CE} = 750 V, V_{GE} = 0 V	—	—	10	μA
Gate to emitter threshold voltage	$V_{GE(th)}$	V_{CE} = 10 V, I_C = 6 mA	5.0	5.5	6.0	V
Collector to emitter saturation voltage	$V_{CE(sat)}$	I_C = 100 A, V_{GE} = 15 V	—	1.00	1.15	V
Internal gate resistor	Rg		—	3.3	—	Ω

Notes: 6. The characteristic items specified in this table guarantee the electrical characteristics in the wafer state but do not the characteristic fluctuations or characteristic defects that occur in the processes after assembling.

Electrical characteristic items tested on dies in the wafer state.
The inspection current is limited to several dozen amperes in wafer-state testing due to probe contacts.
Products with a current rating higher than several dozen amperes cannot be tested or screened at the rated current.
It is therefore necessary to test and screen at the customer's package level.
Testing and screening at the package level must be performed by the customer.

Electrical Characteristics 2

(Not subject to production test, designed target value, Tj = 25 °C unless otherwise noted)

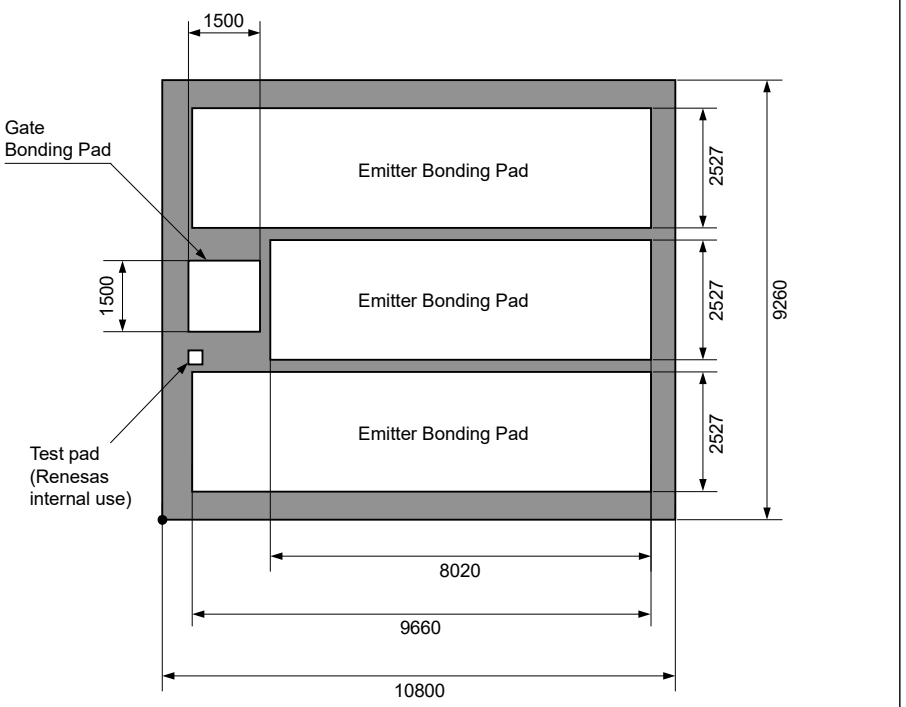
Item	Symbol	Test Conditions		Min	Typ	Max	Unit
Collector to emitter saturation voltage	$V_{CE(sat)}$	I_C = 300 A, V_{GE} = 15 V Notes7	Tj = 25 °C	—	1.35	1.55	V
			Tj = 175 °C	—	1.56	—	V
Input capacitance	C_{ies}	V_{CE} = 25 V, f = 500 kHz Notes7		—	11000	—	pF
Reverse transfer capacitance	C_{res}			—	240	—	pF
Turn-on switching loss	Eon	V_{CC} = 400 V, I_C = 300 A V_{GE} = 15 V Rg_on/off = 3.9 / 2.2 Ω inductive load Notes7, 8		—	9.5	—	mJ
Turn-off switching loss	Eoff			—	12.0	—	mJ
Short circuit capability time	t_{SC}	V_{GE} = 15 V, V_{CE} = 450 V Tj = 175 °C Notes7, 8		3.4	—	—	µs
Short circuit capability energy	E_{SC}			2.2	—	—	J

Notes: 7. Designed target value on Renesas measurement condition.
8. This value is influenced by parasitic inductance and assembly condition.

The above electrical characteristics cannot be tested during wafer testing (shipment inspection). The specifications here are stipulated as target values according to the chip design.
These test items are not guaranteed.
The table mainly lists dynamic characteristic items such as VCE(sat)/ON resistance and switching under high current conditions.
Dynamic characteristics, such as switching, strongly depend on the package design and mounting technology and should be verified by the customer at the package level.
For items that cannot be tested during wafer testing and other characteristics or conditions not specified in the datasheet, we recommend conducting alternative inspections at the customer package level.

3.7 Die Dimensions

Die Dimensions



Unit: μm
Die thickenss: 89 μm
Back side: Collector

Notes 1:

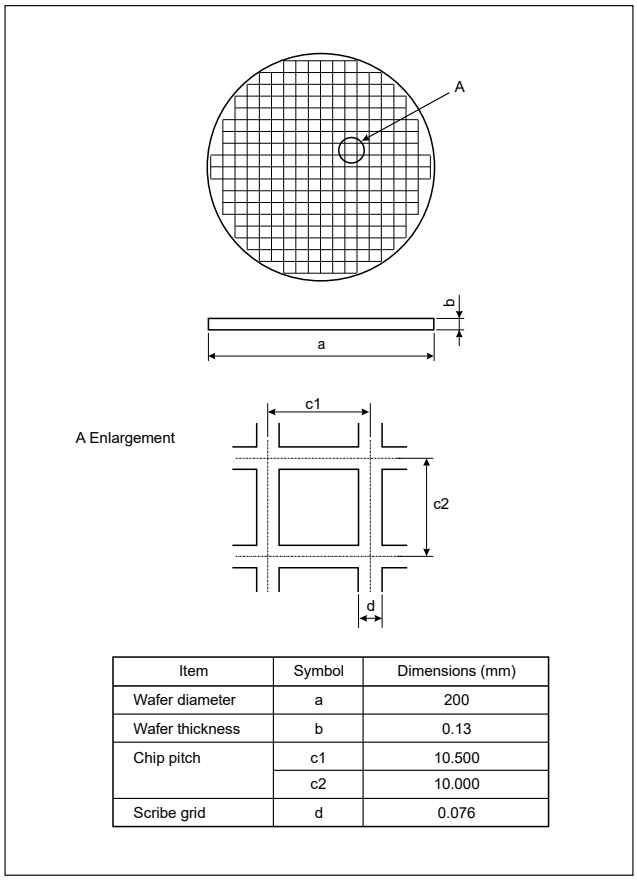
Illustration	Definition
Part of gray	Final passivation (Polymide)
Part of white	Bonding area (AlCu)

Notes 2: Recognition, target and any other patterns which are not related to IGBT operation, may be changed without notice.

The above figure shows detailed chip and pad dimensions.
Use this figure when considering wire diameter or bonding layout for your product.

3.8 Wafer Dimensions

Wafer Dimensions



Item	Symbol	Dimensions (mm)
Wafer diameter	a	200
Wafer thickness	b	0.13
Chip pitch	c1	10.500
	c2	10.000
Scribe grid	d	0.076

This figure shows the external appearance, size, and thickness of the wafer. For unsawn wafers, it also shows the scribe grid value for dicing in the wafer state. The chip size is specified as shown in “A Enlargement” above.

3.9 Ordering Information

Ordering Information

Please contact your Renesas sales representative for sample requests.

Delivery Form	Ordering Part Number	Ordering Quantity Unit
Unsawn wafer	RBN40N65T1UFWA-850#FF0	9900 (5 wafers)
Unsawn wafer	RBN40N65T1UFWA-8F0#FF0	49500 (25 wafers)

Note. The order quantities indicate the maximum quantity of chips for each part number, and the actual quantity of chips shipped will be reduced due to yield. There also a possibility that the number of wafers may decrease during the manufacturing process. The quantity shipped will be indicated on the label as the number of good chips.

The “ordering part number” is a unique number used to order mass-produced product based on delivery form.
For wafer bare die products, the main delivery forms are: Sawn Wafer, Unsawn Wafer, Chip Tray, Tape & Reel.
When ordering a small quantity of samples, please order using the sample product number, not the mass production ordering part number. Feel free to contact us for details.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Oct.22.2024	-	First edition

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
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