RH850/U2B Group

R01AN6916EJ0100
Rev.1.00

Power Supply Voltage Monitor Application Note

Summary

This application note explains the basic usage for the power supply voltage monitor of RH850/U2B.

Aim of this document and software is to provide supplemental information for the function on RH850/U2B. It is not intended to implement in the design for mass production. There is no guarantee to update in this document and software to reflect the latest manual, errata, technical update and development environment. You are fully responsible for the incorporation or any other use of the information of this document in the design of your product or system, and please refer to latest manual, errata, technical update and development environment.

Target Device

- RH850/U2B Group

Target Integrated Development Environment

CS+ (from RENESAS Electronics)

Version : E8.07.00g6

Device File : DR7F702Z21EDBB.DVF

Reference Document

RH850/U2B User's Manual : Hardware

For function details and electrical characteristics, please refer to "User's Manual: Hardware".

This application note is based on the following manual.

・ RH850/U2B User's Manual (Rev.0.80): R01UH0923EJ0080

Items

1. Introduction

This application note describes the usage for the power supply voltage monitor of RH850/U2Bx and the making example for software.

1.1 Use Function

The hardware functions of RH850/U2Bx used in this application note are shown below.

- Power Supply Voltage Monitor
- Clock Monitor
- Reset Controller

2. Function Overview for Power Supply Voltage Monitor

The features of the power supply voltage monitor are shown below.

- The power supply voltage monitor monitors the voltage of E0VCC (hereinafter, it will be referred to as EVCC), VCC, and ISOVDD.
  In the power supply voltage monitor, there are H side (HDET) and L side voltage detection, and it detects whether the monitored voltage is above or below the set voltage.
- In the power supply voltage monitor, there are two detection functions for primally and secondary.
  Primally is detected by the voltage monitor . (VMON)
  Secondly* is detected by SAR-ADC.
- The delay monitor (DMON) supports VMON that detects the L side voltage of ISOVDD.
- The delay monitor (DMON) supports the low level voltage of ISOVDD by the power supply voltage monitor (VMON).
- The primary power supply voltage monitor can set VMON reset on/off when detecting high level of VCC and E0VCC as well as high level and low level of ISOVDD. The low level detection for VCC and E0VCC is constantly occurred VMON reset.
- The primary detection voltage value is settable by fixing. The secondly detection voltage value is settable by SAR-ADC.

2.1 Overview of Voltage Monitor Primary Detection (VMON)

The voltage monitor primary detection (VMON) monitors the voltage of ISOVDD, VCC, and E0VCC. The error of the voltage is notified by the following methods.

- VMON Error Output Pin
- Upper/Lower limit voltage flag of each supplied voltage
- VMON Reset

Figure 2-1 shows the detection voltage. The detection voltage of VMON is fixed.

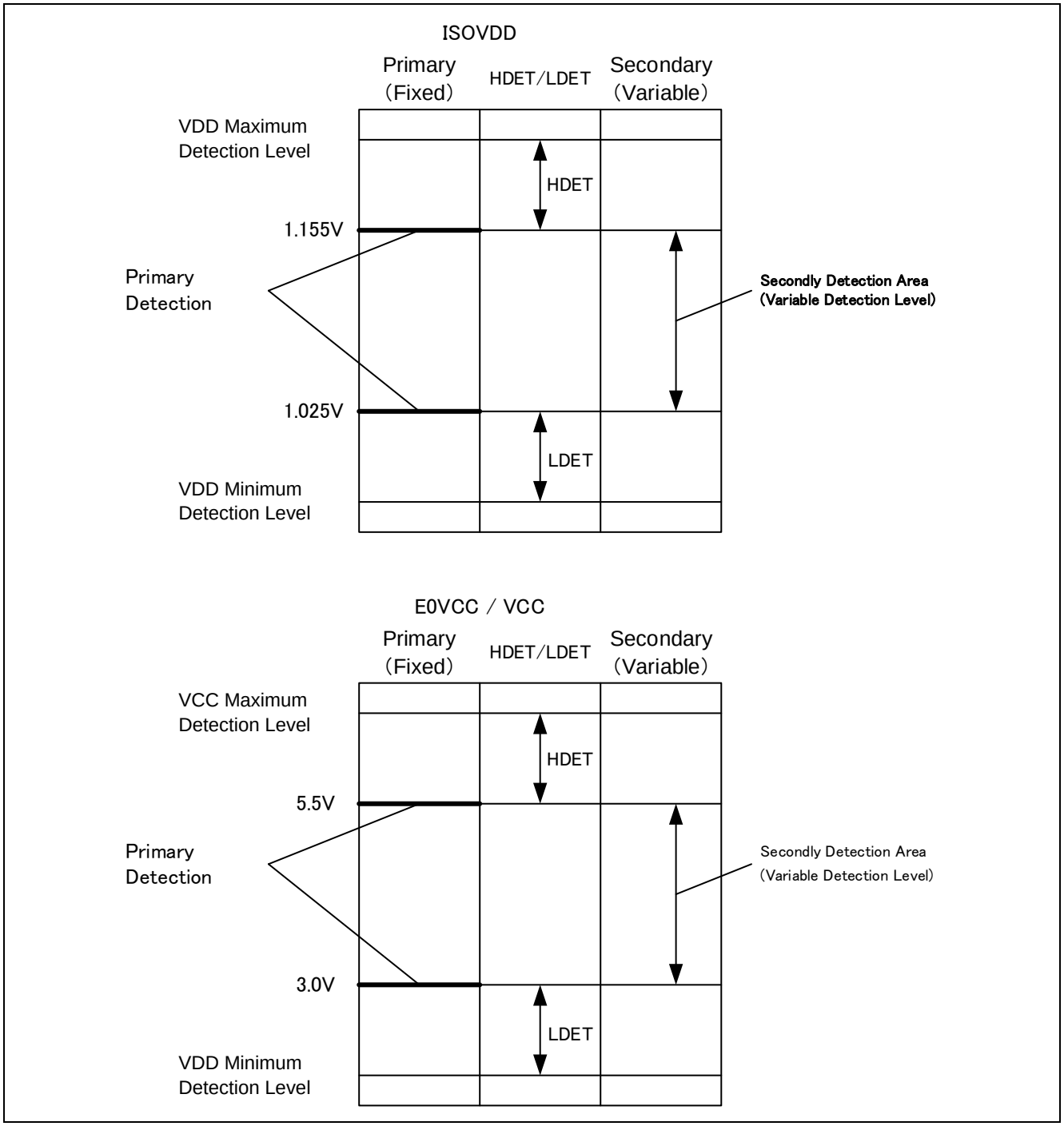

Figure 2-1 Detection Voltage of VMON

2.2 Overview of Delay Monitor (DMON)

The delay monitor (DMON) monitors the delay time depending on ISOVDD supply voltage. When the delay time is lower than the threshold, the delay error is occurred.

When detection the delay error, the error is recorded to DMONF register and notified to VMON.

3. Operation Example for Power Supply Voltage Monitor

3.1 Enable/Disable Setting for Power Supply Voltage Monitor

The enable/disable for the power supply voltage monitor and the setting for the digital filter, etc., are set by the option byte (OPBT4). The setting value is settable by ISOVDDFCR, VCCFCR and E0VCCFCR.

Option Byte (OPBT4)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ISOVDDFLTW [1:0]		ISOVDDCLKSEL[1:0]		ISOVDD FLTEN	—	ISOVD DHDE	ISOVD DLDE	VCCFTW [1:0]		VCCCLKSEL [1:0]		VCCFL TEN	—	VCCHD E	VCCLD E
Value after reset:	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	E0VCCFLTW [1:0]		E0VCCCLKSEL [1:0]		E0VCC FLTEN	—	E0VCC HDE	E0VCC LDE	VDD2FLTW[1:0]		VDD2CLKS EL[1:0]		VD D2FLTE N	DSDET EN	VDD2H DE	VDD2L DE
Value after reset:	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note 1. This value is dependent on the value in the flash memory which is specified by the user.

Figure 3-1 Option Byte (OPBT4)

Table 3-1 Contents of Option Byte (OPBT4)

Bit Position	Bit Name	Function
31, 30	ISOVDDFLTW[1:0]	Minimum filtering width selection of digital noise filter 00 : 20 cycles 01 : 13 cycles 10 : 8 cycles 11 : 3 cycles
29, 28	ISOVDDCLKSEL[1:0]	Clock selection of digital noise filter 00 : CLK_HVIOSC frequency/256 01 : CLK_HVIOSC frequency/128 10 : CLK_HVIOSC frequency/64 11 : CLK_HVIOSC frequency/32
27	ISOVDDFLTEN	Output filter enable of VMONOUT and VMONF 0 : Disable output filter of VMONOUT and VMONF 1 : Enable output filter of VMONOUT and VMONF
26	-	Reserve bit (Set “1” when setting.)
25	ISOVDDHDE	Enable ISOVDD upper limit voltage detection. 0 : Disable ISOVDD upper limit voltage detection. 1 : Enable ISOVDD upper limit voltage detection.
24	ISOVDDLDE	Enable ISOVDD lower limit voltage detection. 0 : Disable ISOVDD lower limit voltage detection. 1 : Enable ISOVDD lower limit voltage detection.

Bit Position	Bit Name	Function
23、22	VCCFLTW[1:0]	Minimum filtering width selection of digital noise filter 00 : 20 cycles 01 : 13 cycles 10 : 8 cycles 11 : 3 cycles
21、20	VCCCLKSEL[1:0]	Clock selection of digital noise filter 00 : CLK_HVIOSC frequency/256 01 : CLK_HVIOSC frequency/128 10 : CLK_HVIOSC frequency/64 11 : CLK_HVIOSC frequency/32
19	VCCFLTEN	Output filter enable of VMONOUT and VMONF 0 : Disable output filter of VMONOUT and VMONF 1 : Enable output filter of VMONOUT and VMONF
18	-	Reserve bit (Set “1” when setting.)
17	VCCHDE	VCC high-voltage detecting activation 0：VCC high-voltage detection disable 1：VCC high-voltage detection enable
16	-	Reserve bit (Set “1” when setting.)
15、14	E0VCCFLTW[1:0]	Minimum filtering width selection of digital noise filter 00 : 20 cycles 01 : 13 cycles 10 : 8 cycles 11 : 3 cycles
13、12	E0VCCCLKSEL[1:0]	Clock selection of digital noise filter 00 : CLK_HVIOSC frequency/256 01 : CLK_HVIOSC frequency/128 10 : CLK_HVIOSC frequency/64 11 : CLK_HVIOSC frequency/32
11	E0VCCFLTEN	Output filter enable of VMONOUT and VMONF 0 : Disable output filter of VMONOUT and VMONF 1 : Enable output filter of VMONOUT and VMONF
10	-	Reserve bit (Set “1” when setting.)
9	E0VCCHDE	E0VCC high-voltage detecting activation 0：E0VCC high-voltage detection disable 1：E0VCC high-voltage detection enable
8～0	-	Reserve bit (Set “1” when setting.)

3.2 Explanation for Operation Example

In this operation example, VMON and DMON are started and the power supply voltage is monitored after self-diagnosis of VMON and DMON.

3.3 Software Explanation

- Module Explanation

The following shows the module list in this operation example.

Table 3-2 Module List

Module Name	Label Name	Function
Main routine	main_pe0	Perform various setting and application startup.
Clock monitor initialization routine	clk_mon_init	Perform initial setting of clock monitor (CLMA0).
VMON diagnosis/startup routine	vmon_diag	Perform self-diagnosis/startup of VMON.
DMON diagnosis/startup routine	dmon_diag	Perform self-diagnosis/startup of DMON.

- Register Setting

The following shows the register setting of various functions in this operation example.

Table 3-3 Register Setting of Voltage Monitor Primary Detection (VMON)

Register Name	Setting Value	Function
VMONKCPROT	0xA5A5A501	Enable writing access to protected register.
	0xA5A5A500	Disable writing access to protected register.
VMONFC	0xFC	Error detection flag clear of VMON source register (VMONF)
VMONDIAGFE	0x00	Set output filter disable when self-diagnosis of VMON is enabled.
	0x0E	Set output filter enable when self-diagnosis of VMON is enabled.
VMONDMASK	0xEE	Mask VMON_ERROROUT and VMON reset when self-diagnosis of VMON is enabled.
VMONDIAG	0xFC	Set to detection level change when self-diagnosis of VMON is enabled. (error injection)
	0x00	Set to normal monitoring when self-diagnosis of VMON is enabled.
ISOVDDDE *1	0xEB	Enable VMON reset by ISOVDD upper/lower limit voltage detection.
VCCDE *2	0xAA	Enable VMON reset by VCC high-voltage detection.
E0VCCDE *2	0xAA	Enable VMON reset by E0VCC high-voltage detection.
VMONDIAGMEW	0x01	Set “disable” to diagnosis function of VMON.

*1 : Bit 3, 1, and 0 are set by the option byte (OPBT4) when either standby reset or external reset is released.

*2 : Bit 3 and 1 are set by the option byte (OPBT4) when either standby reset or external reset is released.

Table 3-4 Register Setting for Delay Monitor (DMON)

Register Name	Setting value	Function
DMONKCPROT0	0xA5A5A501	Enable writing access for protected register.
	0xA5A5A500	Disable writing access for protected register.
DMONFC	0x00000001	Error detection flag clear of DMON source register (DMONF)
DMONFCR	0x00000007	Set 128 sampling time to the minimum filtering width.
DMONDE	0x00000009	Set DMON_REQRESET disable, output filter enable of DMON error detection flag, and DEMON lower-limit delay detection enable.
	0x000000A9	Set DMON_REQRESET enable, output filter enable of DMON error detection flag, and DEMON lower-limit delay detection enable.
DMONDIAG	0x00000001	Error injection
	0x00000000	Set DMON normal operation.
DMONDIAGMEW	0x00000001	Set “disable” to diagnosis function of DMON.

Table 3-5 Clock Monitor Register Setting

Register Name	Setting value	Function
CLMAKCPROT	0xA5A5A501	Enable writing access for protected register.
	0xA5A5A500	Disable writing access for protected register.
CLMA0CMPL	0x025F	CLMA0 lower-limit threshold
CLMA0CMPH	0x02A4	CLMA0 upper-limit threshold
CLMA0CTL	0x01	CLMA0 operation enable

Table 3-6 Reset Controller Register

Register Name	Setting value	Function
RESFC	0x000005BF	Reset flag clear of reset source register (RESF)

- Operation Flow

The following shows the flowchart in this operation example.

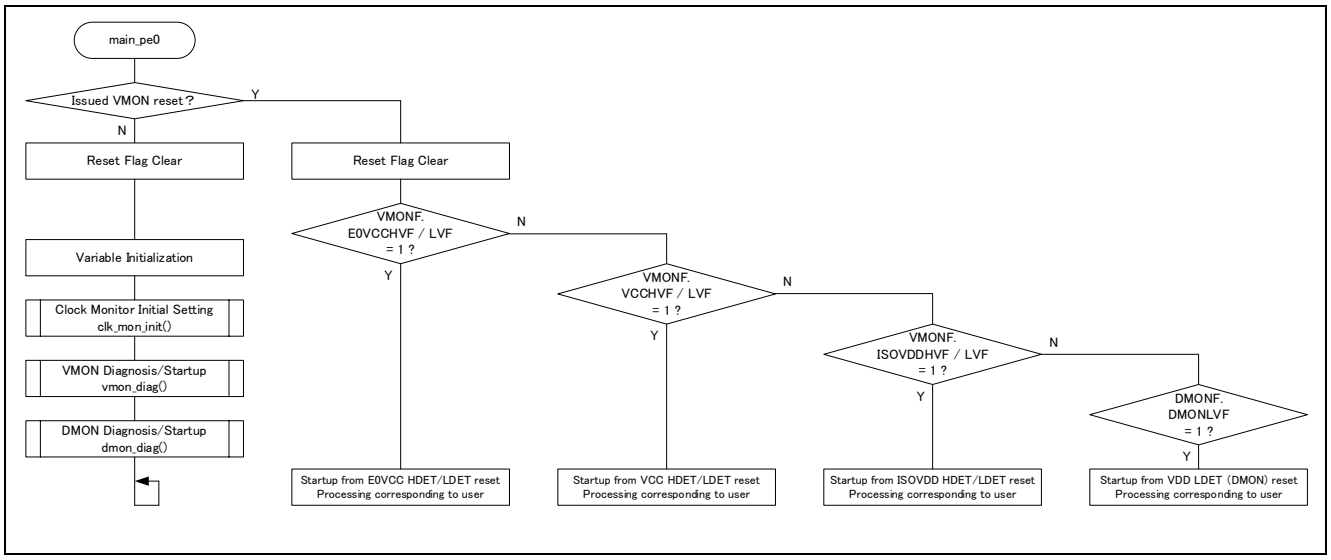

Figure 3-2 Flowchart

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2024.3.8	—	Initial edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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