Application Note

Power Sub-System Design Using The PV88090

AN-PV-007

Abstract

This application note illustrates PMIC power supply design using the PV88090 .

Contents

1 Terms and Definitions

CPU	Central processing unit
DDR	Dual data rate memory
DVC	Dynamic voltage control
FET	Field effect transistor
I/O	Input/output
NMOS	N-type metal oxide semiconductor
PFM	Pulse frequency modulation
PMIC	Power management integrated circuit
PMOS	P-type metal oxide semiconductor
PMU	Power management unit
QFN	Quad flat (package) – no leads
RMS	Root mean squared
VDS	Voltage drain to source

2 Introduction

PV88090 is a power management unit (PMU) optimized for supplying systems with central processing units (CPU), input/output (I/O), and dual data rate (DDR) memory. The target application range covers television, set-up box, wifi routers, and enterprise access point and network addressable servers.

PV88090 features a two-phase buck converter providing up to 9.5 A current, and two one-phase buck converters for dual data rate (DDR) memory and auxiliary power. High efficiency is achieved over a wide load range by using automatic pulse frequency modulation (PFM). All power switches are integrated, eliminating the need for external Schottky diodes. This optimizes power efficiency and reduces the external component count. Two LDO regulators with programmable output voltage are integrated and provide up to 400 mA. PV88090 provides dynamic voltage control (DVC) via I^2C command to support adaptive adjustment of the supply voltage based on the processor loading. All power blocks have over-current circuit protection and the start-up timing can be controlled through the I^2C interface. The supply voltages of PV88090 can be controlled with direct register writes through the I^2C interface to the operating point of the system.

PV88090 includes over-temperature and over-current protection for increased system reliability, without external sensing components. A soft-start mechanism limits the inrush current from the input node and secures a slope-controlled rail activation. A standby mode provides reduced power consumption. Optional standby operation for DDR memory, auxiliary buck, and analog core LDO are configurable in OTP for optimizing the power rails. The PV88090 is available in a 30-pin QFN package and is specified from -40 °C to 85 °C ambient temperature.

3 Design Example

PV88090 provides three adjustable synchronous buck regulators (Buck1, Buck2, Buck3) and two LDO regulators. This example describes the design process for the following:

- Buck1 regulating a 1 V output at a 9.5 A load current
- Buck2 regulating a 1.2 V output at a 2 A load current
- Buck3 regulating a 1.5 V output at a 2 A load current

Table 1: PV88090 Design Example Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Buck1						
Input voltage	V_{DD}		4.75		5.25	V
Output voltage	V_{BUCK1}	$I_{OUT} = I_{MAX}$ Step = 6.25 mV	0.9		1.3	V
Output voltage accuracy	V_{BUCK1_ACC}	V_{OUT} = 1 V $I_{OUT} = ½I_{MAX}$	-3		3	%
Output voltage ripple	V_{BUCK1_RIPPLE}	$I_{OUT} = I_{MAX}$			30	mVpp
Load regulation transient	V_{TR_LOAD}	$I_{OUT} = ¼I_{MAX}$ to I_{MAX} $t_r = t_f$ = 25 µs V_{OUT} = 1 V L = 1.5 µH		25		mV
Line regulation transient	V_{TR_LINE}	V_{DD} = 4.75 V to 5.25 V $t_r = t_f$ = 10 µs I_{OUT} = 8500 mA (Dual) I_{OUT} = 5000 mA (Single)		10		mV
Output current	I_{MAX}	Single Phase Dual Phase	5000 9500			mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Switching frequency	f			1.0		MHz
Buck2						
Input voltage	V_{DD}		4.75		5.25	V
Output voltage	V_{BUCK2}	I_{OUT} = I_{MAX} Step = 6.25 mV	1.0		2.19	V
		I_{OUT} = I_{MAX} Step = 12.5 mV	2.2		2.5	V
Output voltage accuracy	V_{BUCK2_ACC}	V_{OUT} = 1 V I_{OUT} = ½I_{MAX}	-3		3	%
Output voltage ripple	V_{BUCK2_RIPPLE}	I_{OUT} = I_{MAX}			30	mVpp
Load regulation transient	V_{TR_LOAD}	I_{OUT} = ¼I_{MAX} to I_{MAX} t_r = t_f = 10 µs V_{OUT} = 1 V L = 1.5 µH		25		mV
Line regulation transient	V_{TR_LINE}	V_{DD} = 4.75 V to 5.25 V tr = tf = 10 µs I_{OUT} = 2000 mA		10		mV
Output current	I_{MAX}		2000			mA
Switching frequency	f			1.0		MHz
Buck3						
Input voltage	V_{DD}		4.75		5.25	V
Output voltage	V_{BUCK3}	I_{OUT} = I_{MAX} Step = 6.25 mV	1.3		2.19	V
		I_{OUT} = I_{MAX} Step = 12.5 mV	2.2		3.4	V
Output voltage accuracy	V_{BUCK3_ACC}	I_{OUT} = ½ I_{MAX} Note: V_{BUCK3} < 2.5 V	-3		3	%
Output voltage ripple	V_{BUCK3_RIPPLE}	I_{OUT} = I_{MAX}			30	mVpp
Load regulation transient	V_{TR_LOAD}	I_{OUT} = ¼I_{MAX} to I_{MAX} t_r = t_f = 10 µs V_{OUT} = 1 V L = 1.5 µH		25		mV
Line regulation transient	V_{TR_LINE}	V_{DD} = 4.75 V to 5.25 V t_r = t_f = 10 µs I_{OUT} = 2000 mA		10		mV
Output current	I_{MAX}		2000			mA
Switching frequency	f			1.0		MHz

3.1 Inductor Selection

For most applications, buck converter power inductors are generally chosen so the peak-to-peak ripple current is 30 % to 40 % of the nominal current. Given a target ripple current of 40 %, the required inductors can be calculated using the following equations:

Buck1:

$$L = \frac{V_{OUT} \times \left(V_{IN(\max)} - V_{OUT}\right)}{V_{IN(\max)} \times \Delta I_L \times f_{sw}} = \frac{1V \times (5V - 1V)}{5V \times (9.5\,A/2) \times 0.4 \times 1\,Mhz} = 0.42\,\mu H \quad (1)$$

Buck2:

$$L = \frac{V_{OUT} \times \left(V_{IN(\max)} - V_{OUT}\right)}{V_{IN(\max)} \times \Delta I_L \times f_{sw}} = \frac{1.2V \times (5V - 1.2V)}{5V \times 2\,A \times 0.4 \times 1\,Mhz} = 1.14\,\mu H \quad (2)$$

Buck3:

$$L = \frac{V_{OUT} \times \left(V_{IN(\max)} - V_{OUT}\right)}{V_{IN(\max)} \times \Delta I_L \times f_{sw}} = \frac{1.5V \times (5V - 1.5V)}{5V \times 2\,A \times 0.4 \times 1\,Mhz} = 1.31\,\mu H \quad (3)$$

Choose a 1.5 µH inductor for all buck converters to optimize cost and performance.

3.2 Output Capacitor Selection

The criteria for the output capacitor selection is determined by the output voltage ripple. Use the following equation to calculate the required output capacitance:

$$C_{OUT(\min)} = \frac{\Delta I_L}{8 \times f_{sw} \times \Delta V_{OUT}} \quad (4)$$

Buck1:

$$C_{OUT(\min)} = \frac{\Delta I_L}{8 \times f_{sw} \times \Delta V_{OUT}} = \frac{(9.5\,A/2) \times 0.4}{8 \times 1\,Mhz \times 30\,mV} = 7.92\,\mu F \quad (5)$$

Buck2:

$$C_{OUT(\min)} = \frac{\Delta I_L}{8 \times f_{sw} \times \Delta V_{OUT}} = \frac{2\,A \times 0.4}{8 \times 1\,Mhz \times 30\,mV} = 3.33\,\mu F \quad (6)$$

Buck3:

$$C_{OUT(\min)} = \frac{\Delta I_L}{8 \times f_{sw} \times \Delta V_{OUT}} = \frac{2\,A \times 0.4}{8 \times 1\,Mhz \times 30\,mV} = 3.33\,\mu F \quad (7)$$

For all buck converters, consider the stability of each buck converter. The minimum capacitor requirement should at least 60 µF, therefore two 0805, 47 µF, 10 V, X5R ceramic capacitors are used for buck converters output capacitors.

3.3 Input Capacitor Selection

For the 250 mV input voltage ripple requirement (5 % of the input voltage), the minimum input capacitor of buck converters can be derived from the following equation:

Buck1:

$$C_{IN(\min)} = \frac{Iout \times Vout}{V_{in,ripple} \times V_{IN} \times f_{sw}} = \frac{9.5\,A \times 1V}{250\,mV \times 5\,V \times 1\,mHz} = 7.6\,\mu F \quad (8)$$

Buck2:

$$C_{IN(\min)} = \frac{Iout \times Vout}{V_{in,ripple} \times V_{IN} \times f_{sw}} = \frac{2\,A \times 1.2\,V}{250\,mV \times 5\,V \times 1\,mHz} = 1.92\,\mu F \quad (9)$$

Buck3:

$$C_{IN(\min)} = \frac{Iout \times Vout}{V_{in,ripple} \times V_{IN} \times f_{sw}} = \frac{2\,A \times 1.5\,V}{250\,mV \times 5\,V \times 1\,mHz} = 2.4\,\mu F \quad (10)$$

Also the RMS current flow into the input capacitor could be derived from the following equation:

Buck1:

$$I_{CIN} = \sqrt{\frac{V_{OUT}}{V_{IN}}\left[I_{OUT}{}^2 \left(1 - \frac{V_{OUT}}{V_{IN}}\right)\right]} = I_{OUT} \times \sqrt{D \times (1-D)} = 3.8\,A\,RMS \quad (11)$$

Buck2:

$$I_{CIN} = \sqrt{\frac{V_{OUT}}{V_{IN}}\left[I_{OUT}{}^2 \left(1 - \frac{V_{OUT}}{V_{IN}}\right)\right]} = I_{OUT} \times \sqrt{D \times (1-D)} = 0.85\,A\,RMS \quad (12)$$

Buck3:

$$I_{CIN} = \sqrt{\frac{V_{OUT}}{V_{IN}}\left[I_{OUT}{}^2 \left(1 - \frac{V_{OUT}}{V_{IN}}\right)\right]} = I_{OUT} \times \sqrt{D \times (1-D)} = 0.92\,A\,RMS \quad (13)$$

Choose two 2012, 10 µF, 35 V, X5R ceramic capacitors, 2.5 A RMS current rating per capacitor for Buck1, and one 2012, 10 µF, 35 V, X5R ceramic capacitor, 2.5 A RMS current rating per capacitor for Buck2 and Buck3. Higher voltage rating for input capacitor could decrease the derating effect of the ceramic capacitor, ensure the sufficient capacitance during Buck converter operation.

4 Component Selection Summary

The components in this example are listed as below.

4.1 Capacitors

Ref	Value	Tol.	Size (mm)	Height (mm)	Temp. Char.	Rating (V)	Part
VLDO2	2 x 1 µF	±10 %	0603	0.9	X5R	10	GRM188R61A105KA61D
VLDO1	1 µF	±10 %	0603	0.9	X5R	10	GRM188R61A105KA61D
VD1V5	2.2 µF	±10 %	0603	0.9	X5R	10	GRM188R61A225KE34
VBuck1	2 × 100 nF	±10 %	0402	0.55	X7R	16	GRM155R71C104KA88D
	2 × 10 µF	±10 %	0805	1.35	X5R	16	GRM21BR61C106KE15L
	2 × 47 µF	±20 %	0805	1.45	X5R	10	GRM21BR61A476ME15
VBuck2 VBuck3	100 nF	±10 %	0402	0.55	X7R	16	GRM155R71C104KA88D
	10 µF	±10 %	0805	1.35	X5R	16	GRM21BR61C106KE15L
	2 × 47 µF	±20 %	0805	1.45	X5R	10	GRM21BR61A476ME15
VREF VDDIO	100 nF	±10 %	0402	0.55	X5R	10	GRM155R61A104KA01D
VDD VDVDD	1 µF	±10 %	0603	0.9	X5R	10	GRM188R61A105KA61D

4.2 Inductors

Ref	Value	ISAT (A)	IRMS (A)	DCR (Typ) (mΩ)	Size (W×L×H) (mm)	Part
Buck1 Buck2 Buck3	1.5 µH	11.5 10	11 8.5	9.7 12	7.1×6.5×3	TDK SPM6530T -1R5M Sunlord WPL6530H1R5MT
		11.5 10	11 8.5	9.7 12	7.1×6.5×3	TDK SPM6530T -1R5M Sunlord WPL6530H1R5MT
		11.5 10	11 8.5	9.7 12	7.1×6.5×3	TDK SPM6530T -1R5M Sunlord WPL6530H1R5MT

5 Conclusions

With its unique features and flexibility, the PV88090 supports many different applications with varying voltage and current requirements. Using the guidelines discussed in this application note the designer can select the appropriate discrete components easily to implement a robust PMIC design using the PV88090.

Revision History

Revision	Date	Description
1.2	20-Dec-2017	First release
1.1	13-Dec-2017	Corrected grammatical errors in introduction
1.0	30-Sep-2017	Initial version.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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