# Application Note

## PV88090-Dynamic Voltage Control (DVC)

### AN-PV-008


## Abstract

*Dynamic Voltage Control (DVC) facilitates the increase or decrease of power rail voltages dynamically as the load increases on a processor. This functionality save system power when the loading is low while allowing increased processor clocking when system needs it. This application note illustrates the use of DVC using the PV88090 PMIC.*

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# Figures



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# 1 Terms and Definitions

| | |
|---|---|
| GUI | Graphical User Interface |
| LVBuck | Low Voltage Buck converter |

# 2 References

[1] S. Mittal, "A survey of techniques for improving energy efficiency in embedded computing systems", IJCAET, 6(4), 440–459, 2014.

# 3 Introduction

The power consumed by processor cores is proportional to the operating frequency and to supply voltage. DVC is used to optimize performance, power consumption and thermal performance of processor devices. DVC increases voltage to increase processor performance, and decreases voltage to saving power. This technique, initially used in laptops and mobile devices [1], is now becoming prevalent in tethered systems.

# 4 DVC

Traditionally, a mount of resistor divider and MOSFET, as shown in Figure 1, is used to change the divide ratio for adjusting the output voltage of converter. It needs many components and control signals, and therefore, also a large layout area. PV88090 provides DVC, which supports adaptive adjustment of the supply voltage dependent on the processor load, via direct register write in the I2C interface. This simplified the schematics, as shown in Figure 2. The DVC slew rate is also adjustable in the I2C to minimize the overshoot when the output voltage level is not acceptable. For examples of how the PV88090 DVC minimizes overshoot and undershoot, see Figure 3 and Figure 4.

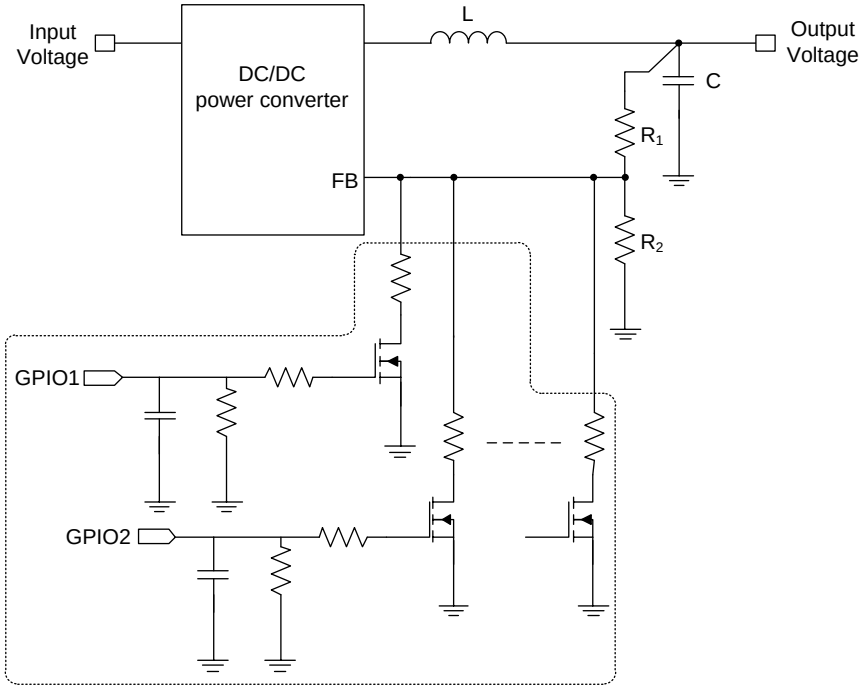


**Figure 1: Traditional DVC solution**

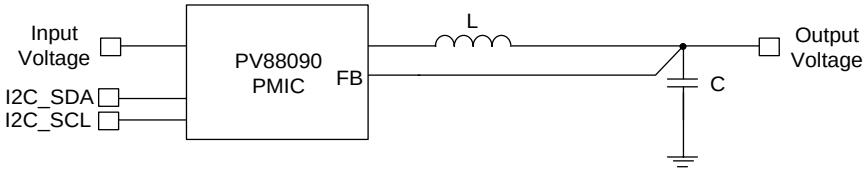


**Figure 2: PV88090 Simplified Block Diagram for one Buck stage**

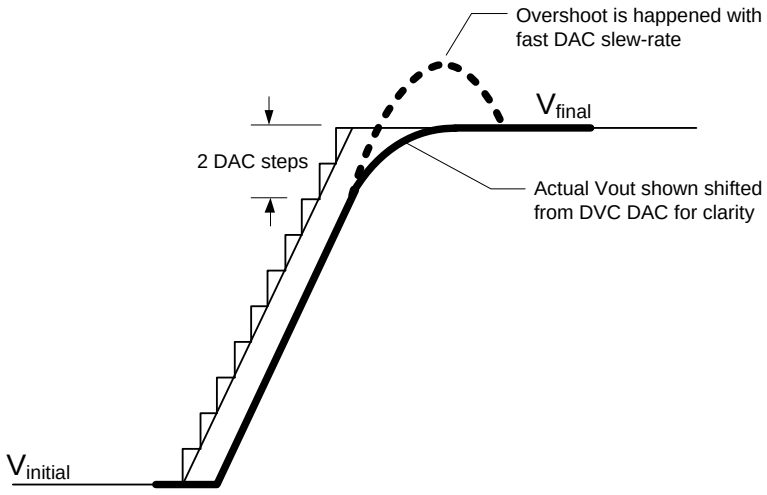


**Figure 3: PV88090 DVC up transition measurement example**

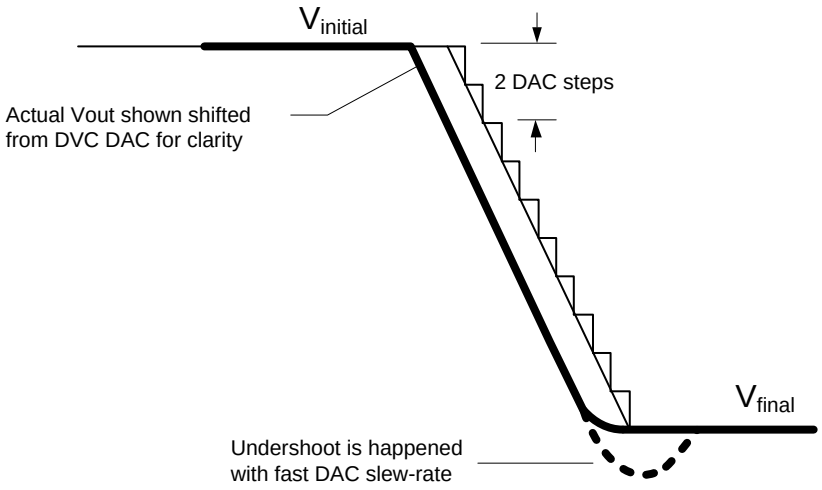


**Figure 4: PV88090 DVC down transition measurement example**

## 4.1 DVC Setting - Buck Converter

**The LVBuck converters support DVC. The output voltage range of BUCK1 is 0.75V to 3.3V, to 3.6V for LVBuck2/3 with different output voltage region showed in Table 1 and** Table 2. Generally, the core voltage of processor is in region 1.

Set register BUCKx_CONF0[6:0] to the target voltage based on your processor requirement. This is done using Dialog's full featured GUI as shown in Figure 5.

**Table 1: Buck1 Output Voltage region**

| Region | Min (V) | Max (V) | Step (mV) |
|---|---|---|---|
| 1 | 0.9 | 1.3 | 12.5 |

**Table 2: Buck2/3 Output Voltage region**

| Region | Min (V) | Max (V) | Step (mV) |
|---|---|---|---|
| 1 | 0.6 | 1.4 | 6.25 |
| 2 | 1.4 | 2.2 | 6.25 |

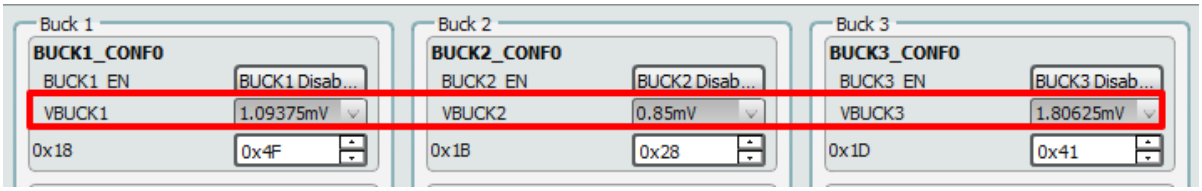


**Figure 5: Dialog GUI - BUCKx_CONF0[6:0]**

The DVC slew rate is adjustable for preventing overshoot or undershoot on the output voltage by setting register Buckx_CONF3[7:6]. This is done using Dialog's full featured GUI as shown in Figure 6. Generally, higher slew rate are more likely to cause overshoot or undershoot. **Error! Reference source not found.** to Figure 8 shows the DVC waveform with different slew. The overshoot and undershoot due to faster slew rate can be observed in Figure 7 and Figure 8.

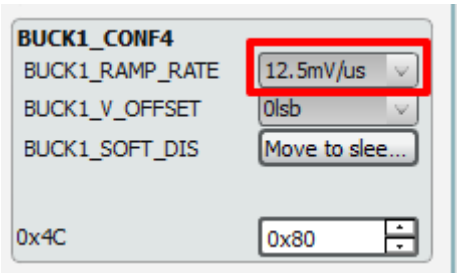


**Figure 6: Dialog GUI - BUCKx_CONF3[7:6]**

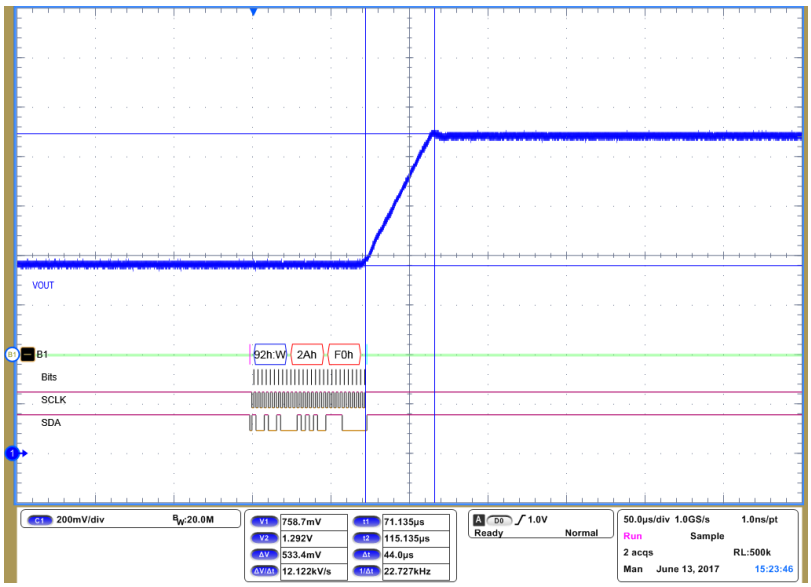


**Figure 7: DVC step-up with 12.5mV/µS slew rate**

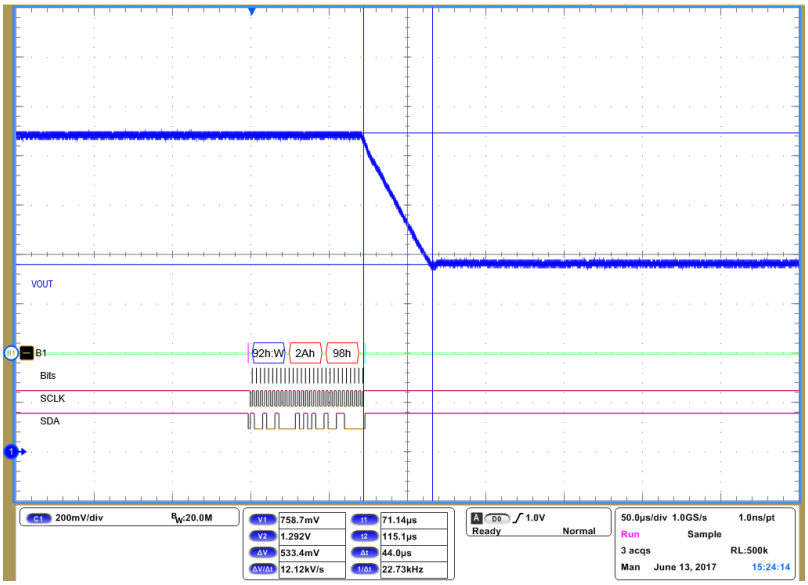


**Figure 8: DVC step-down with 12.5mV/µS slew rate**

By way of example, a processor is supplied by the LVBuck1 for the typical core voltage 1.2V. The LVBuck1 output voltage is in region1, the output voltage table as shown in 1. In idle mode, the core voltage of the process is 1.15V required for saving power. We choose the slew rate 3.125mV/µS for preventing overshoot. Sending the commend 0xD8 to BUCK1_CONF0(0x2A) via I2C interface as shown in Figure 9 and the behavior is showed in Figure 10. The output voltage return to 1.2V that means sending the commend 0xE0 to BUCK1_CONF0(0x2A) as shown in Figure 11 and the waveform is showed in Figure 12.

**Table 3: LVBuck1 Output Voltage - region1**

Register BUCK1_CONF0

| Address | Name | POR value | |
|---|---|---|---|
| 0x0018 | BUCK1_CONF0 | 0x50 | |
| 7 | 6 | 5 | 4 |
| BUCK1_EN | | | |

| Field name | Bits | Type | POR | |
|---|---|---|---|---|
| BUCK1_EN | [7] | RW OTP | 0x0 | Value: 0x0 (POR) = 0: BUCK1 Disabled; 0x1 = 1: BUCK1 Enabled |
| VBUCK1 | [6:0] | RW OTP | 0x50 | Buck Dual Phase Voltage. Value: 0x0 = 0000000: 600mV; 0x1 = 0000001: 606.25mV; 0x2 = 0000001: 612.5mV; ...; 0x3D = 1111101: 1.38125V; 0x3E = 1111110: 1.3875V; 0x3F = 1111111:1.39375V |

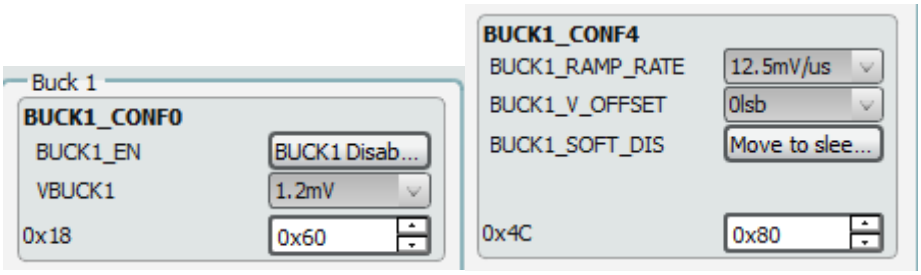


**Figure 9: Setting in Dialog GUI_Sending 0X60 to BUCK1_CONF0**

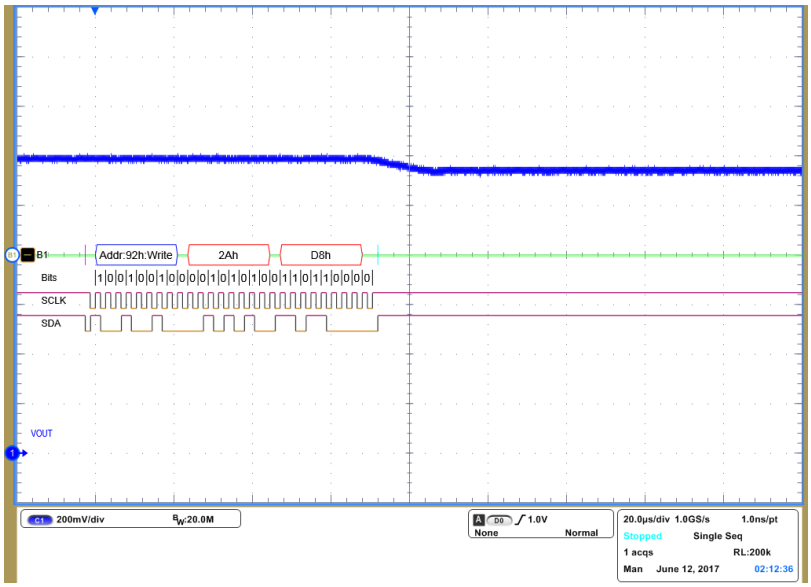


**Figure 10: DVC step-down from 1.2V to 1.15V**

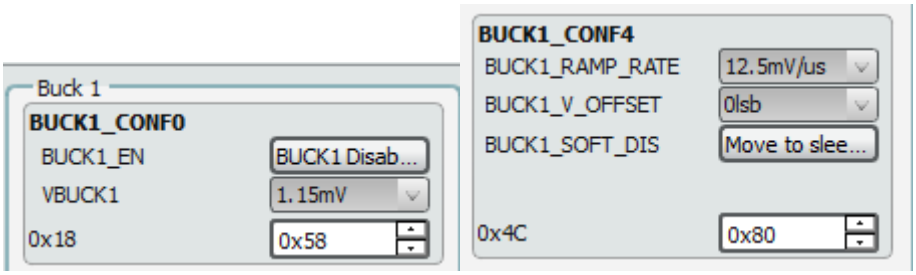


**Figure 11: Setting in Dialog GUI_Sending 0x58 to BUCK1_CONF0**

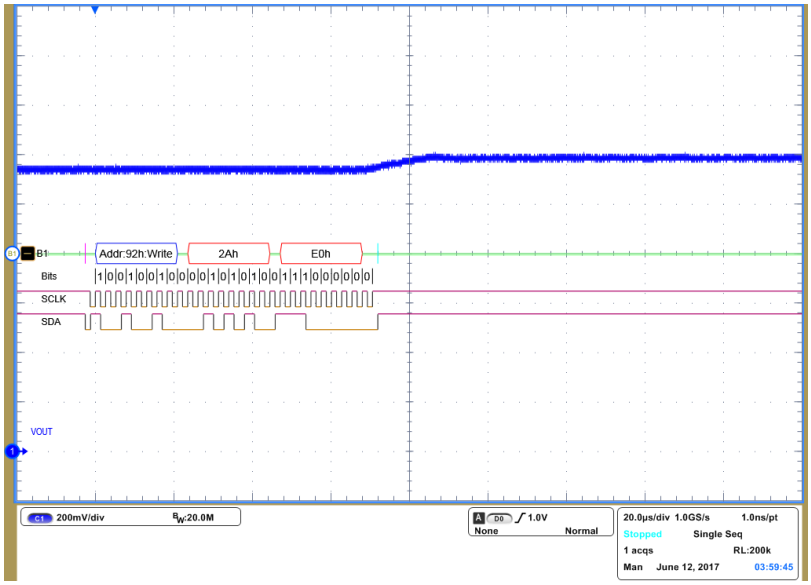


**Figure 12: Dynamic Voltage Control step-up from 1.15V to 1.2V**

# 5 Conclusions

Both the LVBUCKs and HVBUCK in PV88090 support dynamic voltage control(DVC) function. The DVC slew rate is flexible to meet different application for preventing overshoot and undershoot. The I2c interface provides a standard and flexible way to control this feature.

## Revision History

| Revision | Date | Description |
|---|---|---|
| 1.0 | <23-Sun-2017> | Initial version. |

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