R2A20132

Application Note

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1. Introduction

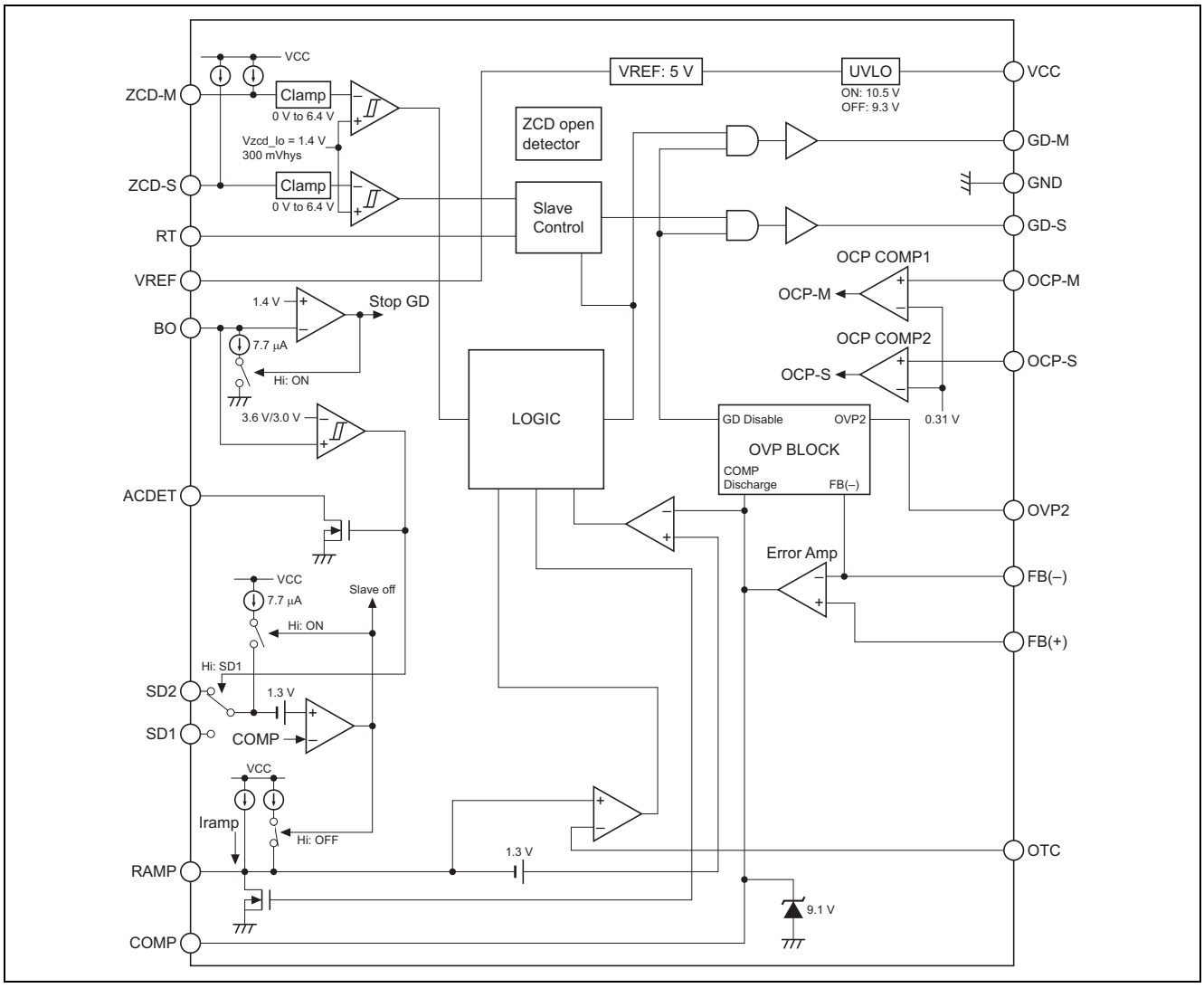
The R2A20132 is an active power factor correction controller that operates in the critical conduction mode (CRM). And the R2A20132 has the interleaved operation function that controls the two boost converters (master and slave) with anti-phase control scheme.

The R2A20132 employs the voltage mode CRM, in which a Power MOSFET is turned on when the current of the boost inductor reaches zero and turned off to keep ON time constant by comparing between the increase rate of RAMP signal and the output voltage of the error amplifier. So that, the peak current of the boost inductor follows the input voltage waveform.

The voltage mode CRM PFC controller does not need the input voltage sense line. It can reduce power loss. The master boost converter is controlled by the voltage mode CRM described above and the slave boost converter is controlled by the internal slave control logic circuit and the inductor zero current detection circuit.

The interleaved operation can reduce the input current ripple, therefore it reduces the size of an input filter, parts count and total cost.

2. Block Diagram



3. R2A20132 Block Description

3.1 Zero Current Detection

3.1.1 Zero Current Detection

The zero current detection (ZCD) detects the inductor current. And the power MOSFET turns on when the inductor current reaches zero. ZCD signal is produced by the auxiliary winding of the boost inductor which is connected to ZCD pin through a current limit resistor R_{ZCD}. The voltage of ZCD pin is clamped by R_{ZCD} and the internal clamp circuit. The high side and low side clamp voltages are 6.4 V and 0 V respectively and the maximum source and sink currents are 10 mA. Also 10 μA constant current flows into ZCD pin.

Even if the AC input voltage is high and, so that, the voltage amplitude induced on the secondary winding goes low, the ZCD signal can easily exceed the ZCD high threshold voltage of 1.7 V and then the stable zero current detection can be achieved due to this source current. And also, when the secondary winding is open, ZCD pin is pulled up to 6.4 V by this constant current.

In case VCC of IC is not supplied but, non-zero voltage is induced on the secondary winding, a current flows from ZCD pin to VCC pin. In such a case, this current should not exceed 10 mA which is the maximum ratings of ZCD pin.

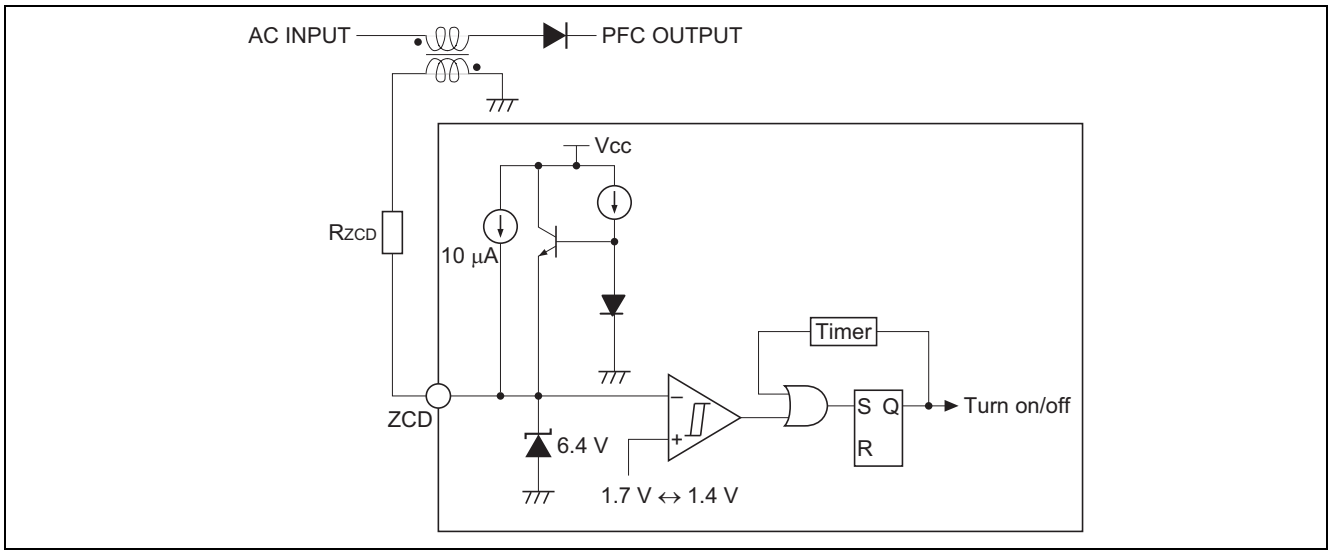


Figure 1

3.1.2 Open Detection of Slave Zero Current Detection

In case the slave zero current detection signal is not propagated to the detection circuit due to open circuit or GND short of ZCD pin, the IC stops not only switching operation of master but also stops that of slave to avoid heat up of master converter, which occurred in order to supply power only by the master converter if only the operation of slave is stopped. In this case IC stops a switching with latch, and the latch is reset when VCC voltage is under UVLO threshold voltage. Latch set time is about 100ms in case the switching frequency is 10 kHz. This time is determined by switching frequency × 1024 count.

In case the master zero current detection signal is propagated to the detection circuit due to GND short of ZCD pin, the operation of master operates in restart mode, and maximum ON time of power MOSFET for master is limited to1us in restart mode. On the other hand, the operation of slave does not operate in master restart mode, so that it is possible to avoid heat up of master and slave converters.

In case the master zero current detection signal is not propagated to the circuit due to open circuit of ZCD pin, the operation of master and slave both stops. (Non-latch)

The condition that switching stop: However master stops without latch, slave stops with latch.

a) ZCD-M pin open (ZCD-M pin becomes high: 6.4 V)
b) ZCD-S pin open (ZCD-S pin becomes high: 6.4 V) or GND short

However in case that master operates with restart or on time of master is 1.5 μs and under, this function is not available.

3.2 Error Amplifier

R2A20132 employs a trance conductance amplifier as the error amplifier. The output current changes according to a voltage difference between FB(–) pin voltage and externally supplied reference voltage, i.e. the voltage of FB(+). COMP pin which is output of the error amplifier is clamped at 9.1 V. COMP quick charge function is built-in. If FB(–) voltage exceeds VFB(+) × 0.92, and then FB(–) voltage becomes under VFB(+) × 0.92, COMP voltage goes up quickly by the quick charge function. In the load change test, the output voltage drop is avoided by this function.

When AC input is supplied and VCC is not supplied, a current flows from PFC output to VCC through the divider resistor and internal ESD protection diode which is between FB(–) pin and VCC pin. This current can be changed by the divider resistor value and AC input voltage, so that it should not exceed 300 μADC. Rough calculation gives the current value as (PFC output voltage) / (resistor value between PFC output and FB(–) pin). We strongly recommend VFB(+) = 2.5 V which is 1/2 of VREF voltage divided by resisters.

3.3 Protection Circuits

The dynamic over voltage protection, two types of the over voltage protection, the over current protection and the feedback open loop protection are available.

3.3.1 Dynamic Over Voltage Protection (D-OVP)

D-OVP discharges COMP pin voltage when FB(–) pin voltage reaches 1.05 × VFB(+), where VFB(+) = 2.5 V typ (strictly (1.05 – 1)(Vref – VFB(+)) + VFB(+)). The power MOSFET ON time is decreases gradually, so that, an inductor current does not stop suddenly. Therefore the audio noise is avoided.

3.3.2 Over Voltage Protection 1 (OVP1)

OVP1 stops an output when FB(–) pin voltage reaches 1.09 × VFB(+) (strictly (1.09 – 1)(Vref – VFB(+)) + VFB(+)), where VFB(+) = 2.5 V typ. A Power MOSFET turns off quickly and OVP1 keeps stopping an output till FB(–) pin voltage reaches 1.09 × VFB(–) – 100 mV (strictly (1.09 – 1)(Vref – VFB(+)) + VFB(+) – 100 mV), when VFB(+) = 2.5 V typ.

3.3.3 Over Voltage Protection 2 (OVP2)

OVP2 stops an output when FB(–) pin voltage reaches 2.685 V (typ.). A power MOSFET is turned off quickly and OVP2 keeps stopping an output till FB(–) pin voltage reaches 2.585 V typ.

3.3.4 Feed Back Open Loop Detection

The feedback open-loop protection discharges COMP pin voltage during FB(–) pin voltage is under 0.5 V. Therefore an output does not appears in this case. There is 0.2 V hysteresis as shown in the diagram below.

3.3.5 Over Current Protection (OCP)

OCP pin senses the each power MOSFET drain current by using an external sense resistor. When OCP-M or OCP-S pin reaches 0.31 V, an output is disabled.

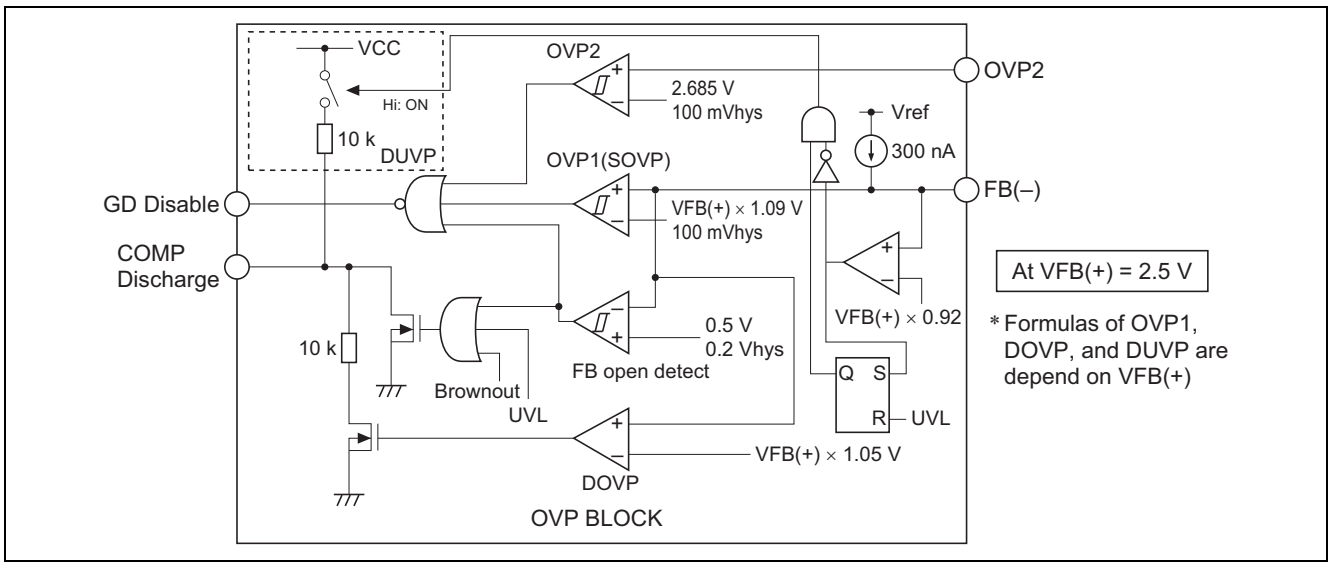


Figure 2

3.4 Ramp Generator

The ramp slope (increase rate) is determined by external capacitor and resistor. The resistor is connected between RT pin and GND, and the capacitor is connected between RAMP pin and GND. RT pin resistor determines the internal oscillation frequency. So that normally this resistor value should be fixed at 22 kΩ. In this case, RAMP pin source current is 165 μA (typ.).

ON time becomes the maximum duration when the output voltage of the error amplifier is 9.1 V. When a capacitor on RAMP pin is 680 pF, the maximum ON time is calculated as 32 μs: 680 pF × (9.1 V – 1.3 V) = 165 μA × tonmax.

The ramp generator starts charging RAMP pin when ZCD detects the inductor zero current and RAMP pin voltage is under 0.2 V.

The ramp generator starts to discharge RAMP pin when the ramp slope reaches COMP voltage.

And when the error amplifier output is under 1.3 V, power MOSFET ON time is zero. Because the level shift voltage of 1.3 V is on RAMP pin internally.

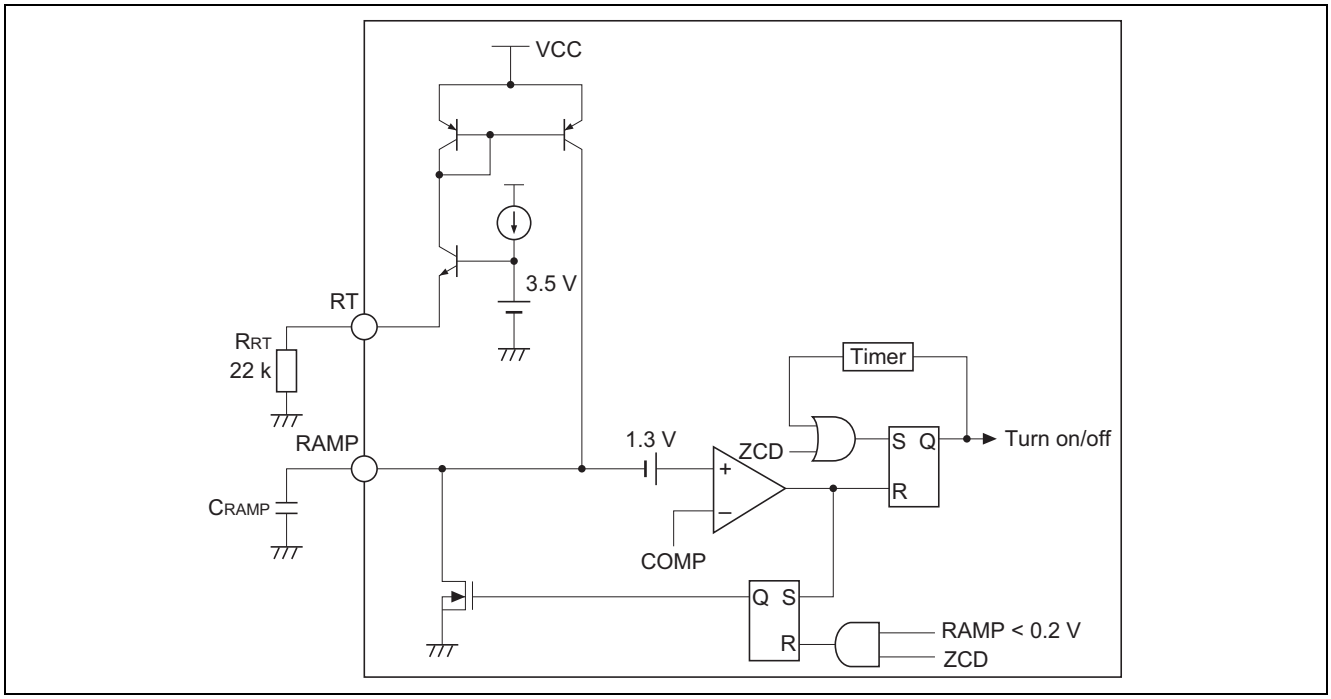


Figure 3

3.5 Drive Stage

The R2A20132 contains two totem-pole output stages for master and slave. The source drivability is 300 mA peak and the sink drivability is 1.2 A peak. Though basically an external pre-driver is not needed, however, if the Qg of Power MOSFET is large or the distance between IC and Power MOSFET is long, please adjust a driving ability according to the characteristics of Power MOSFET to be used. It should be noted that the delay time for turning-off the MOSFET influences power loss more than turning-off in zero current switching scheme.

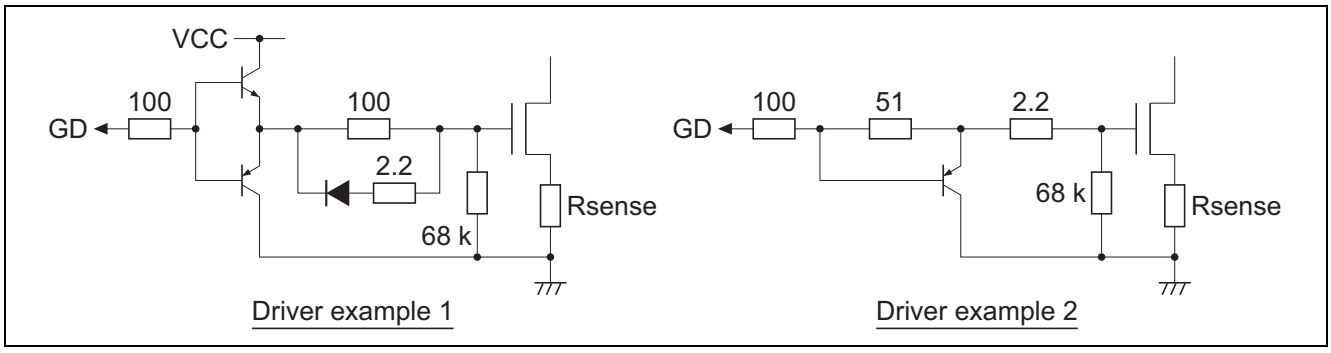


Figure 4

3.6 Brownout and Slave Drop (SD)

Gate drive switching stops when BO pin voltage becomes less than 1.4 V. It is possible to change operating point of brownout by changing the ratio of the resistor divider. And the hysteresis characteristics is determined by the value of resistor and 7.7 μA constant current source, so that, users can be adjusted it by the resistor value. Also the threshold voltage of the slave drop (SD) function, by which slave gate drive can be stopped to improve light load efficiency, is selected by BO pin voltage. The SD point is adjusted by setting SD pin voltage. Also two types of the SD points can be set individually as Hi line or Lo line:

In case BO pin voltage is over 3.6 V, SD2 pin voltage is selected as threshold voltage of SD point.
In case BO pin voltage is under 3.0 V, SD1 pin voltage is selected as threshold voltage of SD point.

When COMP voltage becomes under SD pin voltage, slave gate drive switching stops and RAMP charge current changes from 164 μA to 82 μA to keep COMP voltage because ON time should be doubled to keep switching operation only by master channel. And the hysteresis characteristics of it, determined by the value of the resistor and 7.7 μA constant current source, can be set by resistor value externally.

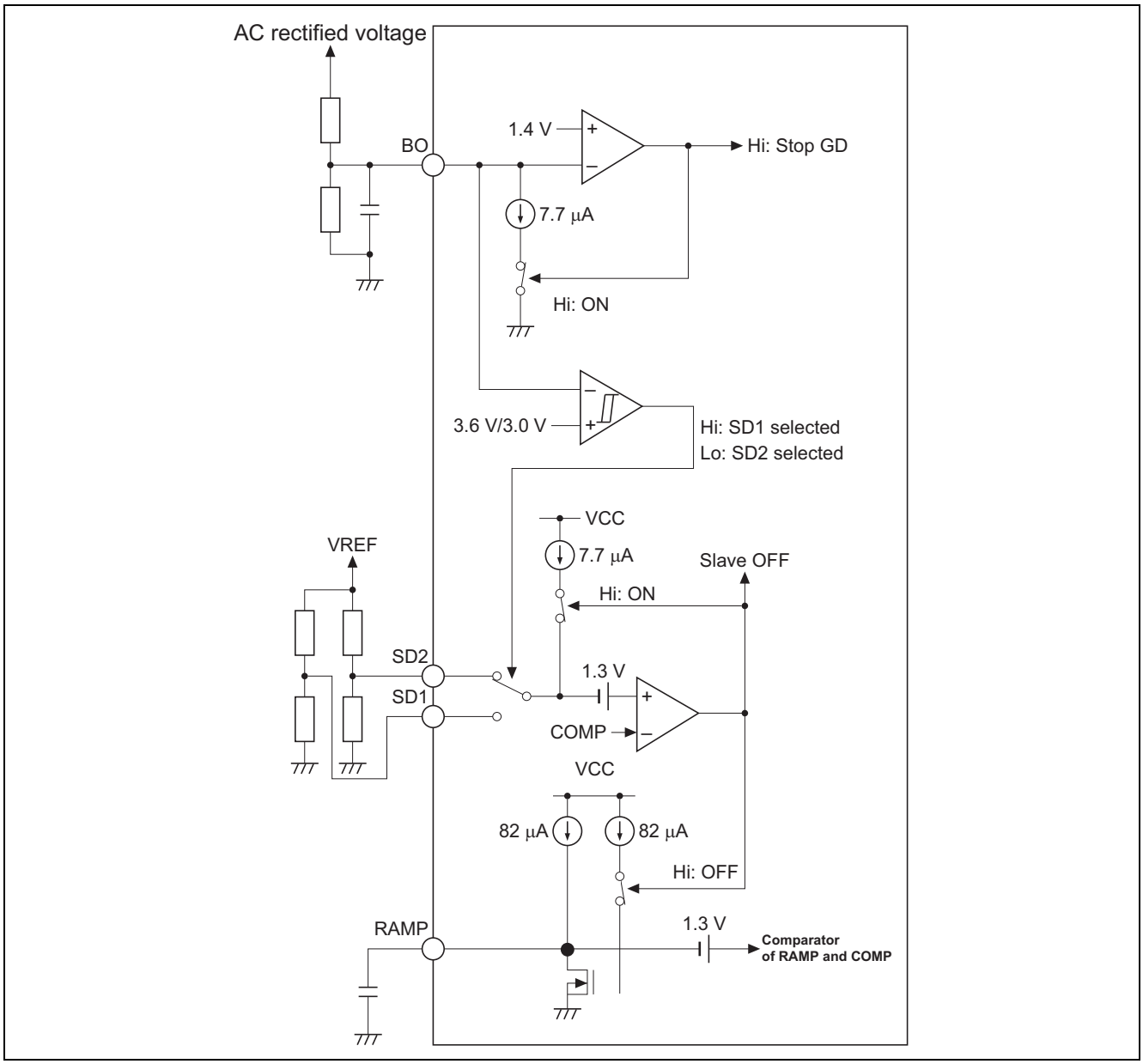


Figure 5

3.7 Other Extra Functions Improving Efficiency

R2A20132 provides some interface functions which can realize extra functions, such as LTB (Load Tracing Boost), FB (follow Boost), DB (Dual Boost) for improving efficiency in suitable ways for various applications along with external circuits and ACDET, VB(+) pins of this IC.

Note: It is not meant that Renesas Electronics permit these patented technology (i.e. efficiency improving by LTB, FB, DB). An user who has a plan to implement these technologies in his or here product should obtain the right to use them or be licensed before mass production.

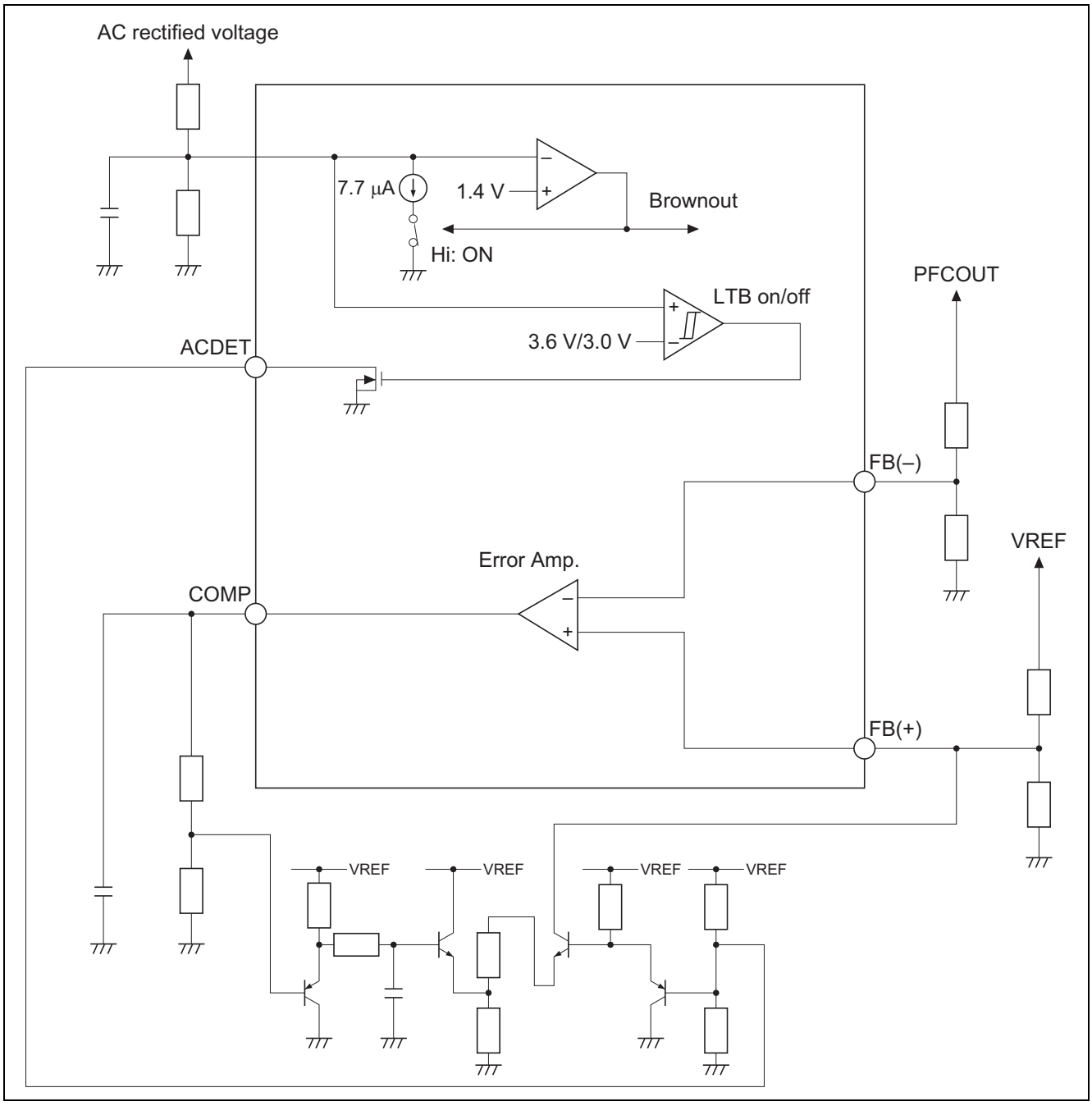
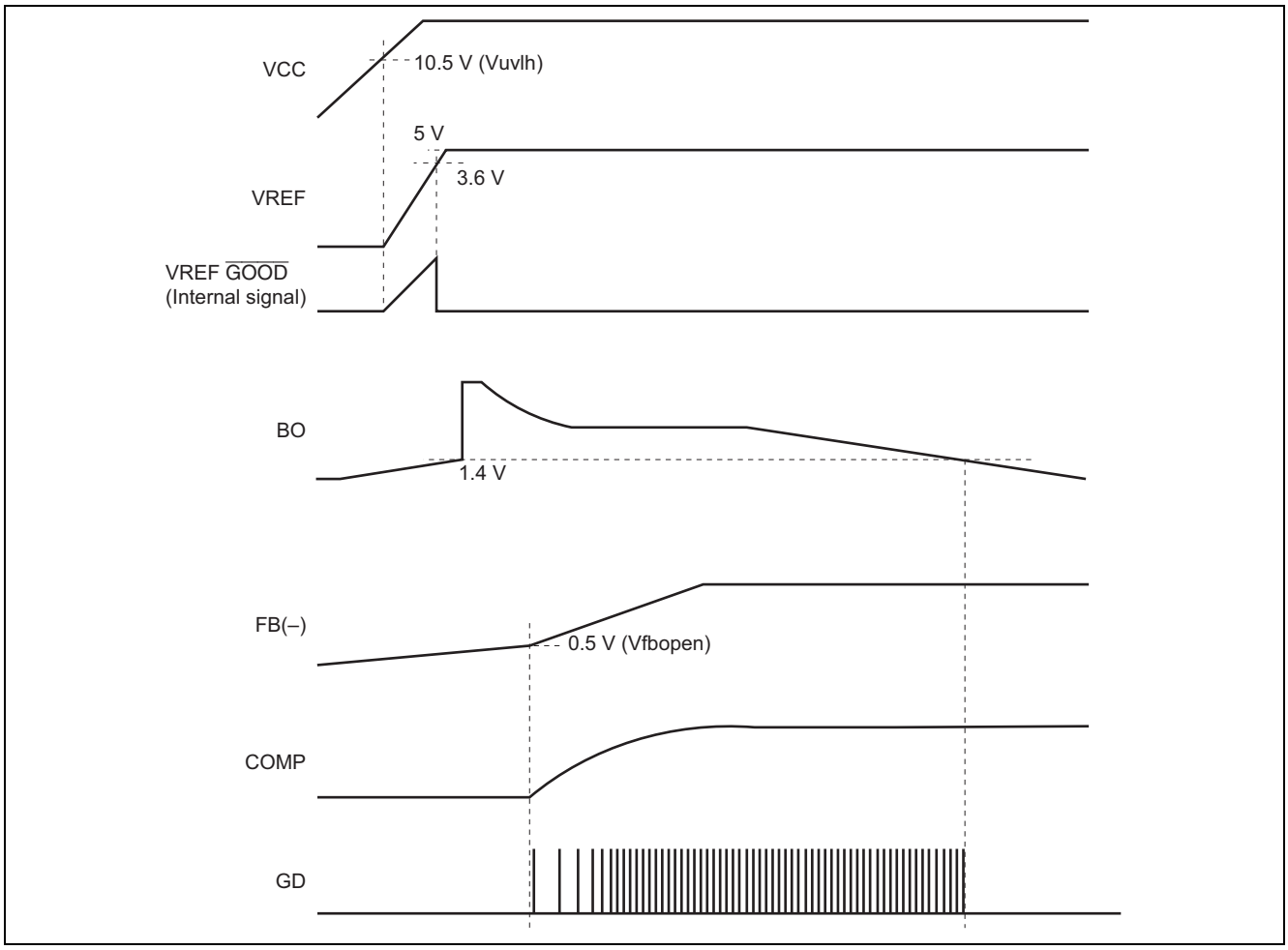


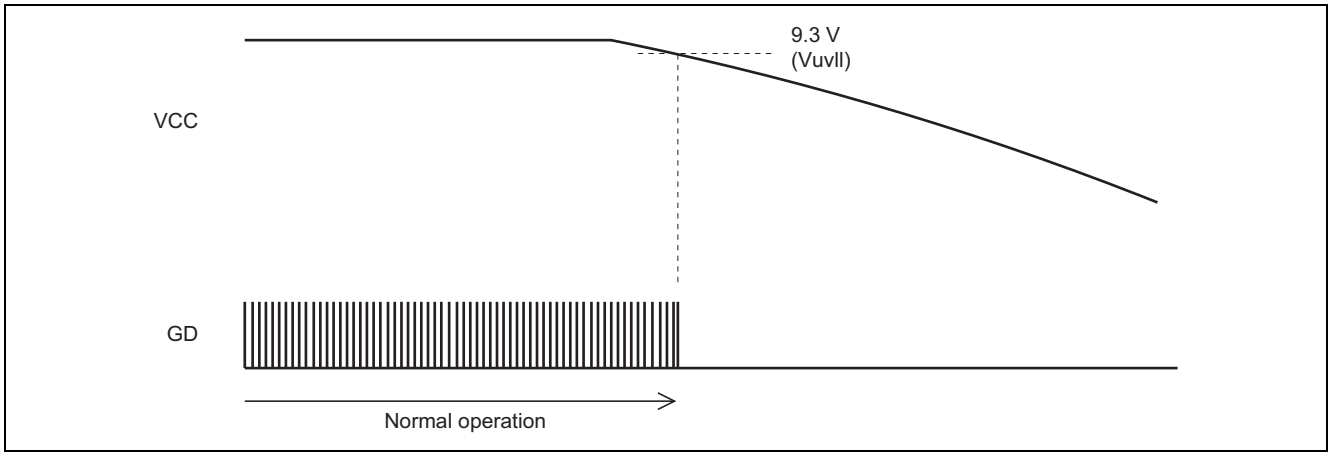
Figure 6

3.8 Timing Chart

3.8.1 Start-up

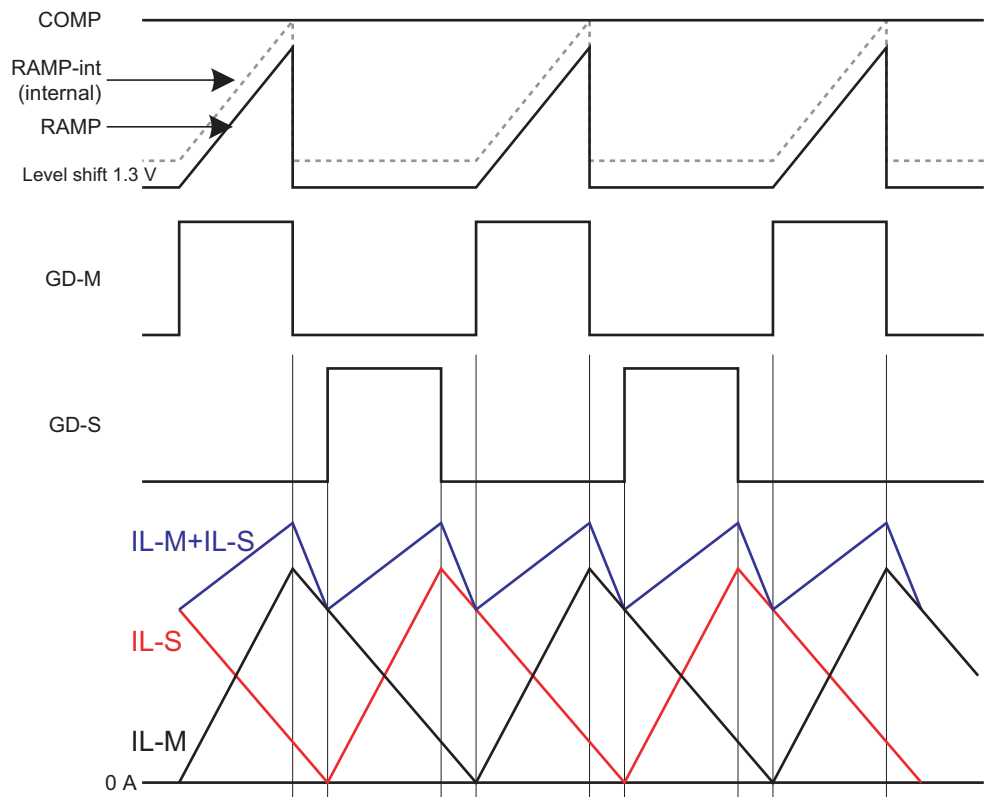


3.8.2 Shut-down

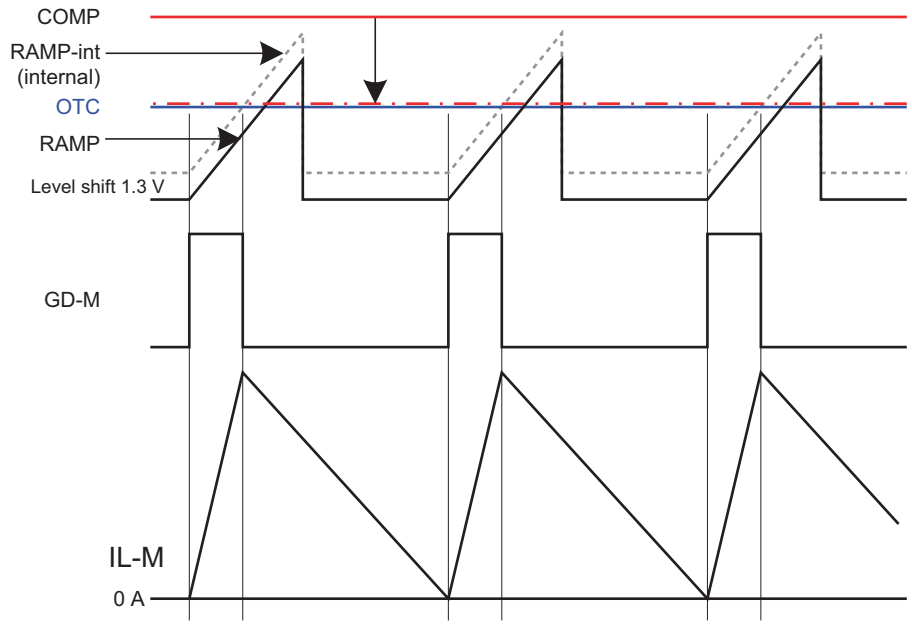


3.8.3 Critical Conduction Mode

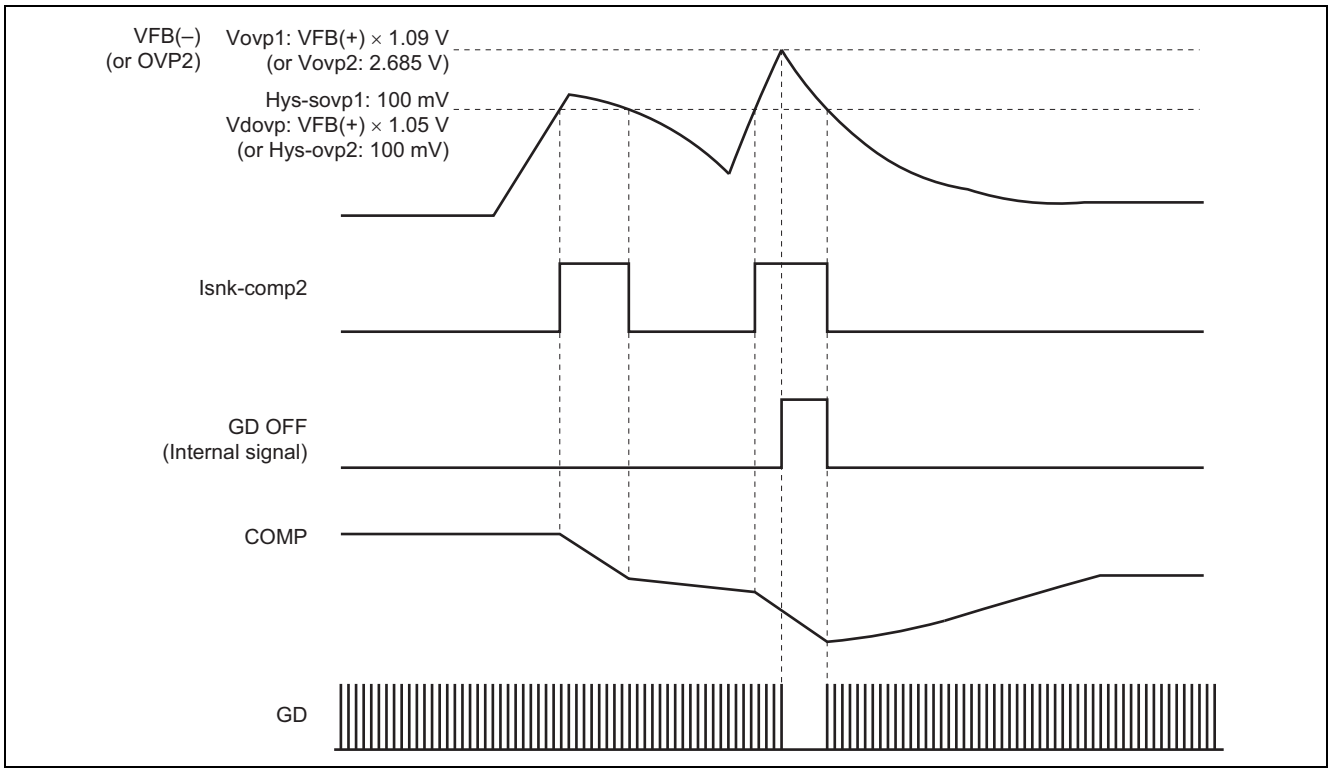
(1) Normal time



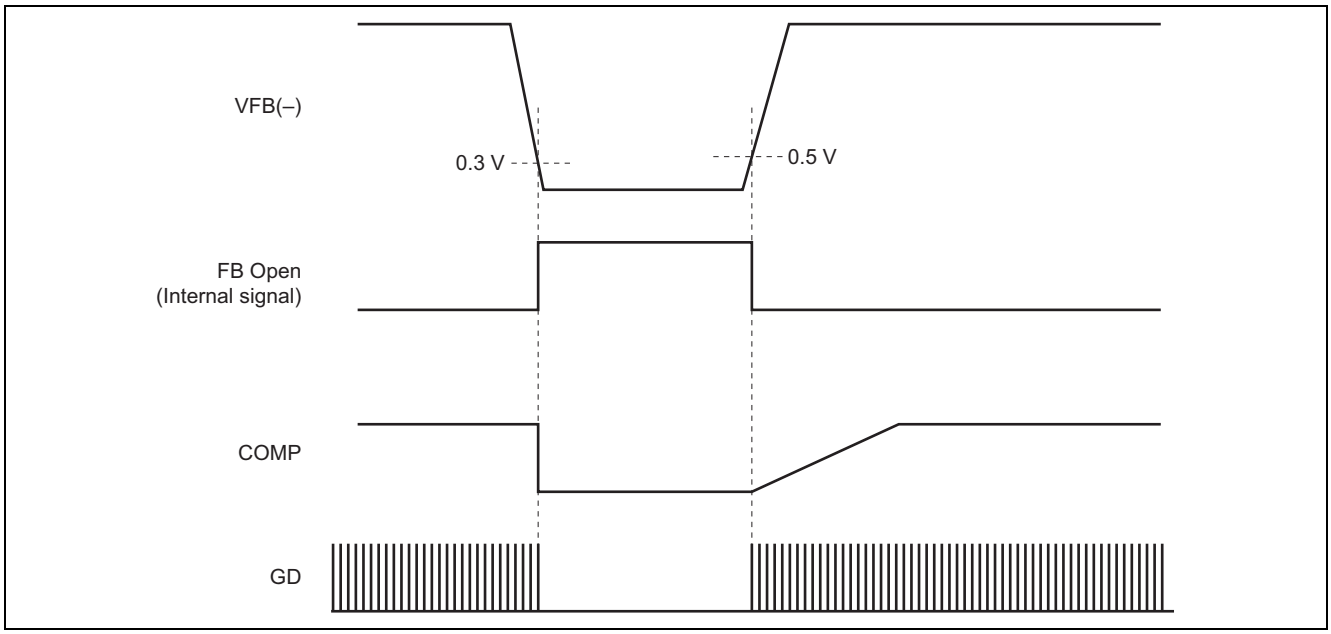
(2) Off time control



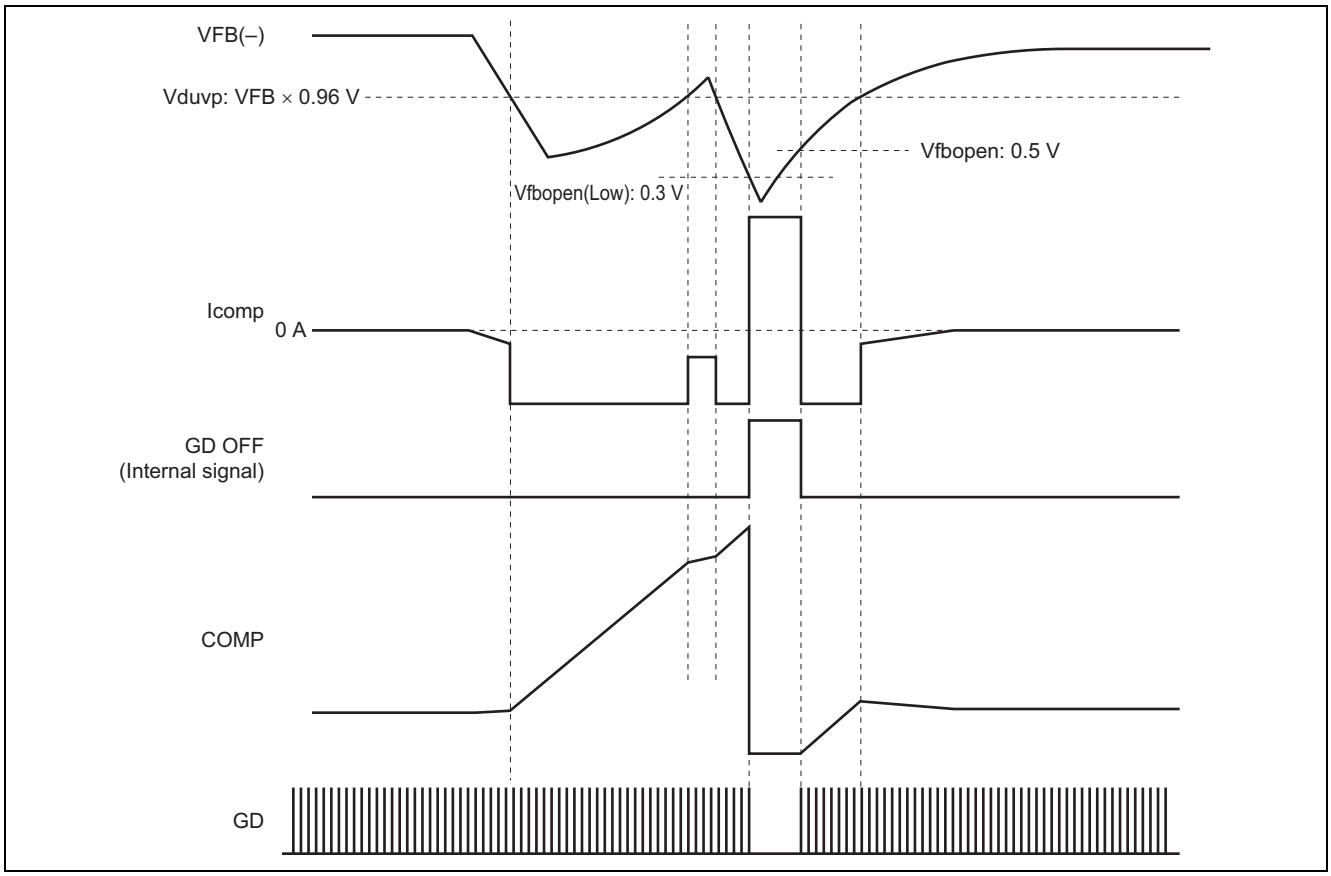
3.8.4 Overvoltage Protection (OVP)



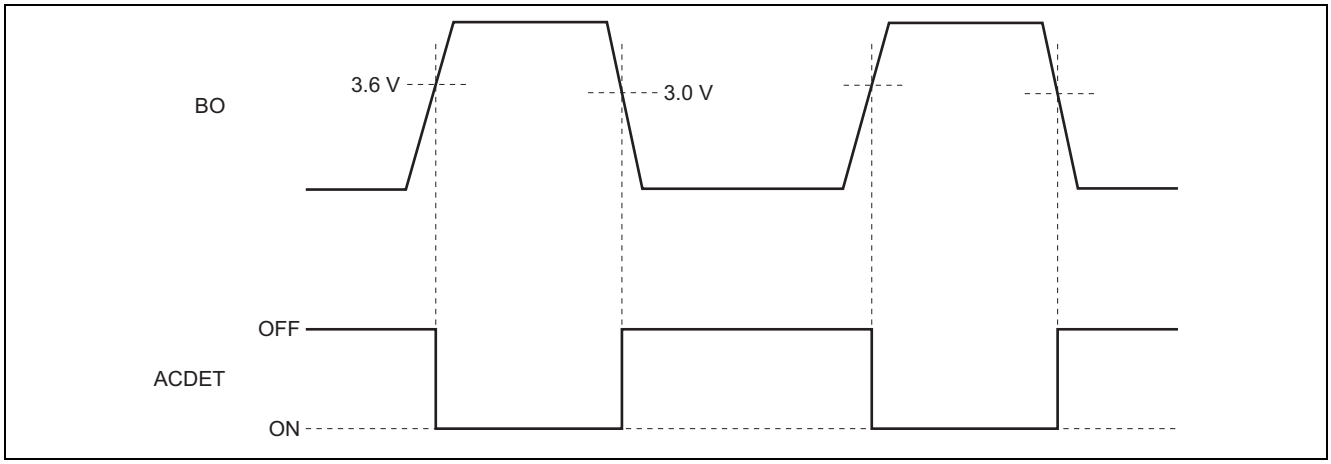
3.8.5 FB Open Detection



3.8.6 Undervoltage Protection (UVP)



3.8.7 ACDET (At the external resistance insertion)



4. Design Guide

Note: * Calculation sheet of excel, in which calculations of circuit constants of external components are provided, is available.

4.1 Boost Inductor

The boost inductor value is determined by an output power and a minimum switching frequency. A minimum switching frequency should be higher than 20 kHz (audio frequency) to avoid audio noise of an inductor or an input capacitor. Generally it is around 50 kHz. The boost inductor value is obtained by equation 1. For a conduction loss η, use the value around 0.9.

$$L[H] = \frac{V_{ACLow}^2 \times \eta}{f_{SWLow} \times V_o \times I_{omax} \times \left(1 + \frac{\sqrt{2} \times V_{ACLow}}{V_o - \sqrt{2} \times V_{ACLow}}\right)} \quad \cdots (1)$$

Vo [V]: PFC output voltage
V_{ACLow} [V]: Effective value of minimum input voltage
Iomax [A]: Maximum output current
f_{SWLow} [Hz]: Minimum frequency

4.2 Output Capacitor

For any preset hold-up time, the capacitor value should satisfy the inequality (2) described below:

$$C_o[F] \geq \frac{2 \times P_o \times t_{hold}}{V_o^2 - V_{omin}^2} \quad \cdots (2)$$

thold [s]: Hold-up time
Vomin [V]: Minimum output voltage

4.3 RAMP Pin Capacitor

COMP pin voltage becomes maximum voltage when minimum input voltage is applied and output current is maximum. The maximum ON time, tonmax is expressed in the next equation. For a conduction loss η, use the value around 0.9.

$$t_{onmax}[s] = \frac{L \times V_o \times I_{omax}}{V_{ACLow}^2 \times \eta} \quad \cdots (3)$$

Therefore RAMP pin capacitor C_{RAMP} is expressed in the next equation.

For a conduction loss η, use the value around 0.9.

$$C_{RAMP}[F] = \frac{I_{RAMP} \times t_{onmax}}{V_{compmax} - 1.3} = \frac{I_{RAMP} \times L \times V_o \times I_{omax}}{(V_{compmax} - 1.3) \times V_{ACLow}^2 \times \eta}$$

$$= \frac{165\,\mu A \times L \times V_o \times I_{omax}}{(V_{compmax} - 1.3) \times V_{ACLow}^2 \times \eta} \quad \cdots (4)$$

Maximum COMP pin voltage is 8 V. Therefore C_{RAMP} can be calculated using the condition of "Vcompmax = 8 V".

4.4 Power MOSFET and Boost Diode

A peak current on a Power MOSFET or a boost diode is expressed in the next equation. For a conduction loss η, use the value around 0.9.

$$I_{Lpk}[A] = \frac{\sqrt{2} \times P_o}{\eta \times V_{ACLow}} \quad \cdots (5)$$

4.5 ZCD Auxiliary Winding

The voltage of auxiliary winding will become minimum when AC input voltage is maximum.

The auxiliary winding value is obtained by equation 6.

And the voltage must be higher than ZCD threshold voltage 1.5 V.

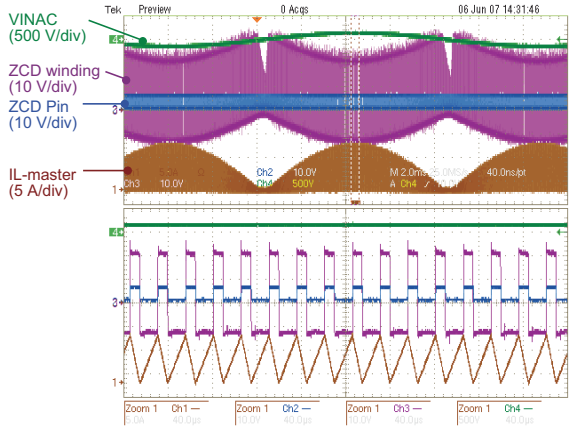
$$Naux = \frac{1.5\ V \times Np}{Vo - \sqrt{2}\ VACmax} \quad \cdots (6)$$

Notes on Audio noise of the inductor and Restart operation in case that AC input voltage is high.

When the AC input voltage exceeds the output voltage, the direct current from AC input to PFC output occurs. In this case, the IC operates with the restart operation because zero current is not detected by ZCD auxiliary winding. Also, when the AC input voltage is high, the voltage of the both ends of the inductor becomes low. Therefore, if the number of turns of ZCD auxiliary winding is not enough, the IC operates the restart operation because the input voltage of the ZCD terminal does not exceed the threshold voltage (Vzcd).

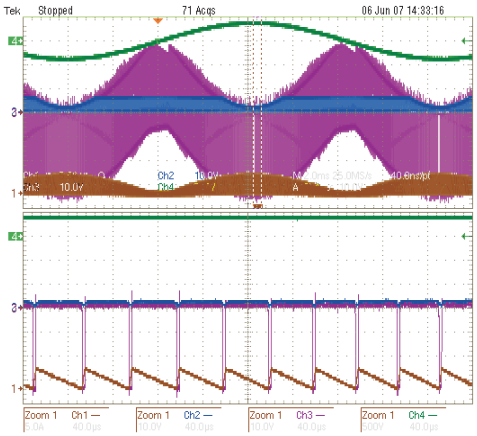
The input voltage making the IC operate restart operation depends on the ripple voltage on the PFC output and the phase difference between the ripple voltage on the PFC output and the input voltage. Therefore, it is possible to raise the input voltage at which the operation starts with the restart operation by setting the output voltage higher or increasing the output capacitor value to reduce ripple voltage. Also, when the restart operation continues, the audio noise of 7.1 kHz (equally restart cycle time:140 µs) of the inductor etc. may occur.

♦Vin: 100 Vac, Output Power: 600 W, Vout: 390 V



Note: This is waveform of R2A20112.

♦Vin: 264 Vac, Output Power: 600 W, Vout: 390 V



Because the turns of the auxiliary winding is not enough, an amplitude of the ZCD terminal becomes small at the peak of AC input voltage.

Figure 7

4.6 ZCD input resistor R_{ZCD}

The maximum ratings of ZCD pin current is 10 mA. So R_{ZCD} is selected with 10 mA and under.

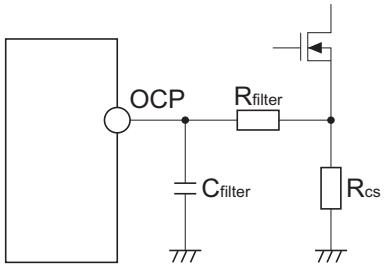
R_{ZCD} is obtained by equation 7.

$$RZCD = \left[\frac{Vo \times Naux}{Np} - 6.4\ V\right] / 3\ mA \quad \cdots (7)$$

4.7 Over Current Detection Resistor Rcs

The value of Rcs is obtained by equation 8. The resultant value is generally very small (ex: 200 mΩ), so that care should be taken in pattern impedance. And it is recommended that a CR filter of around 1 MHz should be connected to the OCP pin to eliminate switching noises.

$$Rcs[\Omega] = 0.31\ V \times \frac{\eta \times V_{ACLow}}{\sqrt{2} \times P_O} \quad \cdots (8)$$



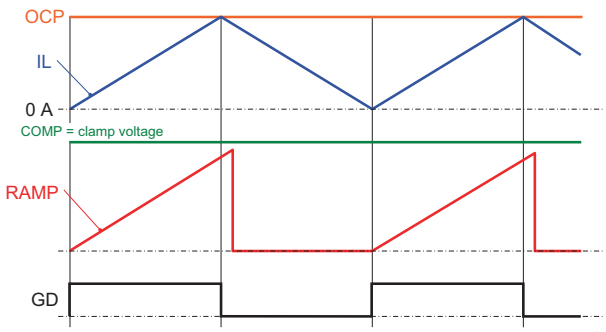
Notes on audio noise of the inductor occurring when the over current is detected.

In the case that the setting level of the over-current detector is lower than the maximum peak current which is determined by tonmax, and when the over-current detector detects over-current, the power MOSFET is turned off. However, the current of the inductor varies discontinuously ("current discontinuous state") because the RAMP terminal is not discharged until the RAMP voltage reaches the COMP voltage.

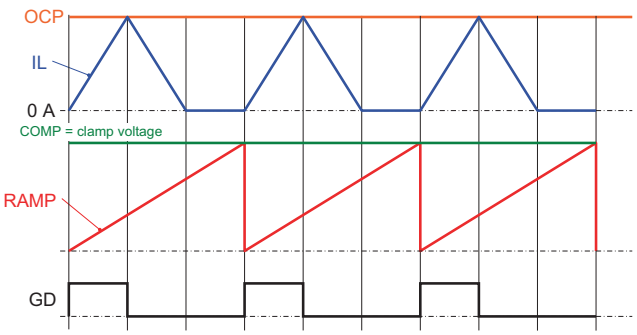
In such a situation, the condition that the power MOSFET is turned on again is that the RAMP terminal is discharged and then the voltage of the ZCD terminal becomes low.

In the "current continuous state", the voltage of the ZCD terminal varies between high and low repetitively (resonant operation). If discharge of the RAMP terminal is just completed while the voltage of the ZCD terminal is low, the power MOSFET is turned on at once. On the other hand, if discharge of the RAMP terminal is completed while the voltage of the ZCD terminal is high, the power MOSFET is turned on at next resonant cycle (the cycle on which the voltage of the ZCD terminal is low).

Therefore, if the relation in transient timing between the signals of the ZCD and RAMP terminals is marginal in the resonant operation, there is possibility that the period of the power MOSFET being turned off varies every cycle. And if the cycle time of the period variation is on audible range, the audio noise of the inductor etc., may occur.



Case: the setting level of the over-current detector is close to the maximum peak current.



Case: the setting level of the over-current detector is lower than the maximum peak current.

Figure 8

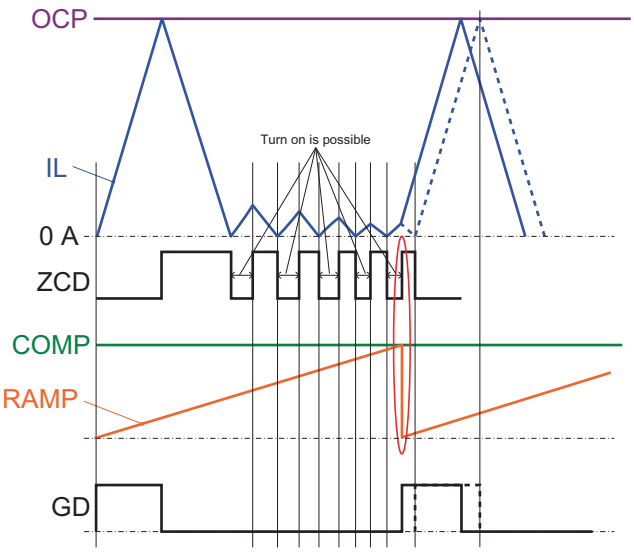


Figure 9 Factor of Audio Noise of the Inductor

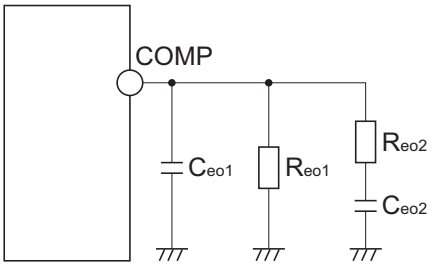
4.8 Frequency Characteristics of the Error Amplifier (gm amplifier)

The error amplifier is a transconductance amplifier (hereafter, gm amplifier). It does not need a feedback circuit onto the input side. Therefore, it is possible to minimize influence of the feedback circuit on input circuit.

Gain of gm amplifier is calculated by product of transconductance and output impedance. It is obtained by equation 9, where Gm-v is tranceconductance of the gm amplifier, Rvo is an output resistor of the gm amplifier itself.

Outline of the characteristics of gain of gm amplifier is shown in figure 10 for each parameter. Also the frequency characteristic of the amplifier is shown in figure 11.

$$G_V = G_{m-v} \cdot \frac{1}{\frac{1}{R_{vo}} + \frac{1}{R_{eo1}} + j\omega C_{eo1} + \frac{1}{R_{eo2} + \frac{1}{j\omega C_{eo2}}}} \quad \cdots (9)$$



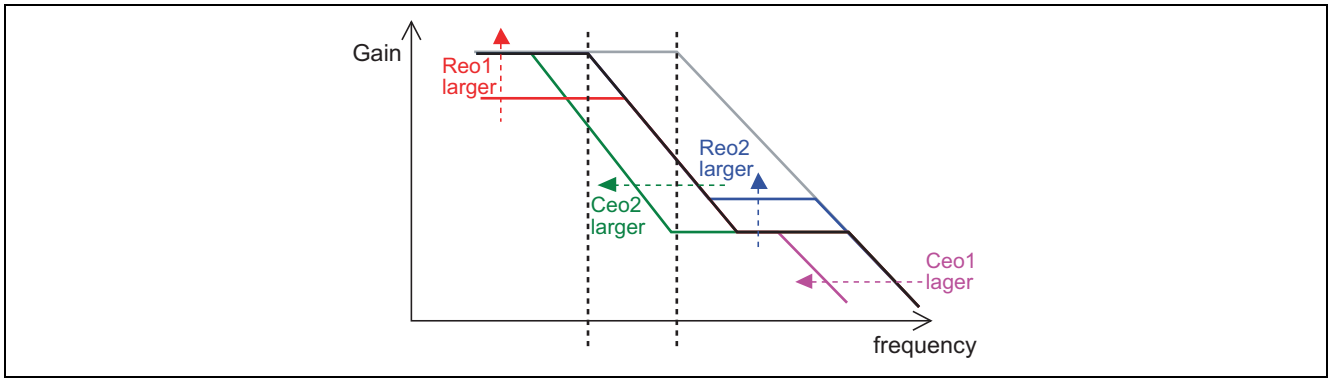


Figure 10 Output Gain Characteristics

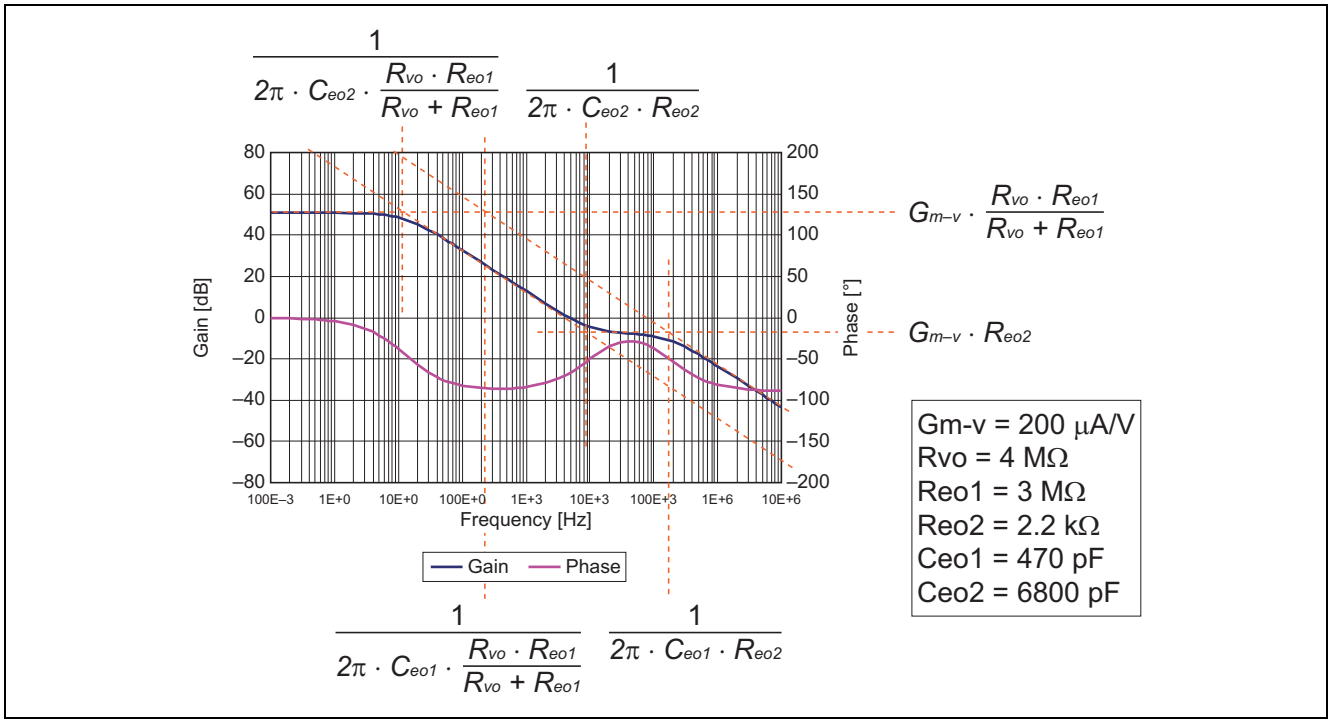


Figure 11 Error Amplifier Frequency Characteristics

Please confirm phase margin of the power supply by the Excel calculation seat for prepared for separately.

4.9 LTB (Load Tracing Boost) Setting

The components value of LTB (LTB components) is determined by the relation between load and the COMP voltage (V_{COMP}). LTB start point is approximately determined by emitter voltage of Q4 ($V_{Q4.E}$), Reo1-1 and Reo1-2, where Reo1-1 + Reo1-2 = Reo1, which can be determined according to the description on the previous page. We recommend to set $R_{B1} = R_{B2}$ (this means that VFB(+) value without taking account of LTB should be 2.5 V), and to set $V_{Q4.E}$ to around 1.3 V.

The LTB starting point is supposed to be determined as the turning point of half a load. However, It should be noticed that COMP voltage changes by Cramp and the boost inductor and input voltage level.

And also, other LTB components can be adjusted based on the values related to LTB stop point and the dropped voltage.

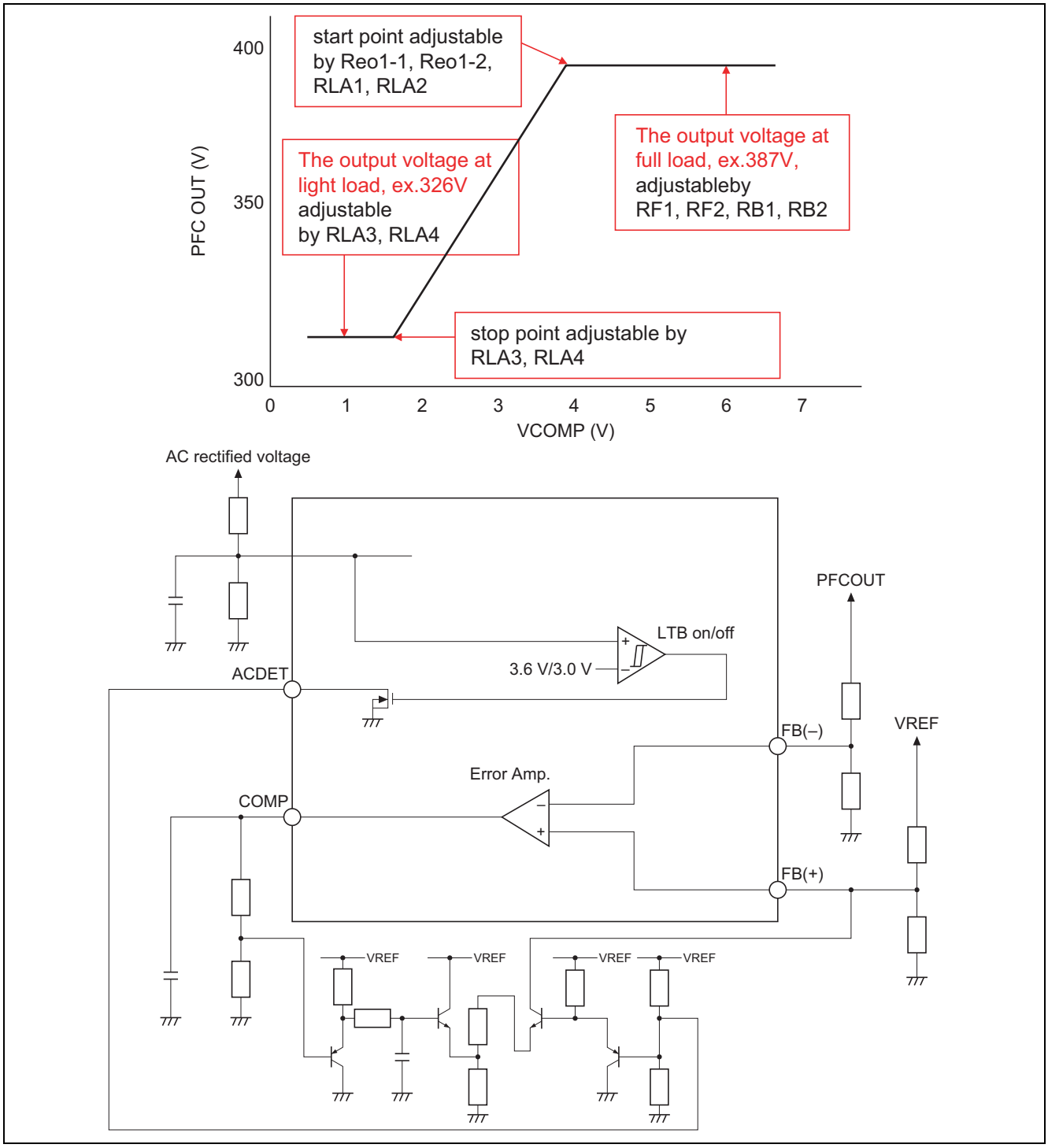


Figure 12

Output voltage at heavy load condition is determined as

$$V_{out(hevy\_load)} = \frac{R_{B2}\,(R_{F1} + R_{F2})}{(R_{B1} + R_{B2})\,R_{F2}} \cdot V_{REF}$$

Here, the value of R_{F1} must be less than or equal to 3 MΩ. And it is recommended to set the condition, $R_{B1} = R_{B2}$, namely VFB(+) = 2.5 V. Also, it is recommended that $V_{Q4.E}$ should be set to 1.3 V approximately to keep the linearity of LTB function. In addition, the value of R_{LA1} should satisfy the condition, $R_{LA1} > 20$ kΩ, in order that the operation can be stopped when 200 Vac is applied (as AC input voltage). By these conditions mentioned above, the relation between R_{LA1} and R_{LA2} is expressed in the next equation:

$$V_{Q3.E} = \frac{R_{LA2}}{R_{LA1} + R_{LA2}} \cdot V_{REF} \cong V_{FB(+)} - 1.2\ V \cong 1.3\ V$$

To accomplish LTB function, Reo1 is divided to two parts. One is Reo1-1, the other is Reo1-2, where Reo1-1 + Reo1-2 = Reo1. Then Start point of COMP voltage is described as follows. Vcomp(Start) is determined by application. But ordinary it approximately equal to half of Vcompmax (refer to the section, "4.3 RAMP Pin Capacitor"). Then we get Reo1-1 and Reo1-2.

$$V_{comp(Start)} = \frac{R_{eo1\text{-}1} + R_{eo1\text{-}2}}{R_{eo1\text{-}2}} \cdot V_{Q2.E} = \frac{R_{eo1\text{-}1} + R_{eo1\text{-}2}}{R_{eo1\text{-}2}} \cdot V_{Q4.E} \cong \frac{R_{eo1\text{-}1} + R_{eo1\text{-}2}}{R_{eo1\text{-}2}} \cdot V_{Q3.B}$$

$$= \frac{R_{eo1\text{-}1} + R_{eo1\text{-}2}}{R_{eo1\text{-}2}} \cdot \frac{R_{LA2}}{R_{LA1} + R_{LA2}} \cdot V_{REF}$$

In the same way, Vcomp(Stop) is approximately 20% of Vcompmax. Using following equation, we get the ratio of R_{LA3} to R_{LA4}.

$$V_{comp(Stop)} \cong \frac{R_{eo1\text{-}1} + R_{eo1\text{-}2}}{R_{eo1\text{-}2}} \cdot \frac{R_{LA4}}{R_{LA3} + R_{LA4}} \cdot V_{Q4.E} \cong \frac{R_{LA4}}{R_{LA3} + R_{LA4}} V_{comp(Start)}$$

To get the values of R_{LA3} and R_{LA4}, Vout(Light_load) is needed. This value is determined by application.

We get $R_{LA3} + R_{LA4}$ by following equation. Then R_{LA3} and R_{LA4} are obtained.

$$V_{out(Light\_load)} = \frac{R_{B2}(R_{F1} + R_{F2})}{(R_{B1} + R_{B2})R_{F2}} \cdot (V_{REF} - I_{Q4.C} \cdot R_{B1})$$

$$I_{Q4.C} = \frac{V_{Q4.E}}{R_{LA3} + R_{LA4}}$$

The values of Re1 and Re3 should be determined to avoid influence on the base currents of Q1, Q2. Namely, they should satisfy the condition described below:

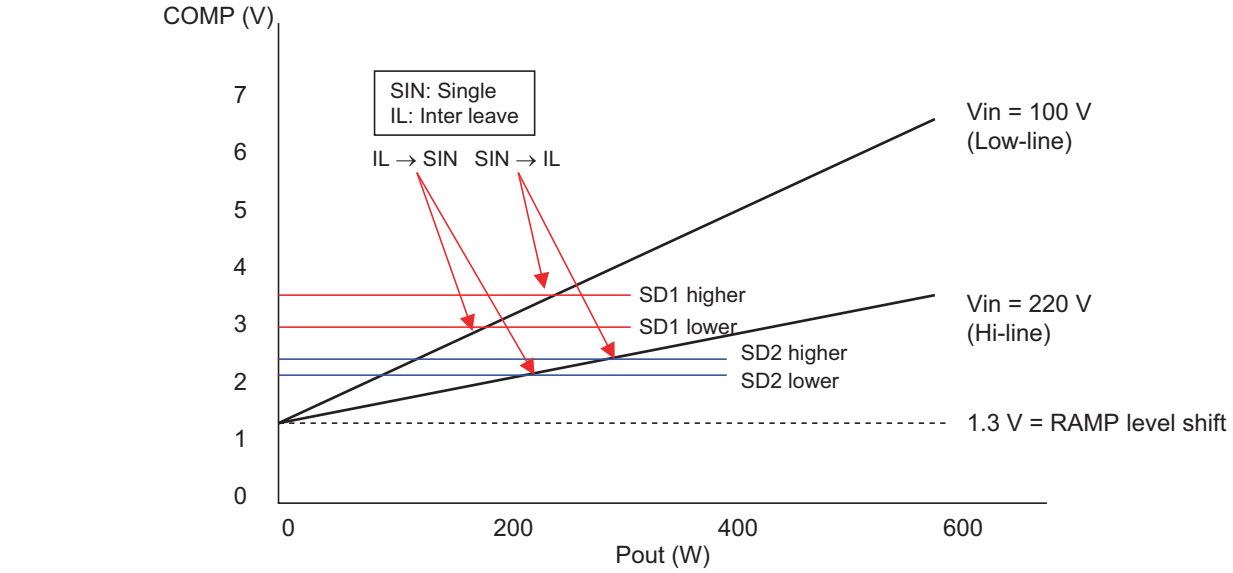
$I_{REO1} << I_{Re1}/hFE$ for $Q1$ and $I_{RLA2} << I_{Re2}/hFE$ for $Q3$

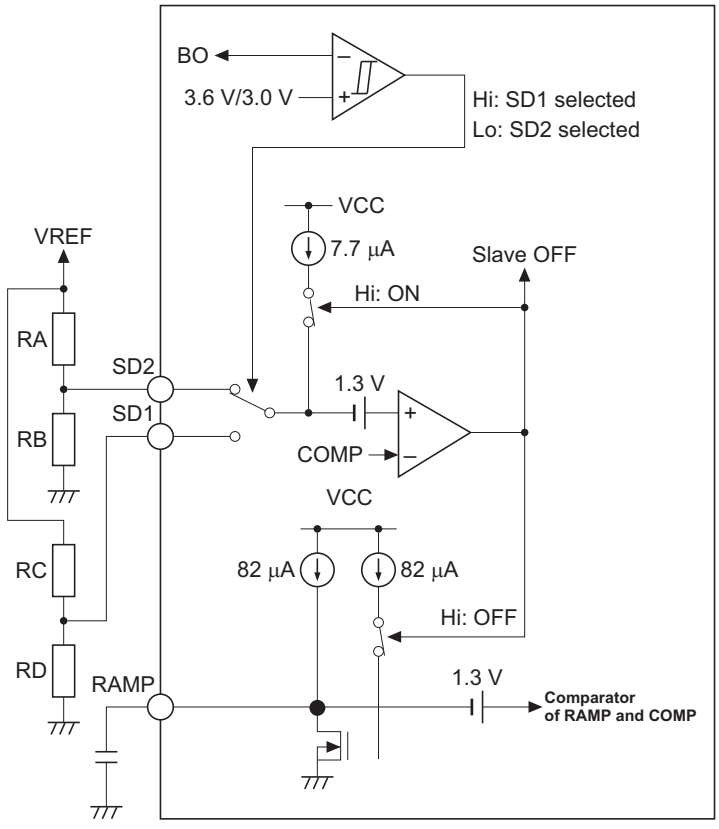
The response frequency of LTB should be much lower than the cut-off frequency of the feedback loop. The desirable cut-off frequency is 1 Hz. This frequency is adjustable with RLPF and CLPF.

4.10 SD (Slave Drop) Setting

The components determining the operation of SD should be set by the relation between load and the COMP voltage. SD point is adjusted by external resistor divider. Also two types of the SD points can be set individually as Hi line and Lo line.

The COMP voltage might include ripple voltage of input voltage frequency (ex.50 Hz), so the hysteresis voltage width should be enough to avoid malfunction by this ripple on COMP pin.





$$SD2lower = \frac{Vref}{RA + RB} \times RB + 1.3$$

$$SD2higher = \frac{RB}{RA + RB} (Vref + 7.7\ \mu A \times RA) + 1.3$$

If in the case of $Vref / (RA + RB) >> 7.7\ \mu A$,

$$\approx \left(\frac{Vref}{RA + RB} + 7.7\ \mu A \right) \times RB + 1.3$$

$$SD1lower = \frac{Vref}{RC + RD} \times RD + 1.3$$

$$SD1higher = \frac{RD}{RC + RD} (Vref + 7.7\ \mu A \times RC) + 1.3$$

If in the case of $Vref / (RC + RD) >> 7.7\ \mu A$,

$$\approx \left(\frac{Vref}{RC + RD} + 7.7\ \mu A \right) \times RC + 1.3$$

Figure 13

4.11 Brownout

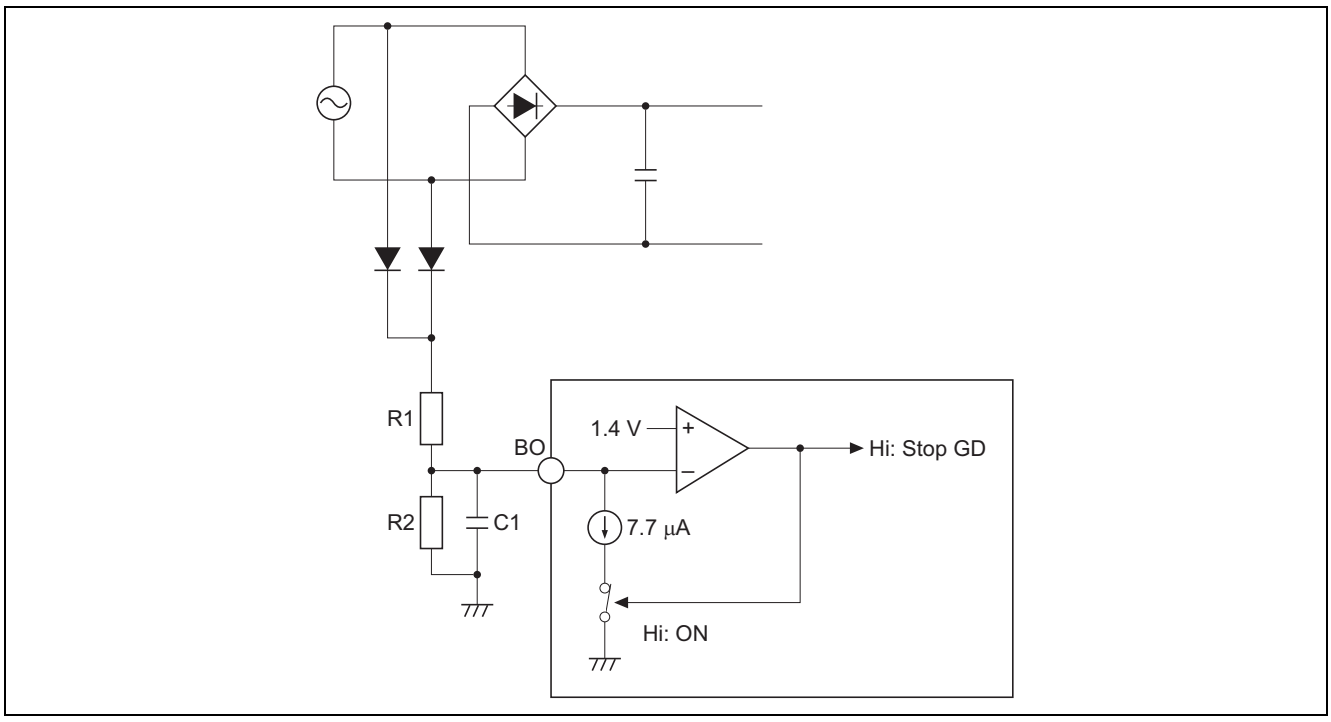


Figure 14

$$Von = \left[\frac{R1 + R2}{R2} \times 1.4\ V\right] \times \frac{\pi}{2\sqrt{2}} + R1 \times 7.7\ \mu A$$

$$Voff = \left[\frac{R1 + R2}{R2} \times 1.4\ V\right] \times \frac{\pi}{2\sqrt{2}}$$

Actual BO pin voltage Vbo is different from the result of these equations.

Because there is offset voltage on AC rectified voltage. And it varies by other conditions, such as load.

Therefore the external parts value should be to adjusted according to the result of measurement of an actual board.

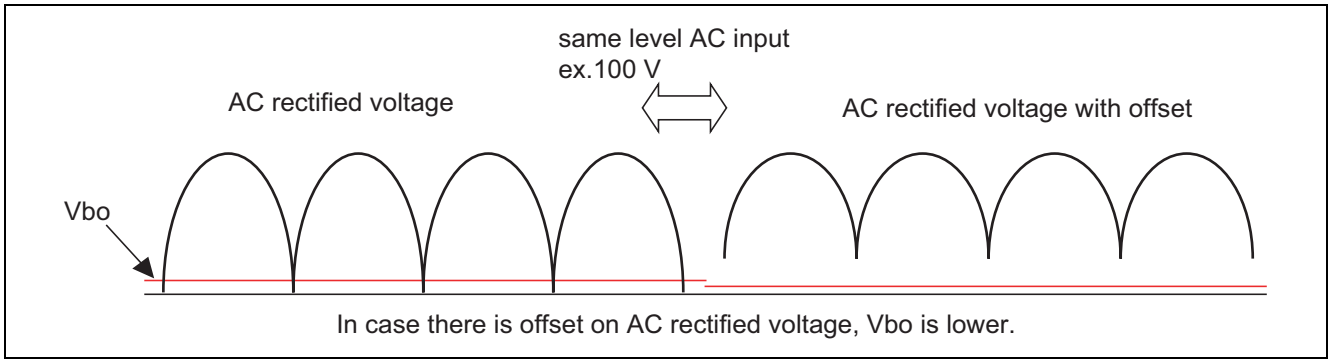


Figure 15

Table 1 Actual Voltage of R2A20132 Evaluation Board

R1 = 3 MΩ, R2 = 68 kΩ, C1 = 2.2 µF	
Von	78.5 V
Voff	69.1 V

4.12 OFF Time Control (OTC)

In case that Vcomp is very low, GD-M pulse width becomes shorter and as a result, switching frequency becomes higher. Consequently power loss might become higher. To avoid such a situation, OFF-time control (OTC) is effective. OTC operates as if Vcomp(min.) should be restricted to maintain high value. As a result, ON-time is fixed and OFF-time is controlled longer. Then switching frequency is kept still lower.

It is recommended on usage of OTC that Votc is set to 0.3 V initially and then it should be adjusted by the result of evaluating waveforms, efficiency, power factor etc..

4.13 Notice for PCB Layout

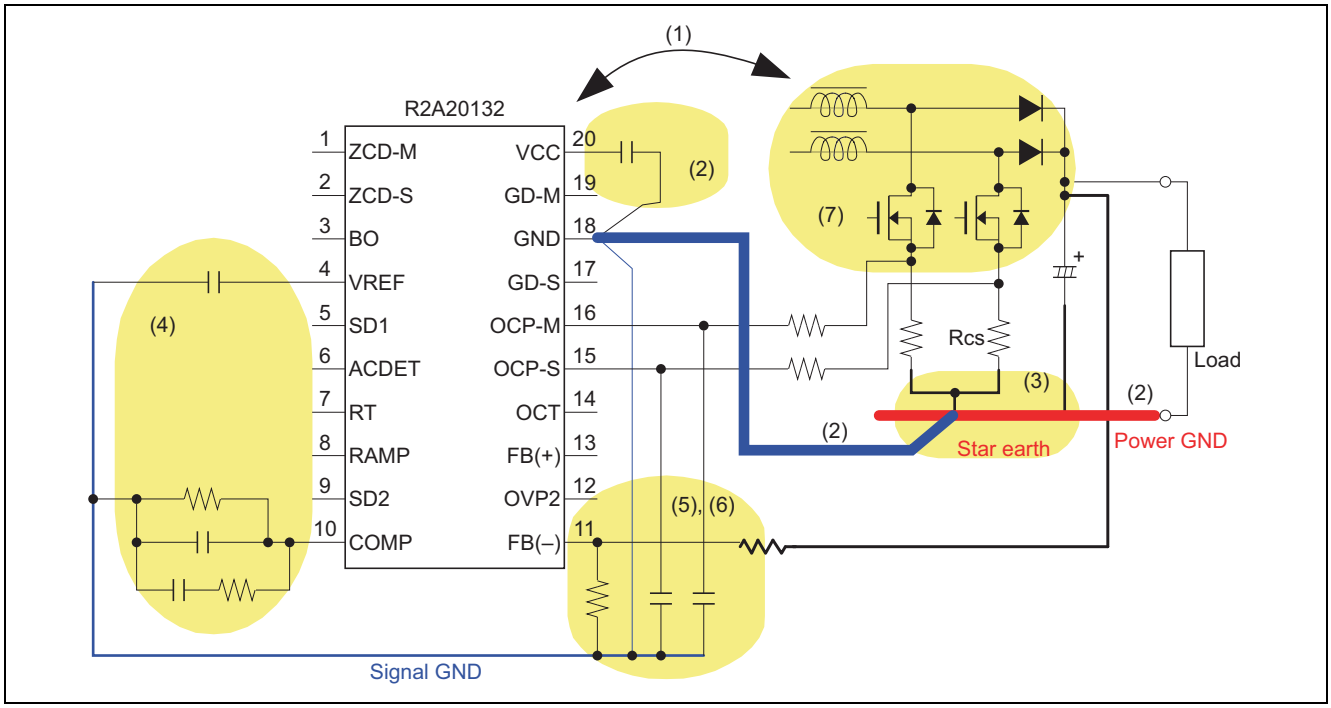


Figure 16

(1) Please make sure PFC IC be located as apart from power stage (MOSFET, DIODE, Boost L) as possible. Specially please be careful to MOSFET drain line layout to avoid radiation noise.
(2) Please separate the GND pattern of an output capacitor (Power GND) from the GND pattern of peripheral components of the IC (Signal GND) surely. And please connect the Signal GND to the GND terminal of the IC and then connect it and the Power GND to the GND side of the current detection resistor (Star Earth) with a single point connection. And also, please make the patterns of the Power GND and the Signal GND as large as possible.
(3) The GND side patterns of the current detection resistors RCS for both master and slave channels should be made as short as possible.
(4) Please place COMP/VREF external components as close to the IC pin as possible.
(5) Please place the filter for OCP-M, OCP-S and ZCD resistor as close to the IC as possible for avoiding radiation noise.
(6) Please place the FB(–) resistor as close to the IC as possible for avoiding radiation noise.
(7) The pattern for power stage (MOSFET, DIODE, Boost L) components should be designed as short as possible.

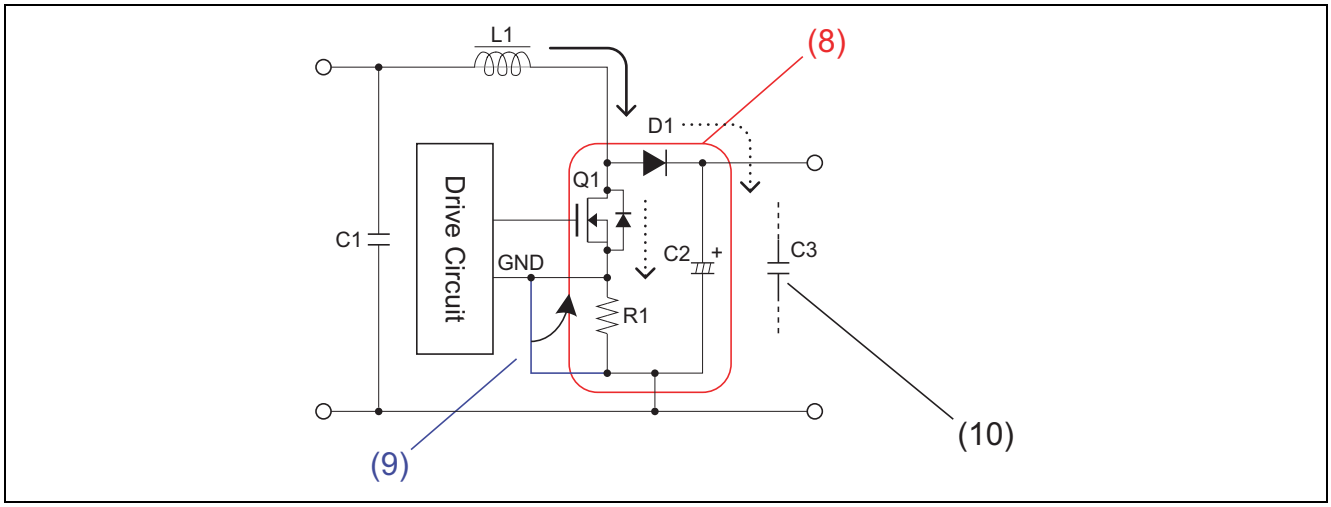


Figure 17

(8) It is possible to reduce MOSFET drain overshoot by making the pattern wide and short, on which discontinuous current flows.

(9) It is possible to improve the turn-off characteristics of the MOSFET(Q1) by connecting the return-GND of the drive circuit to the source terminal of the MOSFET(Q1) directly. However, the matter of surge noise also should be taken into account before deciding to implement this measure.

(10) If switching ripple voltage of output is too large, please place the film capacitor(C3) near the diode(D1). Please select the film capacitor of good high frequency characteristics.

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Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Jan 25, 2011	—	First edition issued

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
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Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
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7F, No. 363 Fu Shing North Road Taipei, Taiwan, R.O.C.
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1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
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