RAA215300 EEPROM Programming

The RAA215300 has a high endurance EEPROM to store all IC settings. This application note describes the minimal circuit requirements and steps to program and recall the EEPROM using an I^2C serial interface.

Contents

1. Introduction

The device features both volatile (registers) and non-volatile (EEPROM) memory. The value of each register can be set by writing data to the appropriate register using the selected interface, or it can be recalled and loaded from the EEPROM.

The EEPROM is partitioned into eight separate banks. All customer banks are programmed each time an EEPROM programming operation commences. For details of each register and bits, see the register map in the *RAA215300 Datasheet*.

For reference material, including the datasheet and supporting manuals, visit the RAA215300 and RTKA215300DE0000BU pages.

A Socket Evaluation Board and Graphical User Interface (GUI) are available from Renesas, and they can be used to program the EEPROM using the I^2C serial interface. See the *RTKA215300E00000BU Socket Evaluation Board Manual* and the *RAA215300 Evaluation Software Manual* for information regarding the socket evaluation board and GUI.

2. Handling Precautions

Take precautions to avoid electrostatic discharge (ESD) to the ICs. These include keeping ICs in protective packaging when possible, and connecting yourself and tools to earth when handling ICs.

Renesas recommends using a vacuum suction tool to lift and place the IC.

Do not apply power to the board when the socket is open. Do not open the socket when power is applied to the board.

Ensure correct orientation of IC. The IC is marked with an etched circle at pin 1.

Before closing the socket lid, ensure the IC is square and level in the socket. Failure to do so may result in damage to either or both the IC and socket.

3. Minimum Setup for EEPROM Programming

The minimum requirement for programming the EEPROM is for the device to be in {STANDBY}. However, the EEPROM can also be programmed in {ACTIVE} and {SLEEP} states.

To make the device enter {STANDBY} from an un-powered condition, apply power to AVDD and set CEN high. The EEPROM is read and the contents are loaded into the registers. Following a successful read and register loading, the internal VIO LDO is enabled. When VIO LDO completes power-up, the device enters {STANDBY} and can be controlled using an I^2C interface. For example, the customer registers can be read and set. For more information regarding operational states and the I^2C interface, see the *RAA215300 Datasheet*.

3.1 Circuit Diagram

The circuit shown in Figure 1 is only suitable for programming the EEPROM when the device is in {STANDBY}.

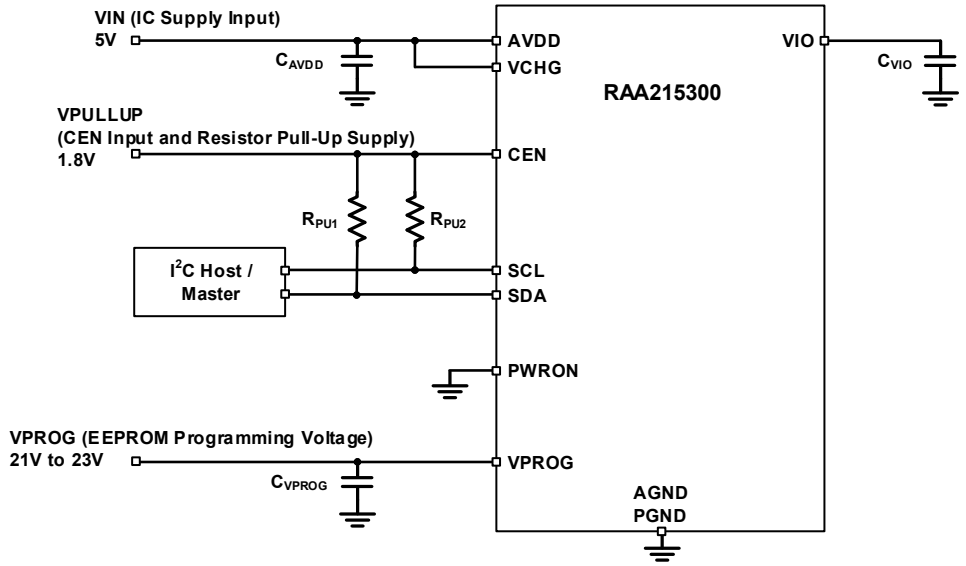

Figure 1. Minimum Circuit for EEPROM Programming

3.2 External Components

A small number of external components are required to power up the device in {STANDBY}. These are listed in Table 1. Capacitors for AVDD, VPROG, and VIO pins and pull-up resistors for the I^2C interface.

Table 1. External Components Required for EEPROM Programming

Name	Description	Key Electrical Specification	Imperial (Metric) Size
C_{AVDD}	Input capacitance for chip. Connect between AVDD and ground.	10µF±20%, 10V, X5R	0603 (1608)
C_{VIO}	Output capacitance for the internal LDO. Connect between VIO and ground.	2.2µF±10%, 10V, X5R	0402 (1005)
C_{VPROG}	Optional: Input capacitance for EEPROM Programming. Connect between VPROG and ground.	2.2µF±20%, 35V, X5R	0402 (1005)
R_{PU1} R_{PU2}	Pull-up resistance for the I^2C clock and data lines. Typical values for pull-up resistors are 1kΩ to 4.7kΩ depending on clock speed, pull-up voltage and bus capacitance. See the *RAA215300 Datasheet* for I^2C general operation.	1kΩ to 4.7kΩ	0402 (1005)

3.3 Supplies and Connections

The programming circuit Figure 1 shows three power supplies that are required for programming the EEPROM.

They are as follows:

- Power up the chip (VIN).
- Drive CEN and supply R_{PU1} and R_{PU2} pull-up resistors for the I^2C serial interface (VPULLUP).
- Provide the high voltage EEPROM programming supply (VPROG).

See Table 2 for pin details and connection.

Table 2. Pin Description and Connection for Minimal EEPROM Programming Setup

Pin	Pin Number	Description
AVDD	40	Analog and digital supply. AVDD and VCHG must be the same voltage. Connect to the VIN supply of 2.7V to 5.5V with a precautionary current limit of 500mA.
VCHG	31	Input Supply for VIO LDO. AVDD and VCHG must be the same voltage. Connect to VIN.
VIO	24	Internal 1.8V LDO output
CEN	47	Chip enable, active high. Connect to VPULLUP supply of 1.8V with a precautionary current limit of 100mA.
PWRON	52	Regulator output enable. Connect to ground.
VPROG	11	High voltage supply input for EEPROM programming. ⚠ See the warning in EEPROM Programming Steps. Apply the VPROG supply of 21V to 23V with a precautionary current limit of 100mA.
SCL	17	I^2C serial clock. Connect to R_{PU2} pull-up resistor.
SDA	18	Bi-directional I^2C serial data. Connect to R_{PU1} pull-up resistor.
AGND	26, 42	Analog and digital ground.
PGND	9	Power ground.
EPAD		Exposed thermal pad. Power ground. All regulator PGNDs are internally down bonded to the EPAD.

All other device pins should be left open when using the circuit of Figure 1.

4. EEPROM

4.1 EEPROM Programming Steps

WARNING! Do not hot-swap: Connecting or disconnecting a device to or from a powered-up circuit can cause damage to the device. All power supplies used for operating the device must be powered down and their outputs discharged before adding or removing a device to or from a circuit, including but not limited to: a test socket, a test harness, or a test jig.

Fast connection or fast disconnection of the power supply to VPROG can damage the PMIC.

The external, current limited power supply to VPROG must be increased from 0V to between 21V and 23V in no less than 1ms.

The external, current limited power supply to VPROG must be decreased from between 21V and 23V to 0V in no less than 1ms.

The following steps are the EEPROM programming sequence for {STANDBY}, {ACTIVE} and {SLEEP} states.

See the Handling Precautions.

1. Apply VIN (2.7V to 5.5V) to AVDD and VCHG.
2. Apply VPULLUP (1.8V) to CEN, and to the I^2C pull-up resistors.
   The device can now be controlled using the I^2C interface. For example, the customer registers can be read and set using I^2C.
3. ⚠ See the warning above. Apply the high voltage EEPROM programming supply (21V to 23V) to VPROG.
   The programming supply can be applied before configuring the customer registers. Writing to the EEPROM fails if the programming supply is less than 21V. This condition sets two EEPROM fault flags, see EEPROM Status Errors.
4. Write 0x02 to register 0xFF to set the write bit in the EEPROM control register.
   Wait for not less than the maximum EEPROM write time (t_{EE_WRITE}) to elapse before attempting additional I^2C activity. See the *RAA215300 Datasheet* for the t_{EE_WRITE} parameter.
5. Power down the high voltage EEPROM programming supply (VPROG).

   After a successful EEPROM write, the registers are loaded from the EEPROM. Read either a single register or all registers to confirm contents.

4.2 EEPROM Recall

EEPROM recall loads the contents of the EEPROM into the registers of the device.

When the EEPROM content is being loaded to the registers, the device is busy and any additional I^2C activity receives a Not Acknowledge (NACK).

There are two ways to recall the EEPROM:

- Automatic Recall – This occurs during initial power-on, power cycle or toggle of CEN. See the Operating {States} and Transition Conditions section of the datasheet.
- Manual/Software Recall – Issue an I^2C reset command to the control byte. Write 0x01 to register 0xFF (EEPROM control register).

4.3 EEPROM Error Correction

Data stored in EEPROM is protected by error correction codes (ECC), which allow a single bit error in a given memory bank to be corrected. Each EEPROM bank is covered by its own error correction code, correction status flag, and error status flag.

When an EEPROM bank is programmed, the error correction code for that bank is generated and stored in the same bank. If a single bit correction occurs, both the corresponding bank corrected status flag and the EEPROM fault flag (NVM Error) are set.

Two bit errors are reported as an uncorrectable error by setting both the corresponding bank error status flag and the EEPROM fault flag (NVM Error). The device ignores the other control inputs (for example, PWRON) and enters {FAULT_OUT} state.

The host can clear these fault bits by writing a 1 to the EEPROM fault flag, NVM Error, 0x5E[4].

For more detail regarding error correction and the EEPROM error correction registers, see the *RAA215300 Datasheet*.

4.4 EEPROM Status Errors

The device sets fault flags if errors are detected when programming the EEPROM. There are two EEPROM fault flags, NVM Error and EE Error. These flags are set for the following:

- Insufficient EEPROM programming voltage
- Corrected error
- Uncorrected error

See Table 3 for a description of when the two EEPROM error flags are set.

Table 3. EEPROM Error Fault Flags

Error Flag	Registor Bit	Setting
NVM Error	0x5E[4]	0: Normal Operation. 1: Insufficient EEPROM programming voltage or ECC error (Corrected or Uncorrected).
EE Error	0x85[0]	0: Normal operation. 1: Insufficient EEPROM programming voltage.

To clear these errors write a 1 to the NVM Error flag, 0x5E[4].

5. Revision History

Revision	Date	Description
1.01	Dec 19, 2022	Updated Table 2. Updated EEPROM Programming Steps section.
1.00	Jun 30, 2022	Initial Release

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