RC2121xA Monitoring and Diagnostic Features

This document describes the monitoring and diagnostic features for the RC2121xA (RC21211A, RC21212A, RC21213A, RC21214A) AutoClock devices.

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1. Introduction

This document is based on the RC2121xA datasheet and RC2121xA programing guide. Refer to these documents when using this application note.

The RC2121xA devices are not designed in compliance to ISO26262, however the RC2121xA devices have many monitoring functions that can be useful in safety applications.

The RC2121xA devices have the capability to enter an inactive state and to notify the system that it has entered this state via a fault pin. The assumption of use is that, during normal operations, monitor functions inside an RC2121xA device are used for diagnostic purposes only. Errors detected during POST (power-on self-test) will lead to the inactive state being maintained.

2. Assumptions of Use

Figure 1 shows the general assumed use case of an RC2121xA device for side-band connections. The RC2121xA devices provide a variety of clocks to the SoC (System-On-Chip) as well as clocks to several peripheral devices. The I^2C slave interface is connected to the SoC so that error information may be obtained. Interrupts are sent to the SoC.

Each error detected by an RC2121xA device can be programmed via an OTP (one-time programming) setting to generate either an interrupt to the SoC that can be used as warning condition, or an internal fault forcing the RC2121xA device to the inactive state.

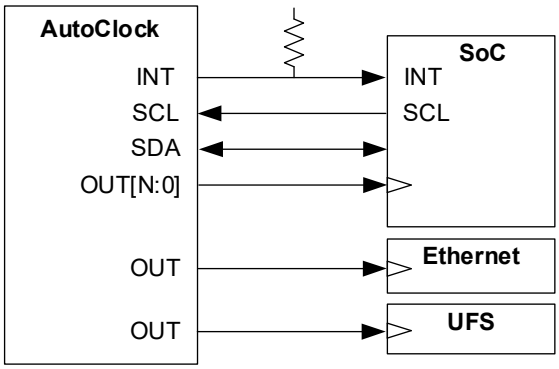

Figure 1. Assumed Use Case (Side-Band)

Figure 2 shows the clock detail. An RC2121xA device provides a variety of clocks to the SoC as well as clocks to several peripheral devices. The data path for the PCIe, Ethernet, and UFS is shown (other interconnects are possible). The main clock to the SoC (XTAL) is provided by a QM Oscillator. The clock used to monitor the main clock (XTALR) is provided by the RC2121xA device. This removes any common cause failures with the SoC clock monitor.

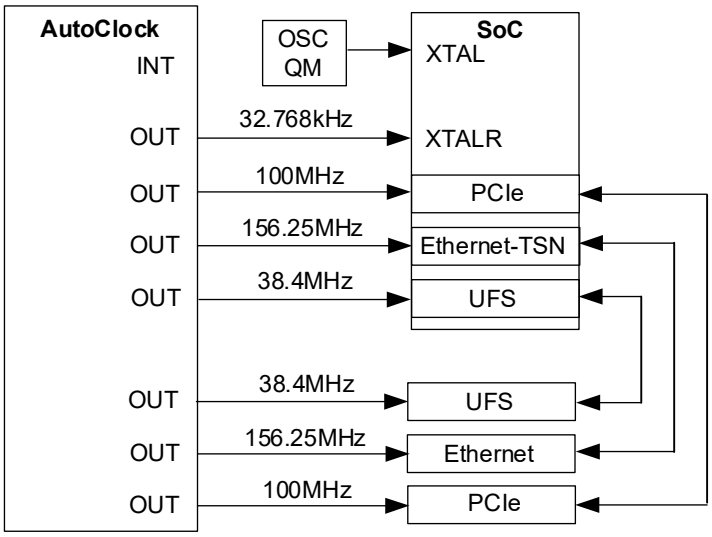

Figure 2. Assumed Use Case (Clocks)

Figure 3 shows the data path end-to-end protection detail for a single peripheral device. The assumed use case is that each high speed serial interface has end-to-end protection. Therefore, a bad clock from an RC2121xA device to either the SoC or the peripheral will be detected by the SoC. Additionally, an RC2121xA device has output clock monitoring.

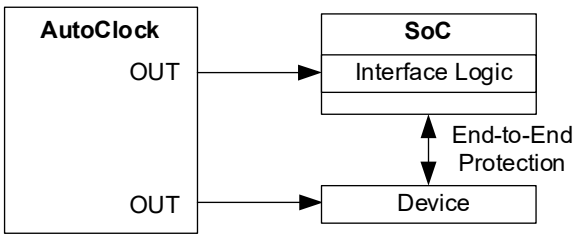

Figure 3. Assumed Use Case (End-to-End Protection)

The Assumptions of Use table (see Table 1) provides additional system integrators information regarding the assumptions taken, such as:

- Assumed requirements considered during the product development
- Assumed system measures to complement on-chip safety measures
- Assumptions considered during the safety analysis

If any of the assumptions considered during the safety analysis is different from the actual system use case, the implication to the FMEDA (Failure Modes Effects and Diagnostic Analysis) shall be considered.

Table 1. Assumptions of Use

AoU Number	Details
AoU 1	The system integrator shall ensure that the VDD supplies to an RC2121xA device are monitored for OV/UV (over-voltage/under-voltage).
AoU 2	The I^2C slave of an RC2121xA device is connected to the SoC, and CRC (cyclic redundancy check) is enabled on the interface.
AoU 3	The interrupt signal of an RC2121xA device is connected to the SoC.

AoU Number	Details
AoU 4	The system integrator shall ensure that the interrupt signal of an RC2121xA device is tested at startup.
AoU 5	The SoC derives its main clock from a QM Oscillator, and the monitoring clock for the SoC is provided by an RC2121xA device.
AoU 6	Serial interfaces (in other words, PCI Express, Ethernet, etc.) have end-to-end protection that will protect against out of specification clocks provided by an RC2121xA device.
AoU 7	An RC2121xA device FTTI (Fault Tolerant Time Interval) shall be assumed as 10ms, maximum. The system can optimize Detection Time depending on system requirements.
AoU 8	All error conditions are mapped to an interrupt (during normal operation).
AoU 9	When using two crystals they shall be within 200ppm of each other.
AoU 10	The system integrator shall ensure that the SoC reads the GPIO status register (GPIO_STS) to determine that the correct output enables (OEs) are applied to the GPIO pins configured as OE. For example, if GPIO 1 is configured as an OE and the SoC has asserted the OE via GPIO 1, then read back the state of GPIO 1 to confirm that an RC2121xA device received the signal.
AoU 11	The system integrator shall ensure that the SoC reads the GPIO startup status register (STARTUP_STS) to determine that the correct OTP image was loaded. Multiple images can be stored in the OTP. Reading back the gpio_at_startup field will indicate the pin state at startup and, therefore, which OTP image was loaded.
AoU 12	The system integrator shall ensure that the SoC reads the device event register (DEVICE_EVENT) to ensure that the OTP load was successful (in other words, otp_load_fail is not set).

3. General Notation and Terminology

This section describes the general notation and terminology used in this document.

These following words appearing in this document are always interpreted to indicate requirement levels as follows:

- **Shall**: Indicates that a method is highly recommended to fulfill the assumptions ("++" in this document indicates the same level)
- **Should**: Indicates that a method is highly recommended to fulfill the assumptions but strongly depends on user application ("+" in this document indicates the same level)
- **Can**: Indicates that multiple measures (including HW measures) are available to be used to fulfill the assumptions, and the proposed measure is one of them. ("o" in this document indicates the same level.)

4. Monitoring Functions

The RC2121xA devices support the system to achieve, or maintain, its safe state with the following capabilities:

- Indicating to the SoC on detection of an error
- Entering the safe state
- Aiding in diagnostics

5. Device States

The device sates are described in Figure 4. The powerup (P/U) state is entered when power is applied to the device. During the powerup sequence, all clock outputs are disabled. GPIO pins that are mapped to interrupt or FAULT are deasserted and shall be pulled high via external pull up resistors. If POST (power-on self-test) passes then normal operation resumes (in other words, active state is entered), outputs are enabled according to OE and register settings. If POST fails, then outputs remain disabled and the inactive state is maintained.

The only way to transition from an Inactive state to an Active state is via a successful POST (requires power cycling).

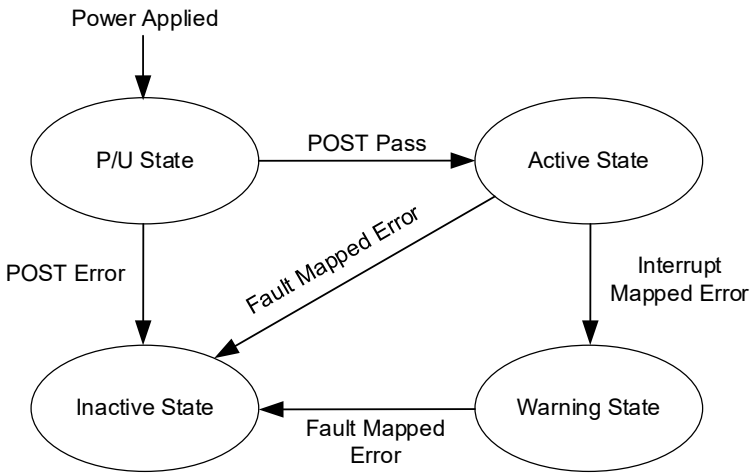

Figure 4. Device States

5.1 Powerup State

- All outputs are disabled
- Interrupt and Fault pins de-asserted
- Internal power-on reset de-asserts, device loads OTP, calibrates various analog circuits, and POST competes
- Next state is **Active** if POST passes, otherwise, it will be **Inactive** state.

5.2 Active State

- All outputs are enabled, according to OE pins and register control
- Interrupt and Fault pins de-asserted
- Next state is **Inactive** if an error condition is detected that is mapped to a Fault via OTP
- Next state is **Warning** if an error condition is detected that is mapped to an Interrupt via OTP

5.3 Inactive State

- All outputs are disabled
- Status registers indicate error condition
- Fault pin asserted (if defined)

5.4 Warning State

- Status registers indicate error condition.
- Interrupt pin asserted (if defined).
- Normal operation continues.
- Next state is **Inactive** if an error condition is detected that is mapped to a Fault via OTP

6. Monitoring Functions Summary

Table 2. Monitoring Functions Requirements

SM Number	SM Name	SM Description	Main Element	When	State[1]	Test Concept	Fault Detection and Response Time
SM 1a	LOL PW	Loss of Lock is detected on the APLL via pulse width.	APLL	Continuous[2]	Warning State	Monitor	< 20µs
SM 1b	LOL CV	Loss of Lock is detected on the APLL via control voltage.	APLL	Continuous[2]	Warning State	Monitor	< 20µs
SM 2	LOS	Loss of signal is detected at crystal input.	XTAL and OSC	Continuous[2]	Warning State	Monitor	< 1µs
SM 3	ppm	ppm difference exceeds programed value.	XTAL	Continuous[2]	Warning State	Monitor	10ms
SM 4	Short Term	Delta count between crystal and feedback clock	XTAL and OSC	Continuous[2]	Warning State	Monitor	2µs
SM 5	Output	Output frequency error is detected	Output dividers	Continuous[2]	Warning State	Monitor	10ms
SM 6	Register CRC	Soft errors detected in configuration registers	Registers	Continuous[2]	Warning State	Checker	10ms
SM 7	I^2C CRC	I^2C access have CRC protection	I^2C	When accessed	Warning State	Checker	5µs
SM 8	OTP CRC	OTP load is checked vs CRC	OTP	Startup	Inactive State	Checker	1 drive cycle
SM 9	APOST	Analog POST window compare on regulators	Internal regulators	Startup	Inactive State	Checker	1 drive cycle
SM 10	LPOST	Logic POST, LBIST and fault insertion	Logic	Startup	Inactive State	Checker	1 drive cycle

1. Warning state (interrupt mapped) is recommended for all continuous faults. This is set by OTP and maps the error condition to either fault mapped or interrupt mapped error (see Figure 4).
2. Continuous = during POST and during operation.

7. Monitoring Functions Details

7.1 SM1a: Pulse Width Detection: APLL Loss of Lock (LOL), SM1b: Control Voltage Detection: APLL Loss of Lock (LOL)

7.1.1 Overview

Loss of lock (LOL) on the APLL (Analog Phase-Locked Loop) is determined by two different mechanisms. The first mechanism is based on the pulse width of the charge pump. When the APLL is locked to the crystal these pules are very narrow. If they are wide then this indicates LOL.

The second mechanism looks at the control voltage on the VCO (voltage-controlled oscillator). If the control voltage is outside of the window compare, this indicates LOL.

Fault detection and response time interval is less than 20µs for either mechanism.

7.1.2 Hardware Description

The functional block diagram is shown in Figure 5. The phase comparator compares the phase of the crystal oscillator input and the divided down VCO. The output of the phase comparator is a signal which either pulses current into the loop filter or out of the loop filter. The loop filter smooths out these pules such that the input to the VCO is a stable voltage. The VCO then generates a frequency proportional to the DC voltage. The VCO output is divided down and fed into the phase comparator.

Mechanism SM1a contains an RC filter that smooths out the pulses and when the voltage is high enough and triggers a latch setting the LOL condition. Large pulses from the phase detector indicate LOL.

Mechanism SM1b is a window compare on the loop filter voltage. If the voltage is out of range, this indicates a LOL.

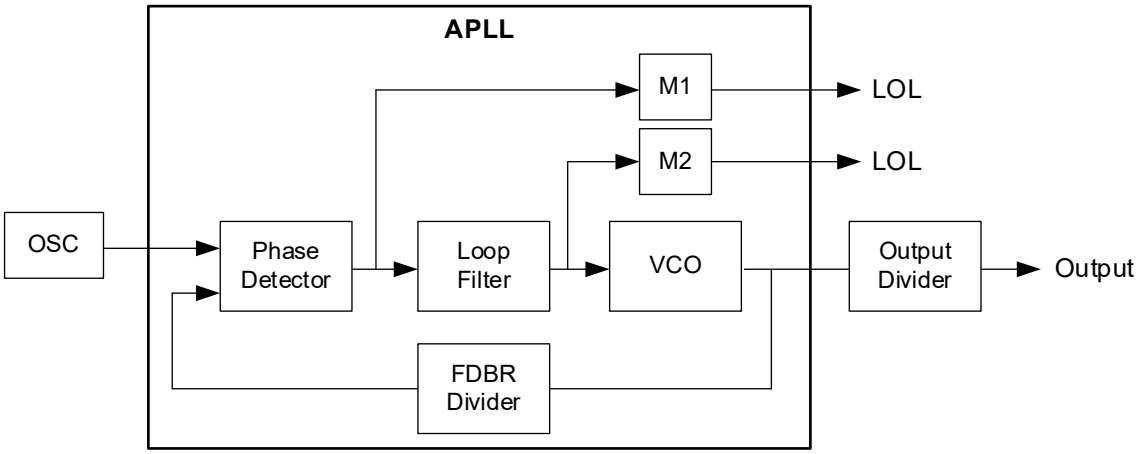

Figure 5. APLL LOL

7.1.3 Recommended Usage

This safety mechanism shall be active during powerup and during normal operation. During powerup it is masked for a few ms, allowing time for the APLL to lock to the crystal.

If the LOL is detected, this indicates that all output clocks may be operating at the wrong frequency.

7.1.4 Fault Control and Operation

When a LOL error is detected, the **apll_lo**l bit is set. The following shall be configured:

- LOL monitor shall be enabled via **apll_lol_mon_en**
- The error shall be mapped to an interrupt via **apll_lol_int_en**

7.1.5 Test Concept

During POST, an incorrect value is programed into the feedback divider in the APLL. This will force a LOL.

7.2 SM2: Loss of Signal on Crystal Inputs

7.2.1 Overview

Loss of signal (LOS) on each crystal input is detected via oversampling the crystal input with an internal high speed clock. If high to low or low to high transitions do not occur at the expected number of over sampled clock ticks, LOS is determined.

Fault detection and response time interval is less than the period of the crystal. For a typical 50MHz crystal, DTI (diagnostic test interval) is less than 20ns.

7.2.2 Hardware Description

Loss of signal on the crystal input is sampled by a divided down clock from the VCO. The VCO is typically programed for 10GHz operation. The VCO is divided down by 16 to ~625MHz. The divided down VCO clock is used to count the 1/2 period of the crystal input. LOS determination is made every 1/2 period.

When a two-variant crystal is used and the primary crystal fails (in other words, LOS is set), and the other crystal is switched in, it is working (in other words. not LOS). This switch is non-revertive.

7.2.3 Recommended Usage

This safety mechanism shall be active during powerup and during normal operation. When a single crystal variant is used, the OTP setting shall map the LOS to an interrupt.

When two crystal variants are used, the OTP setting shall map both crystals LOS to an interrupt and dual crystal fail to an interrupt (in other words, when both crystals fail).

7.2.4 Fault Control and Operation

When an LOS is detected, the **los[1:0]_evt** bits are set. The following shall be configured:

- LOS monitor shall be enabled via **los_mon_en**
- The error shall be mapped to an interrupt via **los_int_en**

When a dual crystal variant is used, the following shall be configured:

- Automatic crystal switching mode selected via **xtal_sel_mode** = 0x2.
- Crystal switch event is enabled via **xtal_switch_mon_en**
- The crystal switch event (**xtal_switch**) shall be mapped to an interrupt via **xtal_switch_int_en**
- The dual crystal failure monitor shall be enabled via **dual_xtal_fail_mon_en**
- The dual crystal failure event (**dual_xtal_fail**) shall be mapped to an interrupt via **dual_xtal_fail_int_en**

7.2.5 Test Concept

During POST, the monitor is configured to expect a transition every oversampled clock tick. This causes the error condition to assert.

7.3 SM3: PPM Error Between Crystals

7.3.1 Overview

The ppm error is determined via two 19-bit counters. This is only applicable to variants with two crystals. Fault detection and response time interval is 10ms for a 50MHz crystal.

7.3.2 Hardware Description

Each crystal clocks a 19-bit counter. The first counter to reach the terminal count of 500,000 stops both counters. The difference between the counters is two 2ppm per LSB (least significant bit). If this difference is greater than the OTP setting for warning or error, the respective error is generated.

7.3.3 Recommended Usage

This safety mechanism shall be active during power up and during normal operation. When a single crystal variant is used, this safety mechanism is not used.

When a two-crystal variant is used, both the warning and error thresholds shall map this error to an interrupt.

7.3.4 Fault Control and Operation

When a ppm error or warning is detected, the **xtal_ppm_err** or **xtal_ppm_warn** bit is set respectively. The following shall be configured:

- ppm error monitor shall be enabled via **xtal_ppm_err_mon_en**
- ppm warning monitor shall be enabled via **xtal_ppm_warn_mon_en**
- The error shall be mapped to an interrupt via **xtal_ppm_err_int_en**
- The warning shall be mapped to an interrupt via **xtal_ppm_warn_int_en**

7.3.5 Test Concept

During POST, the crystal clock 0 is gated while the ppm warning threshold is set to confirm that the ppm warning will assert. During a separate POST test, the crystal clock 1 is gated while the ppm error threshold is set to confirm that the ppm error will assert.

7.4 SM4: Short-term Monitor

7.4.1 Overview

The short-term monitor counts rising edges of both crystal inputs and the feedback clock during a monitor window. If the count difference between a crystal and the feedback (delta count) exceeds a threshold, then that crystal has failed.

7.4.2 Hardware Description

The typical configuration for a 50MHz crystal is to count 100 crystal periods, or 2µs. Due to the low-pass filter of the APLL, the VCO frequency will not track a sudden change in crystal frequency in 2µs. The VCO frequency can be considered constant over the 2µs interval.

The delta count is calculated for each crystal continuously. If the absolute |delta count| for a crystal exceeds the threshold, then the crystal has failed.

When a two crystal variant is used and the primary crystal fails, the backup crystal is switched in, if the backup crystal is working. This switch is non-revertive.

7.4.3 Recommended Usage

This safety mechanism shall be active during powerup and during normal operation.

7.4.4 Fault Control and Operation

When a short term error is detected, the **xtal[1:0]_st_err** bit is set. The following shall be configured:

- Short term monitor enabled via **xtal_st_err_mon_en**
- The error shall be mapped to an interrupt via **xtal_st_err_int_en**
- Short term monitor configured via ST_CNFG register; maximum and minimum thresholds are set to the same value.

When a dual crystal variant is used the following shall be configured:

- Automatic crystal switching mode selected via **xtal_sel_mode** = 0x2.
- Crystal switch event is enabled via **xtal_switch_mon_en**
- The crystal switch event (**xtal_switch**) shall be mapped to an interrupt via **xtal_switch_int_en**
- The dual crystal failure monitor shall be enabled via **dual_xtal_fail_mon_en**
- The dual crystal failure event (**dual_xtal_fail**) shall be mapped to an interrupt via **dual_xtal_fail_int_en**

7.4.5 Test Concept

During POST, the crystal clock 0 is gated. This causes the short-term error to assert for crystal 0 and when crystal clock 1 is gated, a short-term error is asserted for crystal 1.

7.5 SM5: Output Frequency Monitor

7.5.1 Overview

Each output is monitored for correct output frequency in a round-robin technique.

7.5.2 Hardware Description

Each output is typically configured to check its output frequency in a 1ms window (for output frequencies of 10MHz or greater; slower outputs may require a longer window), based on the selected input crystal. The selected input crystal is the crystal that the APLL is currently locked to. For example: with a 50MHz crystal, **freq_fast_window** would be set to 50,000.

Each output is selected in a round-robin technique. The selected output increments a counter for the duration of the timing window. The count is compared to two thresholds and the count must be between the two thresholds. The thresholds are configured per output bank rather than by output pin.

During POST, the output monitors operate on the pre-drivers, rather than the actual output driver, as the outputs cannot be turned on until power-on is complete and the appropriate enables have been asserted. A fixed divide ratio of 100 is used during POST.

7.5.3 Recommended Usage

This safety mechanism shall be active during power up and during normal operation.

7.5.4 Fault Control and Operation

When an output clock frequency error is detected, the **freq[11:0]_evt** bit is set. The following shall be configured:

- Output frequency monitor configured via **FREQMON_THRESH** and **FREQ_WINDOW_CNFG**
- Enable true and compliment clocks outputs for monitoring via **FREQ_CLOCK_SEL**
- Output frequency monitor enabled via **freq_mon_en**
- The error shall be mapped to an interrupt via **freq_int_en**

7.5.5 Test Concept

During POST, the thresholds/window size shall be set in **POST_FREQMON_CNFG** such that the error condition will assert.

7.6 SM6: Register Signature CRC

7.6.1 Overview

The configuration registers are checked for soft errors via calculating a 32 bit “signature” CRC across all configuration registers and comparing to a 32-bit CRC value.

7.6.2 Hardware Description

Every 10ms, hardware reads the configuration registers and computes the CRC based on the read sequence and compares to the pre-calculated signature.

7.6.3 Recommended Usage

This safety mechanism shall be active during power up and normal operation.

7.6.4 Fault Control and Operation

When a Signature CRC error is detected, the **csr_sig_fail** bit is set. The following shall be configured:

- The signature monitor shall be enabled via **csr_sig_fail_mon_en**
- The error shall be mapped to an interrupt via **csr_sig_fail_int_en**
- The signature monitor shall be enabled via **csr_sig_timer**

7.6.5 Test Concept

Signature CRC is tested at startup by bit-wise inverting the expect CRC value.

7.7 SM7: I²C CRC

7.7.1 Overview

The I²C serial interface has a CRC checker. Each read and write between the SoC and AutoClock is checked via an 8-bit CRC, $x^8 + x^2 + x^1 + 1$.

7.7.2 Hardware Description

Writes to the RC2121xA devices are checked for correct CRC. If the CRC is incorrect, the write is discarded. It is the responsibility of the SoC to check for correct CRC on reads.

7.7.3 Recommended Usage

This safety mechanism shall be active during normal operation.

7.7.4 Fault Control and Operation

When an I²C CRC error is detected, the **i2c_crc_err** bit is set. The following shall be configured:

- I²C CRC monitor enabled via **i2c_crc_err_mon_en**
- The error shall be mapped to an interrupt via **i2c_crc_err_int_en**

7.7.5 Test Concept

I²C CRC is tested at startup via LBIST.

7.8 SM8: OTP CRC

7.8.1 Overview

During OTP read, the image is checked for 32-bit CRC.

7.8.2 Hardware Description

The OTP loader checks the data it reads from OTP against the 32-bit CRC. The 32-bit CRC is the last element of a block. If the CRC does not match, then the loader retries up to 3 times. If it fails the 4th time, then the device enters the inactive state and all clock outputs remain disabled. Clock outputs are aways disabled during OTP load.

7.8.3 Recommended Usage

This safety mechanism shall be active during power up.

7.8.4 Fault Control and Operation

When an OTP CRC error is detected, the **otp_crc_err** bit is set.

When an OTP load error is detected, the **otp_load_fail** bit is set.

7.8.5 Test Concept

OTP CRC is tested at startup via LBIST.

7.9 SM9: Analog POST

7.9.1 Overview

Analog POST checks all internal voltage regulators for the correct voltage.

7.9.2 Hardware Description

During power-on self-test (POST), each regulator voltage (nominal 1.2V) is checked via a window compare in a round-robin technique. If the voltage is outside of the compare window, an error is flagged.

7.9.3 Recommended Usage

This safety mechanism shall be active during powerup.

7.9.4 Fault Control and Operation

When an error is detected, the **post_fail** bit is set. The following shall be configured:

- The POST monitor shall be enabled via **post_fail_mon_en**
- The error shall be mapped to a fault via **post_fail_fault_en**
- The error shall trigger the inactive state via **post_fail_action_en**

7.9.5 Test Concept

During POST, the window compare thresholds are modified such that the error condition will assert.

7.10 SM10: Digital POST

7.10.1 Overview

Digital POST includes LBIST, as well as fault insertion to check that the various monitors will detect an error condition.

7.10.2 Hardware Description

Fault insertion injects an error into each monitor and checks that the error is detected. The following summarizes the method for each monitor:

- **LOL**: The feedback divider is programmed with an incorrect value which causes a LOL on the APLL. The VCO has a very narrow range and will be unable to lock when the feedback divider is programed with an incorrect value.
- **LOS**: The LOS count is set to a low number (1), such that the next crystal edge is not found which causes a LOS. Normally it takes 5–6 ticks to see an edge with 50MHz crystal.
- **PPM**: The clock is gated from XTAL 0 for the warning threshold and gated from XTAL 1 for the error threshold. When one crystal is gated, the ppm error will be high and will fail. Applies to dual-crystal only.
- **Short-term**: The clock is gated from each crystal, in turn. This causes a difference between the feedback clock counter and crystal clock counter.
- **Output frequency**: The minimum and maximum thresholds are set such that every output frequency will fail.
- **XTAL switching**: LOS is generated on the primary crystal, forcing a crystal switch. Dual-crystal only.
- **Signature CRC**: An inverted CRC is written into the expected CRC register.

7.10.3 Recommended Usage

This safety mechanism shall be active during powerup.

7.10.4 Fault Control and Operation

When an error is detected, the **post_fail** bit is set. The following shall be configured:

- The POST monitor shall be enabled via **post_fail_mon_en**
- The error shall be mapped to an fault via **post_fail_fault_en**
- The error shall trigger the inactive state via **post_fail_action_en**

7.10.5 Test Concept

Digital BIST checks the logic via LBIST and fault insertion.

8. Revision History

Revision	Date	Description
1.00	May 8, 2024	Initial release.

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