RH850/U2A-EVA Group

SAN Sample Program List

Introduction

This document explains the sample programs of safety mechanisms for RH850/U2A-EVA Group.
This document note is made based on the RH850/U2Ax SAN.

Disclaimer

Aim of this document and software is to provide supplemental information for the function on RH850/U2A. It is not intended to implement in the design for mass production.
There is no guarantee to update in this document and software to reflect the latest manual, errata, technical update and development environment. You are fully responsible for the incorporation or any other use of the information of this document in the design of your product or system, and please refer to latest manual, errata, technical update and development environment.

Target Device

- RH850/U2A-EVA Group

Target integrated development environment

CS+ (by Renesas Electronics Corporation)
Version : V.8.07.00
Device file : DR7F702300.DVF
DR7F702301.DVF
DR7F702302.DVF

Reference Document

The User's Manual provides information about functional and electrical behavior of the device.
At the release time of this application note the following manual version available:
RH850/U2A-EVA Group User's Manual : Hardware (Rev1.20): R01UH0864EJ0120
RH850/U2Ax SAN (Rev2.00): R01AN5390EJ0200

Contents

1. Sample program list....3

Revision History....9

1. Sample program list

RH850/U2Ax SAN		Sample Program	
Chapter	SAN ID	Folder Name	Description
3.2 Memory Protection Unit (MPU)	SW self-test for MPU [SAN-U2Ax-0301-401]	3_2_1_memoryprotectionMDP	This sample program is for **MPU** software self-test by using **MDP exception**, checking whether MDP exception occurs when CPU does read access to memory area protected by MPU. For detail flow, please refer to ***RH850/U2Ax SAN Section 3.2.3.2 SW Test procedure***. **NOTE**: This sample program can be used as a reference for the following error injection. ・**MPU** software self-test by using **MIP exception** (For detail flow, refer to ***RH850/U2Ax SAN Section 3.2.3.2 SW Test procedure***.) For detail of the differences between MDP exception and MIP exception, please refer to ***RH850/U2A-EVA User's Manual : Hardware***.
3.3 Processor Element Guard (PEG)	SW self-test for PEG [SAN-U2Ax-0302-401]	3_3_1_processElementGuard	This sample program is for **PEG** software self-test by using **PEG error**, checking whether PEG error occurs when sDMAC does access to memory area protected by PEG. For detail flow, please refer to ***RH850/U2Ax SAN Section 3.3.3.2 SW Test procedure***. **NOTE**: This sample program can be used as a reference for the following error injection. ・**CRG error** injection (For detail flow, refer to ***RH850/U2Ax SAN Section 3.4.3.2 SW Test procedure***.) ・**CSG error** injection (For detail flow, refer to ***RH850/U2Ax SAN Section 3.4.3.2 SW Test procedure***.) ・**INTC2 Guard error** injection (For detail flow, refer to ***RH850/U2Ax SAN Section 3.5.3.2 SW Test procedure***.) ・**DTS Guard error** injection (For detail flow, refer to ***RH850/U2Ax SAN Section 3.6.3.2 SW Test procedure***.) ・**sDMAC Guard error** injection (For detail flow, refer to ***RH850/U2Ax SAN Section 3.7.3.2 SW Test procedure***.) ・**IBG error** injection (For detail flow, refer to ***RH850/U2Ax SAN Section 3.8.3.2 SW Test procedure***.) ・**PBG error** injection (For detail flow, refer to ***RH850/U2Ax SAN Section 3.9.3.2 SW Test procedure***.) ・**HBG error** injection (For detail flow, refer to ***RH850/U2Ax SAN Section 3.10.3.2 SW Test procedure***.) For detail of the differences between PEG error and the above error, please refer to ***RH850/U2A-EVA User's Manual : Hardware*****.**
5. Window Watchdog Timer (WDTB)	WDTBA SW Test procedure [SAN-U2Ax-0500-402]	5_1_2_WatchdogTimer	This sample program is for **WDTBA** software self-test by using WDTBA reset, checking whether WDTBA reset occurs when WDTBA counter overflows. For detail flow, please refer to ***RH850/U2Ax SAN Section 5.4.2 SW Test procedure, WDTBA SW Test procedure***. **NOTE**: This sample program can be used as a reference for ***U2Ax SAN Section 5.4.2 SW Test procedure, WDTBA SW Test procedure [SAN-U2Ax-0500-403].***
6. Built-In-Self-Test (BIST)	Standby-Resume BIST [SAN-U2Ax-0602-402]	6_3_2_Standby_Resume_BIST_TAUJ	This sample program is for **Standby-Resume BIST** software self-test. For detail flow, please refer to ***RH850/U2Ax SAN Section 6.3.4.2 SW test procedure, Standby-Resume BIST [SAN-U2Ax-0602-402]***.
7.2 Code Flash ECC and Address Parity	ECC decoder and address parity checker test for Code Flash memory [SAN-U2Ax-0701-401]	7_2_1_CodeFlashEccandAddressParity_N1_all	This sample program is for **Code Flash** software self-test by using Code Flash ECC error 1bit error , 2bit error and Address Parity error, checking whether this ECC error occurs when CPU0 does read access to Code Flash ECC Test Area of Bank A. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.2.4.2 SW Test procedure, ECC decoder and address parity checker test for Code Flash memory***.
	ECC decoder test for data access in PEs and Global FLASH Bus [SAN-U2Ax-0701-402]	7_2_4_CodeFlashEccandAddressParity_N4	This sample program is for **Code Flash (Global Area)** software self-test by using Code Flash ECC 1bit error, checking whether this ECC error occurs when **CPU0** does read access to Code Flash ECC Test Area of Global Area. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.2.4.2 SW Test procedure, ECC decoder test for data access in PEs and Global FLASH Bus***. **NOTE**: This sample program can be used as a reference for **ECC 2bit error injection**.
		7_2_6_CodeFlashEccandAddressParity_N6	This sample program is for **Code Flash (Global Area)** software self-test by using Code Flash ECC 1bit error, checking whether this ECC error occurs when **DTS** does read access to Code Flash ECC Test Area of Global Area. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.2.4.2 SW Test procedure, ECC decoder test for data access in PEs and Global FLASH Bus***. **NOTE**: This sample program can be used as a reference for ECC 2bit error injection.
	ECC decoder test for instruction fetch in PEs [SAN-U2Ax-0701-403]	7_2_8_EccDecoder1b	This sample program is for **Code Flash (Global Area)** software self-test by using Code Flash ECC 1bit error, checking whether this ECC error occurs when CPU0 does **instruction fetch** to Code Flash ECC Test Area of Global Area. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.2.4.2 SW Test procedure, ECC decoder test for instruction fetch in PEs***.

RH850/U2Ax SAN		Sample Program	
Chapter	SAN ID	Folder Name	Description
			NOTE: This sample program can be used as a reference for ECC 2bit error injection.
7.3 Data Flash ECC	ECC decoder test of Data Flash [SAN-U2Ax-0702-401]	7_3_1_DataFlashEccCrcCheck	This sample program is for **Data Flash** software self-test by using Data Flash ECC 1bit error, checking whether this ECC error occurs when CPU0 reads Data Flash that is injected the error. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.3.4.2 SW Test procedure, ECC decoder test of Data Flash***. **NOTE**: This sample program can be used as a reference for ECC 2bit error injection.
7.4 Local RAM ECC and Address Feedback	RAM failure mode classification SW procedure (data fault/address fault) [SAN-U2Ax-0703-401]	7_4_1_dataaddressfault	This sample program is for **LRAM** failure mode classification SW procedure (data fault/address fault). For detail flow, please refer to ***RH850/U2Ax SAN Section 7.4.4.2 SW Test procedure, RAM failure mode classification SW procedure (data fault/address fault)***. **NOTE**: This sample program can be used as a reference for the following SW flows. ・**CRAM** failure mode classification (For more detail, refer to ***RH850/U2Ax SAN Section 7.5.4.2 SW Test procedure, RAM failure mode classification SW procedure (data fault/address fault)***.) ・**DTS RAM** failure mode classification (For more detail, please refer to ***RH850/U2Ax SAN Section 7.7.4.2 SW Test procedure, RAM failure mode classification SW procedure (data fault/address fault)***.) For detail of the differences between LRAM error and the above RAM error, please refer to ***RH850/U2A-EVA User's Manual : Hardware***.
	Write Verify Test: [SAN-U2Ax-0703-402-NoLink]		This sample program is for **LRAM** Write Verify Test. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.4.4.2 SW Test procedure***, Write Verify Test. **NOTE**: This sample program can be used as a reference for the following SW flows. ・**CRAM** Write Verify Test (For more detail, refer to ***RH850/U2Ax SAN Section 7.5.4.2 SW Test procedure, Write Verify Test***.) ・**DTS RAM** Write Verify Test (For more detail, refer to ***RH850/U2Ax SAN Section 7.7.4.2 SW Test procedure, Write Verify Test***.) For detail of the differences between LRAM error and the above RAM error, please refer to ***RH850/U2A-EVA User's Manual : Hardware***.
	Self-Diagnosis for ECC decoder [SAN-U2Ax-0703-403]	7_4_3_lramSelfDiagnosisEccdecoder_item3	This sample program is for **LRAM** software self-test by using ECC 1bit error, checking whether this ECC error occurs when CPU does read access to LRAM that is injected the error. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.4.4.2 SW Test procedure, Self-Diagnosis for ECC decoder***. **NOTE**: This sample program can be used as a reference for "LRAM's ECC 2bit error injection" and "the following ECC 1bit and 2bit error injection". ・**CRAM** ECC error injection (For more detail, refer to ***RH850/U2Ax SAN Section 7.5.4.2 SW Test procedure, Self-Diagnosis for ECC decoder.***) For detail of the differences between LRAM ECC error injection and the above ECC error injection, please refer to ***RH850/U2A-EVA User's Manual : Hardware***.
	Self-Diagnosis for the address feedback [SAN-U2Ax-0703-404]	7_4_5_lramSelfdiagnosisforaddressfeedback	This sample program is for **LRAM** software self-test by using LRAM address feedback error, checking whether address feedback error occurs when CPU does access to LRAM that is injected the error. For detail flow, please refer to **RH850/U2Ax SAN Section 7.4.4.2 SW Test procedure, Self-Diagnosis for the address feedback**. **NOTE**: This sample program can be used as a reference for the following SW flows. ・**CRAM** Address Feedback (For more detail, refer to ***RH850/U2Ax SAN Section 7.5.4.2 SW Test procedure, Self-Diagnosis for the address feedback***.) ・**DTS RAM** Address Feedback (For more detail, refer to ***RH850/U2Ax SAN Section 7.7.4.2 SW Test procedure, Self-Diagnosis for the address feedback***.) For detail of the differences between LRAM error injection and the above RAM error injection, please refer to ***RH850/U2A-EVA User's Manual : Hardware***.
7.5 Cluster RAM ECC and Address Feedback	・Self-Diagnosis for ECC decoder [SAN-U2Ax-0704-403] 1. Writing to the RAM Data 2. Writing and Reading the ECC Data ・Self-Diagnosis of the ECC Decoder for Read-Modify-Write [SAN-U2Ax-0704-404] 1. ECC Decoder for Read Data	7_5_5_DecoderforReadModifyWritetoRead1b	This sample program is for **CRAM** software self-test by using CRAM ECC 1bit error, checking whether this ECC error occurs when CPU0 accesses CRAM0 with RmW operation (**ECC Decoder for Read Data**). For detail flow, please refer to ***RH850/U2Ax SAN Section 7.5.4.2 SW Test procedure, Self-Diagnosis of the ECC Decoder for Read-Modify-Write.*** **NOTE**: This sample program can be used as a reference for ECC 2bit error injection.

RH850/U2Ax SAN		Sample Program	
Chapter	SAN ID	Folder Name	Description
	・Self-Diagnosis of the ECC Decoder for Read-Modify-Write [SAN-U2Ax-0704-404] 2. ECC Decoder for Write Data	7_5_7_decoderforReadModifyWritetoWrite	This sample program is for **CRAM** software self-test by using CRAM ECC 1bit error , checking whether this ECC error occurs when CPU0 accesses CRAM0 with RmW operation (**ECC Decoder for Write Data**). For detail flow, please refer to ***RH850/U2Ax SAN Section 7.5.4.2 SW Test procedure, Self-Diagnosis of the ECC Decoder for Read-Modify-Write***. **NOTE**: This sample program can be used as a reference for ECC 2bit error injection.
		7_5_9_CRAMECCRMWSDWData	This sample program is for **CRAM** software self-test by using CRAM ECC 1bit error , checking whether this ECC error occurs when CPU0 accesses CRAM0 with RmW operation (**ECC Decoder for Write Data**) by **CAXI** operation. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.5.4.2 SW Test procedure, Self-Diagnosis of the ECC Decoder for Read-Modify-Write***. **NOTE**: This sample program can be used as a reference for ECC 2bit error injection.
7.6 Instruction Cache EDC and Address Feedback	Self-Diagnosis for EDC decoder [SAN-U2Ax-0705-401]	7_6_1_EdcAddressinjection	This sample program is for **Instruction cache data RAM** software self-test by using Instruction cache data RAM EDC 1bit error, checking whether this ECC error occurs when CPU0 reads the instruction cache, which is injected the error, by instruction fetch. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.6.4.2 SW Test procedure, Self-Diagnosis for EDC decoder***. **NOTE**: This sample program can be used as a reference for ECC 2bit error injection.
		7_6_1_EdcAddressinjection_TAG	This sample program is for **Instruction cache tag RAM** software self-test by using Instruction cache tag RAM EDC 1bit error, checking whether this ECC error occurs when CPU0 reads the instruction cache, which is injected the error, by instruction fetch. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.6.4.2 SW Test procedure, Self-Diagnosis for EDC decoder***. **NOTE**: This sample program can be used as a reference for ECC 2bit error injection.
	Self-Diagnosis for the address feedback [SAN-U2Ax-0705-402]	7_6_3_InstructionCacheEdcAddressFeedback	This sample program is for **Instruction cache tag RAM** software self-test by using instruction cache address feedback error, checking whether instruction cache address feedback error occurs when CPU prefetches to the address that caching is disabled. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.6.4.2 SW Test procedure, Self-Diagnosis for the address feedback***.
		7_6_3_InstructionCacheEdcAddressFeedback_DATA	This sample program is for **Instruction cache data RAM** software self-test by using instruction cache address feedback error, checking whether instruction cache address feedback error occurs when CPU prefetches to the address that caching is disabled. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.6.4.2 SW Test procedure, Self-Diagnosis for the address feedback***.
7.7 DTS RAM ECC and Address Feedback	Self-Diagnosis for ECC decoder [SAN-U2Ax-0706-403]	7_7_3_SelfDiagnosisEccDecoder	This sample program is for **DTS RAM** software self-test by using DTS RAM ECC 1bit error, checking whether this ECC error occurs when CPU0 reads DTS RAM which is injected the error. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.7.4.2 SW Test procedure, Self-Diagnosis for ECC decoder***. **NOTE**: This sample program can be used as a reference for ECC 2bit error injection.
7.8 sDMAC RAM ECC	Self-Diagnosis for ECC decoder of Descriptor RAM [SAN-U2Ax-0707-401]	7_8_1_DescriptorRAM1bit	This sample program is for **sDMAC Descriptor RAM** software self-test by using sDMAC Descriptor RAM ECC 1bit error, checking whether this ECC error occurs when CPU0 reads DTS Descriptor RAM which is injected the error. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.8.4.2 SW Test procedure, Self-Diagnosis for ECC decoder of Descriptor RAM***. **NOTE**: This sample program can be used as a reference for ECC 2bit error injection.
	Self-Diagnosis for ECC decoder of Data RAM [SAN-U2Ax-0707-402]	7_8_3_DataRAM1bit	This sample program is for **sDMAC Data RAM** software self-test by using sDMAC Data RAM ECC 1bit error, checking whether this ECC error occurs when CPU0 reads sDMAC RAM which is injected the error. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.8.4.2 SW Test procedure, Self-Diagnosis for ECC decoder of Data RAM***. **NOTE**: This sample program can be used as a reference for ECC 2bit error injection.
7.9 ECC for Peripheral RAM	Self-Diagnosis for ECC decoder of Peripheral RAM [SAN-U2Ax-0708-401]	7_9_1_EccPeripheralRam32b	This sample program is for **Peripheral RAM (RSCAN0)** software self-test by using ECC 1bit error, checking whether this ECC error occurs when CPU0 reads RSCAN RAM which is injected the error. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.9.4.2 SW Test procedure, Self-Diagnosis for ECC decoder of Peripheral RAM***. **NOTE**: This sample program can be used as a reference for ECC 2bit error injection.
7.10 ECC protection on Bus	Error Injection for CPU data path (bus-master side) [SAN-U2Ax-0709-401]	7_10_1_EccProtectionBusCpu0	This sample program is for the **data transfer path**'s software self-test by using "ECC 1bit error in **read** data to **PE0** from peripherals", checking whether this ECC error occurs when CPU0 reads EGDATORG0. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.10.4.2 SW Test procedure, Error Injection for CPU data path (bus-master side)***. **NOTE**: This sample program can be used as a reference for ECC 2bit error injection.

RH850/U2Ax SAN		Sample Program	
Chapter	SAN ID	Folder Name	Description
	Error Injection for CPU data path (bus-slave side) [SAN-U2Ax-0709-402]	7_10_3_Cpu0busSlaveDataPath	This sample program is for the **data transfer path**'s software self-test by using "ECC 1bit error in **write** data to **PE0**", checking whether this ECC error occurs when DTS transfers from EGDATORG0 to LRAM. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.10.4.2 SW Test procedure, Error Injection for CPU data path (bus-slave side)***. **NOTE**: This sample program can be used as a reference for ECC 2bit error injection.
	Error Injection for Peripheral data path (including P-Bus/H-Bus/I-Bus modules) [SAN-U2Ax-0709-403]	7_10_5_Pbusmoduledatapathpbus0	This sample program is for the **data transfer path**'s software self-test by using "ECC 1bit error in **write** data to **VCI2APB** bridge for P-Bus Group 0", checking whether this ECC error occurs when DTS transfers from EGDATORG0 to P-Bus. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.10.4.2 SW Test procedure, Error Injection for Peripheral data path (including P-Bus/H-Bus/I-Bus modules)***. **NOTE**: This sample program can be used as a reference for ECC 2bit error injection.
		7_10_7_PbusmoduledatapathHBus	This sample program is for the **data transfer path**'s software self-test by using "ECC 1bit error in **write** data to **H-Bus slave**", checking whether this ECC error occurs when DTS transfers from EGDATORG0 to H-Bus Group. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.10.4.2 SW Test procedure, Error Injection for Peripheral data path (including P-Bus/H-Bus/I-Bus modules)***. **NOTE**: This sample program can be used as a reference for ECC 2bit error injection.
		7_10_9_pathforIPIRdatapath	This sample program is for the **data transfer path**'s software self-test by using "ECC 1bit error in **write** data to **IPIR**", checking whether this ECC error occurs when DTS transfers from EGDATORG0 to I-Bus Group0 : IPIR. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.10.4.2 SW Test procedure, Error Injection for Peripheral data path (including P-Bus/H-Bus/I-Bus modules)***. **NOTE**: This sample program can be used as a reference for ECC 2bit error injection.
	Error Injection for DTS, sDMAC and H-Bus masters data path [SAN-U2Ax-0709-404]	7_10_11_EccProtectionBusDTS	This sample program is for the **data transfer path**'s software self-test by using "ECC 1bit error in **read** data to **DTS**", checking whether this ECC error occurs when DTS transfers from EGDATORG0 to CRAM(Cluster0). For detail flow, please refer to ***RH850/U2Ax SAN Section 7.10.4.2 SW Test procedure, Error Injection for DTS, sDMAC and H-Bus masters data path***. **NOTE**: This sample program can be used as a reference for ECC 2bit error injection.
		7_10_13_EccProtectionBusSDMAC	This sample program is for the **data transfer path**'s software self-test by using "ECC 1bit error in **read** data to **sDMAC0**", checking whether this ECC error occurs when sDMAC0 transfers from EGDATORG0 to CRAM(Cluster0). For detail flow, please refer to ***RH850/U2Ax SAN Section 7.10.4.2 SW Test procedure, Error Injection for DTS and sDMAC data path***. **NOTE**: This sample program can be used as a reference for ECC 2bit error injection.
	Error Injection for sDMAC Data RAM data path [SAN-U2Ax-0709-405]	7_10_15_sDmacDataRAMdatapath	This sample program is for the **data transfer path**'s software self-test by using "ECC 1bit error in **internal buffer of sDMAC0**", checking whether this ECC error occurs when sDMAC0 reads from CRAM(Cluster0) to CRAM(Cluster0). For detail flow, please refer to ***RH850/U2Ax SAN Section 7.10.4.2 SW Test procedure, Error Injection for sDMAC Data RAM data path***. **NOTE**: This sample program can be used as a reference for ECC 2bit error injection.
	Error Injection for system bus data path (RMW: read data/write data) [SAN-U2Ax-0709-406]	7_10_17_InterelementbusdatapathReaddata	This sample program is for the **data transfer path**'s software self-test by using "ECC 1bit error in **read** data to **VCI2AXI bridge** in cluster 0", checking whether this ECC error occurs when CPU0 reads H-Bus Group. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.10.4.2 SW Test procedure, Error Injection for system bus data path (RMW: read data/write data).*** **NOTE**: This sample program can be used as a reference for ECC 2bit error injection.
		7_10_19_InterelementbusdatapathWitedata	This sample program is for the **data transfer path**'s software self-test by using "ECC 1bit error in **write** data to **VCI2AXI bridge** in cluster 0", checking whether this ECC error occurs when CPU writes H-Bus Group. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.10.4.2 SW Test procedure, Error Injection for system bus data path (RMW: read data/write data)***. **NOTE**: This sample program can be used as a reference for ECC 2bit error injection.
	Error Injection for address path [SAN-U2Ax-0709-407]	7_10_21_EccProtectionBusCram	This sample program is for the **data transfer path**'s software self-test by using "the address ECC 1bit error in request address **from PE0 to Cluster RAM in cluster 0**", checking whether this ECC error occurs when CPU0 reads from CRAM(Cluster0) to LRAM. For detail flow, please refer to ***RH850/U2Ax SAN Section 7.10.4.2 SW Test procedure, Error Injection for address path***. **NOTE**: This sample program can be used as a reference for ECC 2bit error injection.

RH850/U2Ax SAN		Sample Program	
Chapter	SAN ID	Folder Name	Description
		7_10_23_EDCaddrErrInjectDtsCram1bit	This sample program is for the **data transfer path**'s software self-test by using "the address ECC 1bit error in request address **to Cluster RAM in cluster 0 from outside**", checking whether this ECC error occurs when DTS reads CRAM(Cluster0). For detail flow, please refer to ***RH850/U2Ax SAN Section 7.10.4.2 SW Test procedure, Error Injection for address path***. **NOTE**: This sample program can be used as a reference for the error injection of "an address ECC 2bit error in request address to Cluster RAM in cluster 0 from outside" and the following address ECC 1bit and 2bit error. ・request address to **PE0** ・request address to **Code Flash bank B in cluster 0** ・request address to **H-Bus slave** ・request address to **IPIR** ・request address to **AXI2VCI bridge in cluster 0** ・request address to **SAXI2FAXI bridge** ・request address to **AXI2PVCI bridge** ・request address to **SAXI2MBI bridge for cluster 0** ・request address to **the remap module for data read from PE0** ・request address to **the remap module for instruction fetch from PE0** ・request address to **the remap module from a SAXI master** ・request address to **FAXI2SAXI bridge** For detail of the differences between ECC error injection for access from DTS to CRAM and ECC error injection for the above access, please refer to ***RH850/U2A-EVA User's Manual : Hardware***.
8.1 Data CRC Function K (KCRC)	Code Flash Memory Signature test [SAN-U2Ax-0800-401]	8_1_1_KCRCCodeFlashSignTest	This sample program is for **Code Flash Memory Signature** software self-test by using **CPU**, checking whether CRC data calculated from data of Code Flash Memory by KCRC matches the expected value of CRC, which has already been written in Code Flash Memory. For detail flow, please refer to ***RH850/U2Ax SAN Section 8.4.2 SW Test procedure, Code Flash Memory Signature test***. **NOTE**: This sample program can be used as a reference for **Data Flash Memory Signature** test (by **CPU**). For detail of the differences between Code Flash Memory and Data Flash Memory, please refer to ***RH850/U2A-EVA User's Manual : Hardware***.
		8_1_2a_KCRCCodeFlashSignTest_DTS	This sample program is for **Code Flash Memory Signature** software self-test by using **DTS**, checking whether CRC data calculated from data of Code Flash Memory by KCRC matches the expected value of CRC, which has already been written in Code Flash Memory. For detail flow, please refer to ***RH850/U2Ax SAN Section 8.4.2 SW Test procedure, Code Flash Memory Signature test***. **NOTE**: This sample program can be used as a reference for **Data Flash Memory Signature** test (by **DTS**).For detail of the differences between Code Flash Memory and Data Flash Memory, please refer to ***RH850/U2A-EVA User's Manual : Hardware***.
		8_1_2b_KCRCCodeFlashSignTest_DMAC	This sample program is for **Code Flash Memory Signature** software self-test by using **sDMAC**, checking whether CRC data calculated from data of Code Flash Memory by KCRC occurs when the expected value of CRC, which has already been written in Code Flash Memory. For detail flow, please refer to ***RH850/U2Ax SAN Section 8.4.2 SW Test procedure, Code Flash Memory Signature test***. **NOTE**: This sample program can be used as a reference for **Data Flash Memory Signature** test (by **sDMAC0**). For detail of the differences between Code Flash Memory and Data Flash Memory, please refer to ***RH850/U2A-EVA User's Manual : Hardware***.
9.1 Voltage Monitor	SW self-diagnosis test for Voltage Monitor [SAN-U2Ax-0900-401]	9_1_2_VoltageMonitorVMONOUT	This sample program checks whether "**HDET and LDET voltage error** of ISOVDD, AWOVDD, VCC, and E0VCC" occur and "**VMONOUT flag**" is set when voltage violation error is injected by VMONDIAG register. For detail flow, please refer to ***RH850/U2Ax SAN Section 9.1.4.2 SW Test procedure and Hardware User's manual***.
		9_1_3_VoltageMonitorRESET	This sample program checks whether "**HDET and LDET voltage error** of ISOVDD, AWOVDD, VCC, and E0VCC" and "**VMON Reset**" occur when voltage violation error is injected by VMONDIAG register. For detail flow, please refer to ***RH850/U2Ax SAN Section 9.1.4.2 SW Test procedure and Hardware User's manual***.
9.2 Delay Monitor	SW self-diagnosis test for Delay Monitor [SAN-U2Ax-0901-401]	9_2_1_Delay Monitor	This sample program checks whether **DMON error** occurs when DMON error is injected by DMONDIAG register. For detail flow, please refer to ***RH850/U2Ax SAN Section 9.2.4.2 SW Test procedure and Hardware User's manual***.
10. Clock Monitor (CLMA)	・CLMA SW Test procedure [SAN-U2Ax-1000-401] ・CLMA SW Test procedure [SAN-U2Ax-1000-402]	10_1_1_Clock Monitor	This sample program checks whether **CLMA0-3, 5 and 6 higher error** occurs when CLMA higher error is injected. For detail flow, please refer to ***RH850/U2Ax SAN Section 10.4.2 SW Test procedure and Hardware User's manual***. **NOTE**: This sample program must be operated when CLK_SYS source is **PLL clock**.
		10_1_1_Clock Monitor_2	This sample program checks whether **CLMA0-3, 5 and 6 lower error** occurs when CLMA lower error is injected. For detail flow, please refer to ***RH850/U2Ax SAN Section 10.4.2 SW Test procedure and Hardware User's manual***. **NOTE**: This sample program must be operated when CLK_SYS source is **PLL clock**.

RH850/U2Ax SAN		Sample Program	
Chapter	SAN ID	Folder Name	Description
		10_1_1_ClockMonitor_CLMA4	This sample program checks whether **CLMA4 higher error** occurs when CLMA higher error is injected. For detail flow, please refer to ***RH850/U2Ax SAN Section 10.4.2 SW Test procedure and Hardware User's manual***. **NOTE**: This sample program must be operated when CLK_SYS source is **CLK_IOSC clock**.
		10_1_1_ClockMonitor_CLMA4_2_	This sample program checks whether **CLMA4 lower error** occurs when CLMA lower error is injected. For detail flow, please refer to ***RH850/U2Ax SAN Section 10.4.2 SW Test procedure and Hardware User's manual***. **NOTE**: This sample program must be operated when CLK_SYS source is **CLK_IOSC clock**.
11.1 Failure detection of I/O ports	SW test for I/O port [SAN-U2Ax-1100-401]	11_1_1_detectionIOports	This sample program checks whether the **input and output port** are same level when the output and input port are external-loopback- connected. For detail flow, please refer to ***RH850/U2Ax SAN Section 11.4.2 SW Test procedure***.
13. Failure detection of A/D Converter (ADCJ)	A/D Conversion Circuit Diagnostic Function [SAN-U2Ax-1300-401]	13_1_1_ADConversionCirDiagnosticFunc	This sample program is for ADC software self-test by using **normal A/D conversion**, checking whether A/D conversion result of normal A/D conversions the same as input voltage to the analog input pin. For detail flow, please refer to ***RH850/U2Ax SAN Section 13.4.2 SW Test procedure, A/D Conversion Circuit Diagnostic Function***.
	A/D Converter Self-Diagnosis Function [SAN-U2Ax-1300-402]		This sample program is for ADC software self-test by using **A/D conversion circuit self-diagnosis**, checking whether A/D conversion result of A/D conversion circuit self-diagnosis is the same as the A/D conversion circuit self-diagnosis voltage level. For detail flow, please refer to ***RH850/U2Ax SAN Section 13.4.2 SW Test procedure, A/D Converter Self-Diagnosis Function and Hardware User's manua***l.
	A/D Pin Level Diagnostic Function [SAN-U2Ax-1300-403]	13_1_3_ADPinLevelDiagnosticFunc_IO_RRAMP_Adcore	This sample program is for ADC software self-test by using **Pin-level self-diagnosis with Buffer Amp**, checking whether A/D conversion result of pin-level self-diagnosis is the same as the pin level self-diagnosis voltage level. For detail flow, please refer to ***RH850/U2Ax SAN Section 13.4.2 SW Test procedure, A/D Pin Level Diagnostic Function and Hardware User's manual***.
		13_1_4_ADPinLevelDiagnosticFunc_IO_Adcore	This sample program is for ADC software self-test by using **Pin-level self-diagnosis without Buffer Amp**, checking whether A/D conversion result of Pin-level self-diagnosis is the same as the pin level self-diagnosis voltage level. For detail flow, please refer to ***RH850/U2Ax SAN Section 13.4.2 SW Test procedure, A/D Pin Level Diagnostic Function and Hardware User's manua***l.
		13_1_5_ADPinLevelDiagnosticFunc_IO_TH_Adcore	This sample program is for ADC software self-test by using **Pin-level self-diagnosis of the T&H path**, checking whether A/D conversion result of pin-level self-diagnosis of the T&H path is the same as the pin level self-diagnosis voltage level. For detail flow, please refer to ***RH850/U2Ax SAN Section 13.4.2 SW Test procedure, A/D Pin Level Diagnostic Function and Hardware User's manual***.
	A/D Wiring-Break Detection Function [SAN-U2Ax-1300-404]	13_1_6_ADWiringBreakDetFuncMode1	This sample program is for ADC software self-test by using **Wiring-Break Detection Mode 1**, checking whether A/D conversion result is near 0 V. For detail flow, please refer to ***RH850/U2Ax SAN Section 13.4.2 SW Test procedure, A/D Wiring-Break Detection Function and Hardware User's manual***.
		13_1_7_ADWiringBreakDetFuncMode2_1	This sample program is for Wiring-Break Detection software self-test by using **Wiring-Break Detection Mode 2** (physical channel IO pull-down and pull-up) and normal AD conversion mode, checking whether the wiring is broken. For detail flow, please refer to ***RH850/U2Ax SAN Section 13.4.2 SW Test procedure, A/D Wiring-Break Detection Function and Hardware User's manual***.
14. Inter-processor communication resources	IPIR [SAN-U2Ax-1400-401]	14_1_1_communicationIPIR	This sample program is for the example of the **internal communications** between CPU0 and CPU1 by using **IPIR**. For detail flow, please refer to ***RH850/U2Ax SAN Section 14.4.2 SW Test procedure, IPIR***.
	BARR [SAN-U2Ax-1400-402]	14_1_2_communicationBar	This sample program is for the example of **synchronization for completion of the processes** of CPU0 and CPU1 by using **BARR**. For detail flow, please refer to ***RH850/U2Ax SAN Section 14.4.2 SW Test procedure, BARR***.
16. Error Control Module (ECM)	Error Injection for ECM [SAN-U2Ax-1600-401]	16_1_1_errorcontrolmoduleecm	This sample program is for **ECM** software self-test by using **ECM compare error and ERROROUT status error**, checking whether ECM compare error and ERROROUT status error occurs when ECM compare error is injected. For detail flow, please refer to ***RH850/U2Ax SAN Section 16.4.2 SW Test procedure, Error Injection for ECM***. **NOTE**: This sample program can be used as a reference for checking **ERROROUT_C pin status** (For detail, refer to Note1 of "***RH850 U2Ax SAN Figure 16.3 Example of ECM pseudo error injection flowchart (static mode without delay timer)***").
	Procedure for Port safe state [SAN-U2Ax-1600-402-NoLink]	16_1_4_PortSafeProcedure	This sample program is for setting **port safe state function**. For detail flow, please refer to ***RH850/U2Ax SAN Section 16.4.2 SW Test procedure, Procedure for Port safe state***.
-	-	OPBT_com_setting\src\optionbytes.asm	This is settings of **Configuration Setting Area** for sample programs except below. ● 3_2_1_memoryprotectionMDP ● 5_1_2_WatchdogTimer ● 9_1_2_VoltageMonitorVMONOUT ● 9_1_3_VoltageMonitorRESET ● 9_2_1_DelayMonitor The settings in the **Configuration Setting Area** for each of the above sample programs are contained in "optionbytes_*.asm" in the folder of each sample program.
-	-	bist_common.h	This is common program for C source sample programs.
-	-	common.h	This is common program for C source sample programs.
-	-	common_asm.inc	This is common program for assembler sample programs.

Revision History

Rev.	Date	Description	
		Page	Summary
0.7	2020.04.24	-	Initial version
1.0	2020.11.11	1	Modified target device.
		5	Modified the description of 7.6 Instruction Cache EDC and Address Feedback.
		7	Add the description of 8_1_1_KCRCCodeFlashSignTest.
1.01	2022.01.31	1	Modified the following description. ● Device file of “Target integrated development environment ● Reference Document
		3-8	Deleted revision information of reference document.
		7,8	Modified the following description. ● 10_1_1_ClockMonitor ● 10_1_1_ClockMonitor_2 Add the following description. ● 10_1_1_ClockMonitor_CLMA4 ● 10_1_1_ClockMonitor_CLMA4_2
1.1	2022.06.30	1	Modified the following description. ● Device file of “Target integrated development environment ● Revision of reference document
		6	Modified the following description. ● 7_10_7_PbusmoduledatapathHBus ● 7_10_17_InterelementbusdatapathReaddata ● 7_10_19_InterelementbusdatapathWritedata
		8	Added the following description. ● OPBT_com_setting\src\optionbytes.asm ● bist_common.h ● common.h ● common_asm.inc

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.