RH850/U2B Group

R01AN6859EJ0110
Rev.1.10

RLIN3 Application Note

Summary

This application note explains the basic usage of LIN interface (RLIN3) for RH850/U2Bx.

Aim of this document and software is to provide supplemental information for the function on RH850/U2B. It is not intended to implement in the design for mass production. There is no guarantee to update in this document and software to reflect the latest manual, errata, technical update and development environment. You are fully responsible for the incorporation or any other use of the information of this document in the design of your product or system, and please refer to latest manual, errata, technical update and development environment.

Target Device

- RH850/U2B Group

Target Integrated Development Environment

CS+ (from RENESAS Electronics)

Device file: DR7F702Z21*.DVF

Reference Document

RH850/U2B User's Manual: Hardware

For function details and electrical characteristics, please refer to "User's Manual: Hardware".

This application note is based on the following manual.

- RH850/U2B User's Manual (Rev.1.00): R01UH0923EJ0100

Contents

1. Introduction

1.1 Specification

This application note explains the following functions for operating the basic function.

- LIN master header & response transmission
- LIN master header/slave response transmission

1.2 System Configuration

Figure 1-1 shows the system configuration.

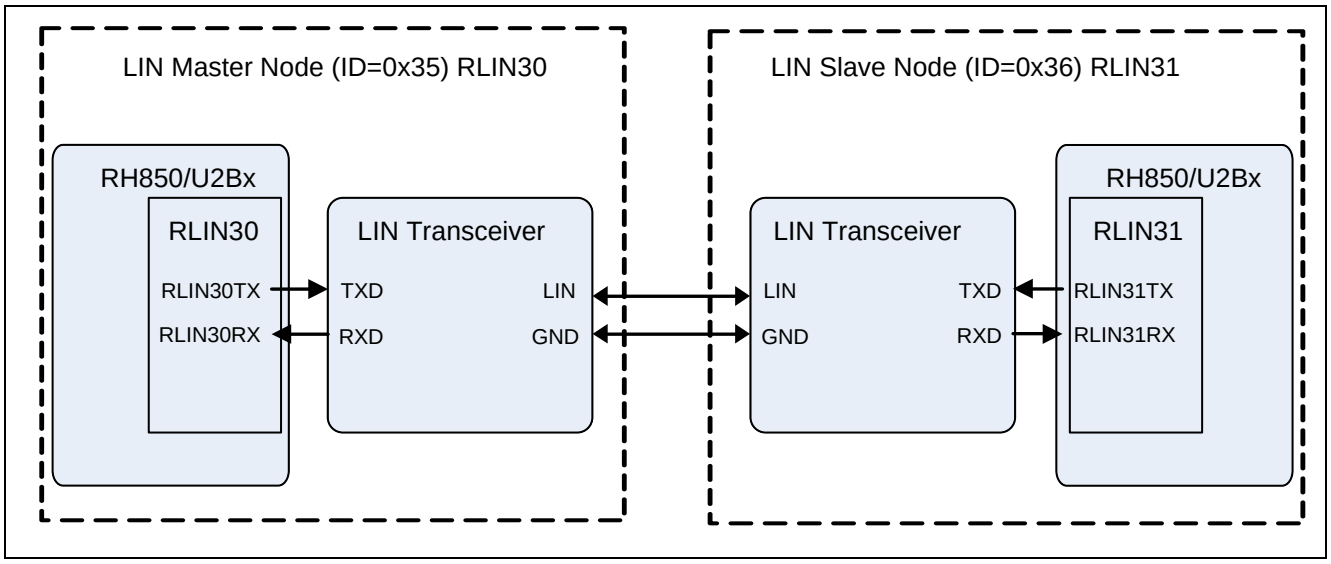

Figure 1-1 System Configuration

2. LIN Communication

2.1 LIN Master Header & Response Transmission

2.1.1 Specification

LIN master transmits the header and response. In this operation example, perform transmit start request after (1) to (9) settings in this operation example.

As the setting example, the setting details of the sample code are written below.

- (1) Transmit/Receive Port Setting
  Port for transmission: Set P34_0 (RLIN30TX) to the sharing output mode 8.
  Port for reception: Set P34_2 (RLIN30RX) to the sharing output mode 8.

- (2) Transmission Baud Rate Setting: 9600bps
  <RLIN30>
  Communication Baud Rate
  =LIN communication clock source / Prescaler / LIN baud rate prescaler
  / LIN system clock / Bit sampling number
  =80MHz / 2 / 130 / 2 / 16
  ≒9600bps

-
  Prescaler setting: Select 1/2
  LIN baud rate prescaler 0 setting: Specify 1/(129+1)
  LIN baud rate prescaler 1 setting: Unused
  LIN system clock selection: Select fb(1/2)
  Number of bit sampling selection: Select 16 sampling

Figure **2-1** shows the connection of the baud rate setting.

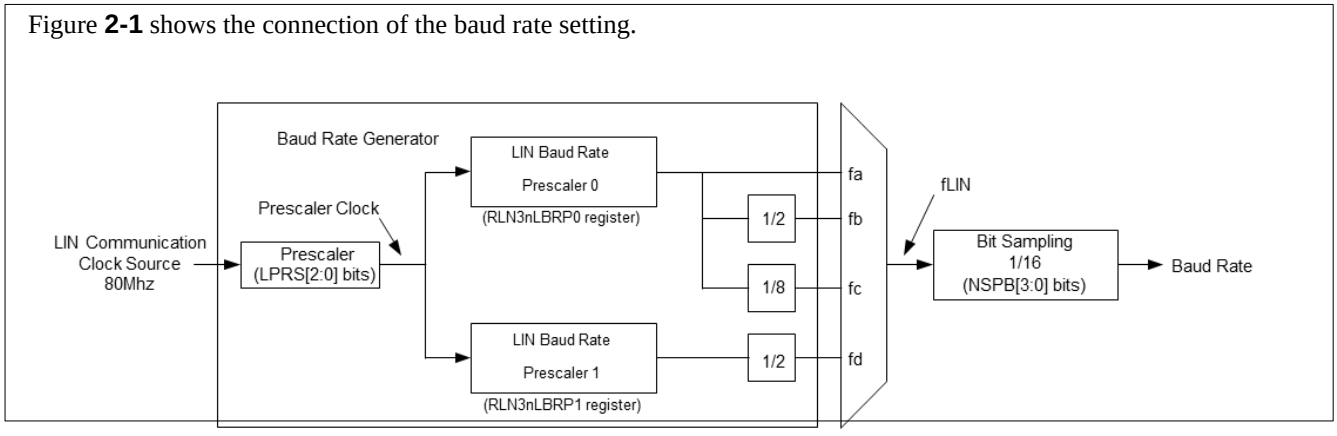

Figure 2-1 Baud Rate Setting

- (3)Interrupt Setting
  RLIN30 receive completion/Transmit completion/Error detection interrupt: Enable (ch622, ch621, ch623)

- (4)Error Detection Setting
  Framing error: Enable
  Frame timeout error: Enable
  Physical Bus Error: Enable
  Bit error: Enable

- (5)Frame Configuration Setting
  Transmit break width: 13Tbits
  Transmit break delimiter width: 1Tbit
  Interbyte space (response): 0Tbit
  Interbyte space (header) / response space: 0Tbit

Figure 2-2 shows the frame configuration.

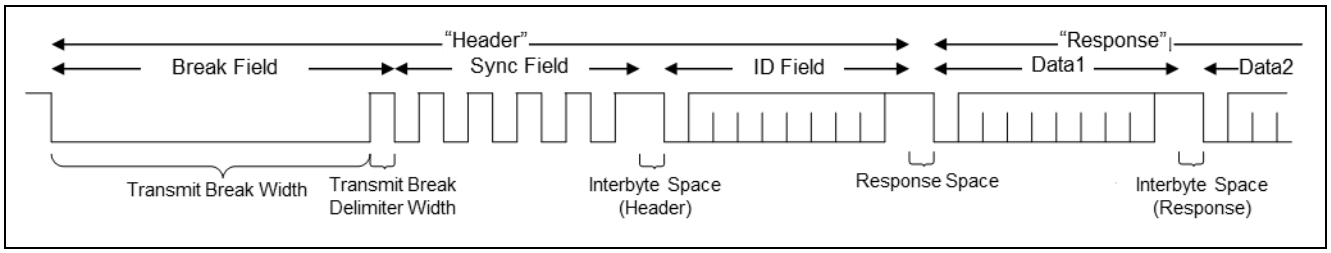

Figure 2-2 Frame Configuration

- (6)Mode Switching
  LIN mode selection bit: LIN operation mode
  LIN reset bit: Release LIN reset mode

- (7)Config Setting of Data Field
  Frame separate mode: Disable (Transmit "header" and "response" by the one of the transmit request)
  Check sum selection: Classic
  Response field communication destination: Transmission
  Response filed length: 8 bytes + check sum

- (8) "Header" Transmit Data Setting
  Parity Bit (2 bits): 11b
  ID (6 bits): 0x35

- (9)"Response" Transmit Data Setting
  Data 1:0x00
  Data 2:0x01
  Data 3:0x02
  Data 4:0x03
  Data 5:0x10
  Data 6:0x11
  Data 7:0x12
  Data 8:0x13

2.1.2 Communication Operation

Figure 2-3 shows the frame transmit operation.

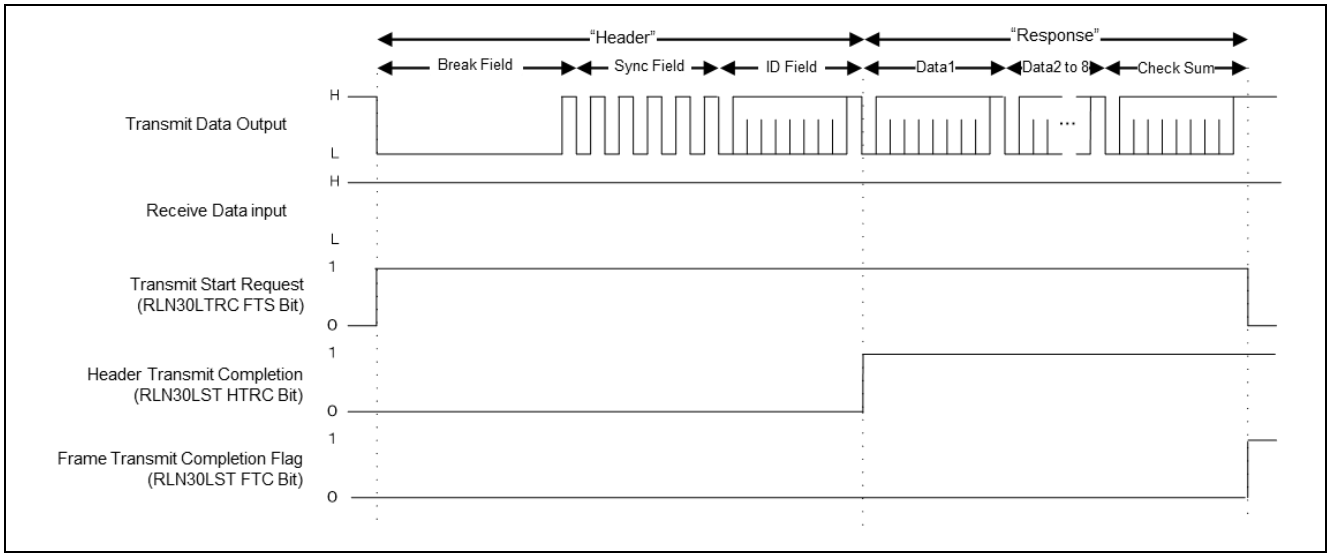

Figure 2-3 Frame Transmit Operation

The following shows the overview of the operation.

- (1)Start the transmission to set 1 to the transmission start request by the software.
- (2)The transmit completion flag becomes 1 when the “header” transmission is completed.
  At this time, the transmit completion interrupt is generated in this setting example.
- (3) The transmit completion flag becomes 1 when the “response” transmission is completed.
  Also, the transmit start request that is set 1 in sequence (1) becomes 0.
  At this time, the transmit completion interrupt is generated in this setting example.

2.1.3 Register Setting

The following shows the setting value of the register and the sample code used in the frame transmit setting.

Table 2-1 shows the register setting value of the transmit/receive port setting.

Table 2-1 Register Setting Value (Port)

Register Name	Setting Value	Function
PCR34_2	0x03000057	Drive strength：high
		Port mode control: Sharing mode Port mode: Input mode Port function control: Sharing mode 8 (RLIN30RX)
PCR34_0	0x03000047	Drive strength：high
		Port output: Low level Port mode control: Sharing mode Port mode: Output mode Port function control: Sharing mode 8 (RLIN30TX)

Table 2-2 shows the register setting value of the communication baud rate setting and the frame configuration setting.

Table 2-2 Register Setting Value (RLIN3 Operation)

Register Name	Setting Value	Function
RLN30LWBR	0x02	Number of bit sampling selection: Select 16 sampling Prescaler division ratio: 1/2
RLN30LBRP0	129	Baud rate prescaler division ratio: 1/(129+1)
RLN30LMD	0x14	Noise filter: Use LIN interrupt output selection: Use transmit completion/ receive completion/status interrupt LIN system clock selection: fb LIN/UART mode selection: LIN master mode
RLN30LBFC	0x00	Transmit break delimiter width: 1Tbit Transmit brake width: 13Tbits
RLN30LSC	0x00	Interbyte space (response) setting: 0Tbit Interbyte space (header) / response space setting: 0Tbit

Table 2-3 shows the register setting value of the interrupt controller.

Table 2-3 Register Setting Value

Register Name	Setting Value	Function
EIBD621	0x00000000	Simultaneous notification interrupt enable bit: Disable Simultaneous notification interrupt port number setting bit: not necessary Host/Guest partition selection bit: Not necessary to set because it corresponds to INTC1 virtualization configuration register (IHVCFG) Interrupt bind destination PEID: PE0(CPU0)
EIC621	0x0040	Interrupt request flag: No interrupt request Interrupt mask bit: No mask Interrupt vector method: Table reference method Interrupt priority: 0 (highest)
EIBD622	0x00000000	Simultaneous notification interrupt enable bit: Disable Simultaneous notification interrupt port number setting bit: not necessary Host/Guest partition selection bit: Not necessary to set because it corresponds to INTC1 virtualization configuration register (IHVCFG) Simultaneous notification interrupt enable bit: Disable
EIC622	0x0040	Interrupt request flag: No interrupt request Interrupt mask bit: No mask Interrupt vector method: Table reference method Interrupt priority: 0 (highest)
EIBD623	0x00000000	Interrupt request flag: No interrupt request Interrupt mask bit: No mask Interrupt vector method: Table reference method Interrupt priority: 0 (highest)
EIC623	0x0040	Simultaneous notification interrupt enable bit: Disable Simultaneous notification interrupt port number setting bit: not necessary Host/Guest partition selection bit: Not necessary to set because it corresponds to INTC1 virtualization configuration register (IHVCFG) Simultaneous notification interrupt enable bit: Disable

Table 2-4 shows the register setting value of the interrupt enable setting and the error detection setting.

Table 2-4 Register Setting Value (Interrupt Enable and Error Detection)

Register Name	Setting Value	Function
RLN30LIE	0x0F	Header transmit interrupt enable bit: Enable Error detection interrupt enable bit: Enable Frame receive completion interrupt enable bit: Enable Frame transmit completion interrupt enable bit: Enable
RLN30LEDE	0x8F	Timeout error selection bit: Response timeout error selection Framing error detection enable bit: Enable Timeout error detection enable bit: Enable Physical bus error detection enable bit: Enable Bit error detection enable bit: Enable

Table 2-5 shows the register setting value of the mode switching.

Table 2-5 Register Setting Value (RLIN3 Mode)

Register Name	Setting Value	Function
RLN30LCUC	0x03	LIN mode selection bit: LIN operation mode LIN reset bit: Release LIN reset mode

Table 2-6 shows the regsiter setting value of the frame transmission.

Table 2-6 Register Setting Value (Frame Transmit Setting)

Register Name	Setting Value	Function
RLN30LDFC	0x18	Continuous selection bit: Data group that is transmitted/received next is the last Communication direction: Transmission Not Frame separate mode Check sum: Classic Response field data length: 8bytes+check sum
RLN30LIDB	0xF5	Parity bit P1:1 Parity bit P0:1 ID:0x35
RLN30LDBR1	0x00	Data 1:0x00
RLN30LDBR2	0x01	Data 2:0x01
RLN30LDBR3	0x02	Data 3:0x02
RLN30LDBR4	0x03	Data 4:0x03
RLN30LDBR5	0x10	Data 5:0x10
RLN30LDBR6	0x11	Data 6:0x11
RLN30LDBR7	0x12	Data 7:0x12
RLN30LDBR8	0x13	Data 8:0x13
RLN30LTRC (FTS)	1	Transmit start request

2.1.4 Sample Code

Table 2-7 shows the global variable of the sample code.

Table 2-7 Global Variable List

Variable Name	Size	Contents
g_errstatus	1byte	When generating the status interrupt, save the error status if the error is generated. (RLN30LEST register vale)

Table 2-8 shows the function list of the sample code.

Table 2-8 Function List

Module Name	Function Name	Function
Maine function	main_pe0	Main processing for LIN. After performing the initial setting, perform the communication start request and it becomes the interrupt waiting status.
RLIN30 initial setting function	Init_RLIN30M	Perform the initial setting for performing the communication processing.
LIN frame communication start function	Start_RLIN30Frame	Perform the communication setting of the header and the response, and communication request.
PID calculation processing function	get_pid	Calculate PID form the frame.
RLIN30 error detection interrupt function	eiint623	Perform the interrupt processing when detecting the error.
RLIN30 receive completion interrupt function	eiint622	Perform the receive completion interrupt processing of LIN frame.
RLIN30 transmit completion interrupt function	eiint621	Perform the transmit completion interrupt processing of LIN frame.

Figure 2-4 shows the flowchart of the main function.

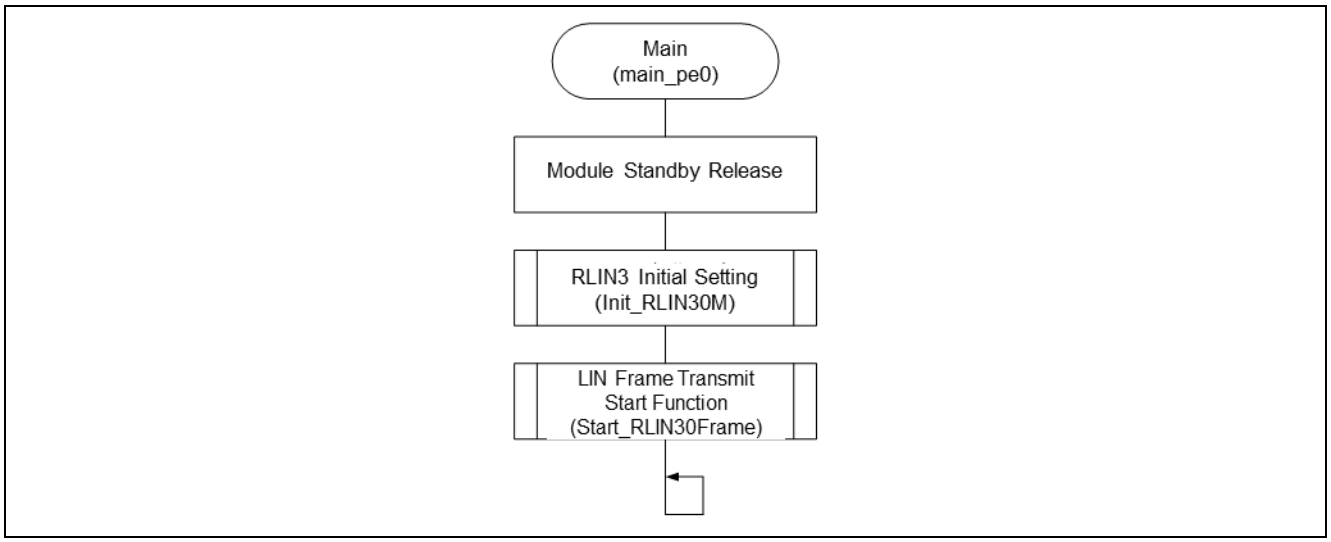

Figure 2-4 Main

Figure 2-5 shows the flowchart of the RLIN3 initial setting function.

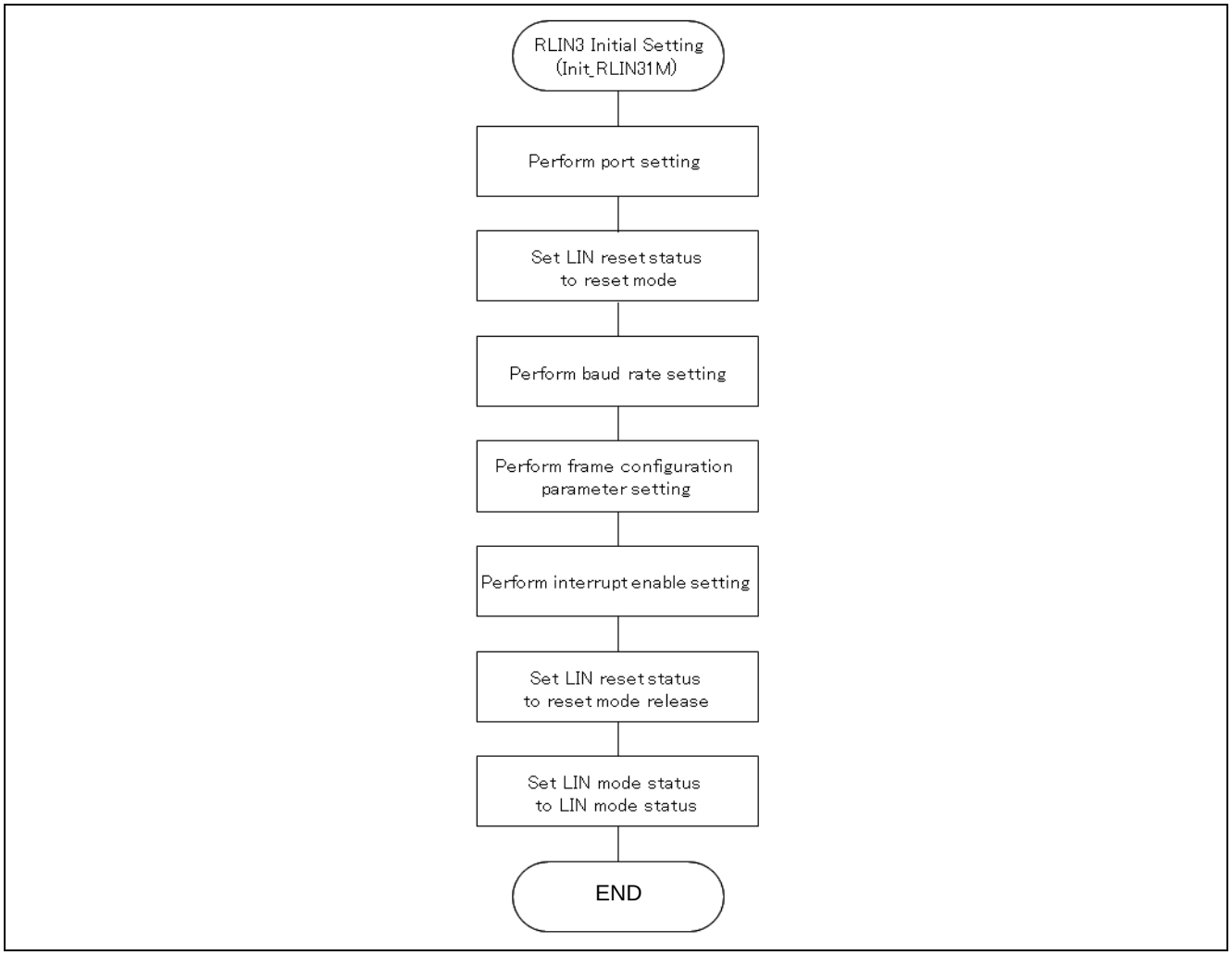

Figure 2-5 RLIN30 Initial Setting

Figure 2-6 shows the flowchart of the LIN frame communication start function.

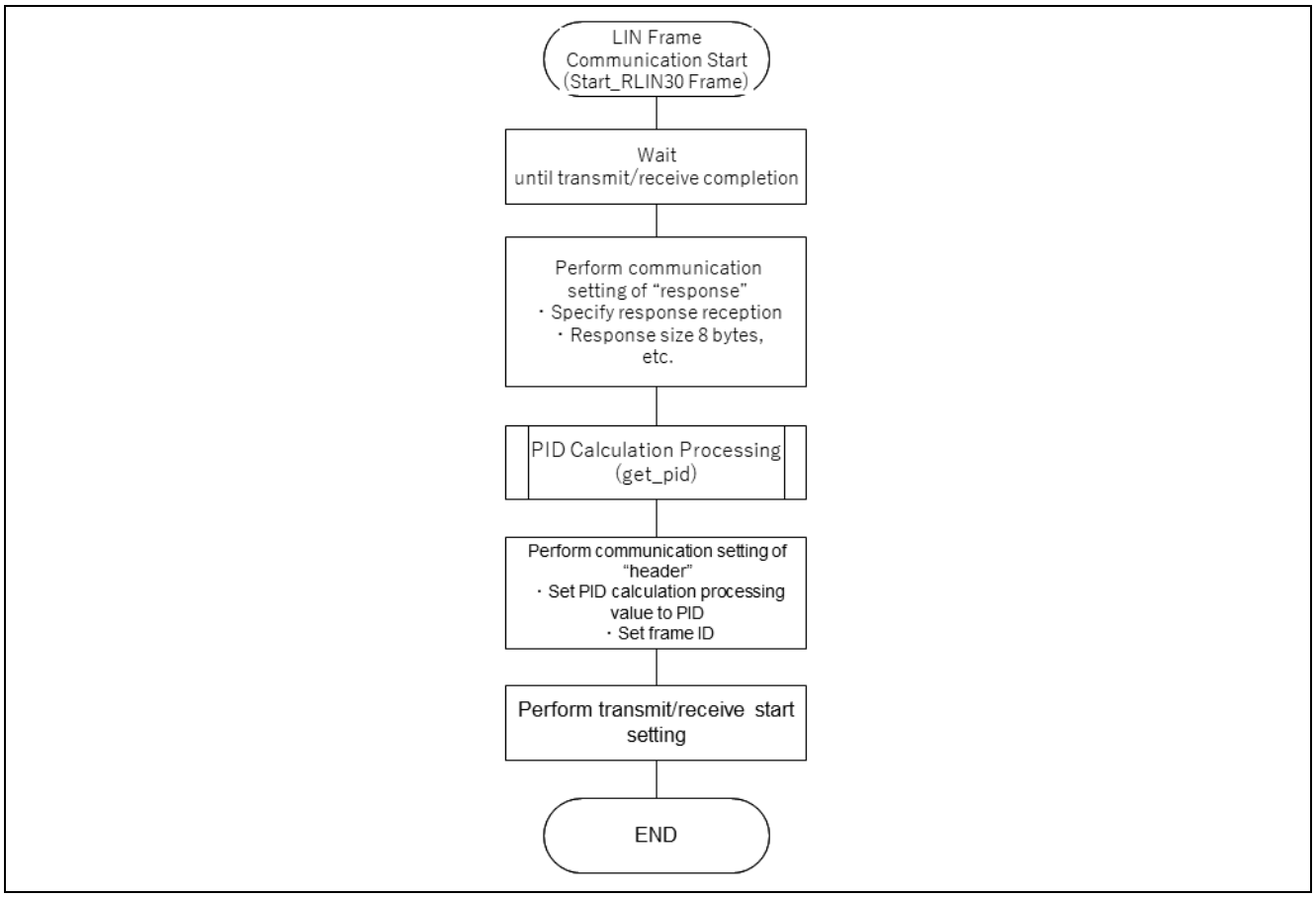

Figure 2-6 LIN Frame Communication Start

Figure 2-7 shows the flowchart of the PID calculation function.

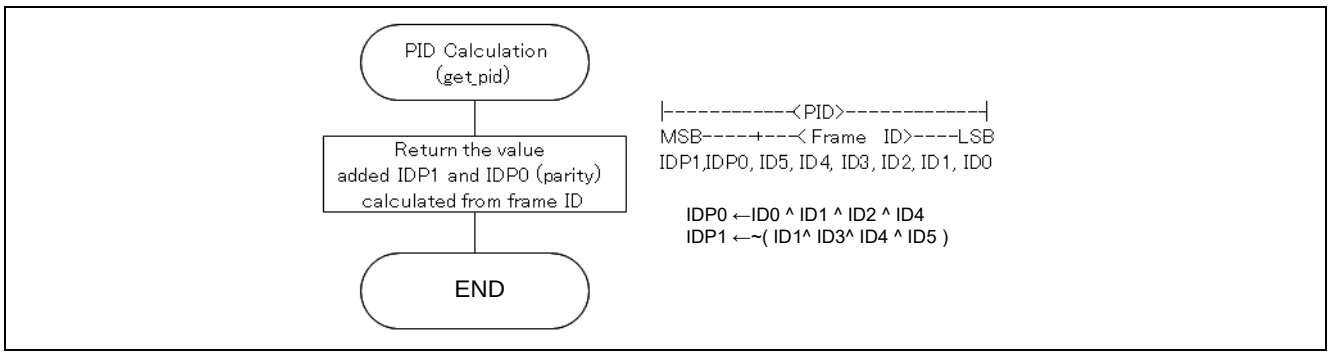

Figure 2-7 PID Calculation

Figure 2-8 shows the flowchart of the RLIN30 transmit completion/receive completion/error detection interrupt function.

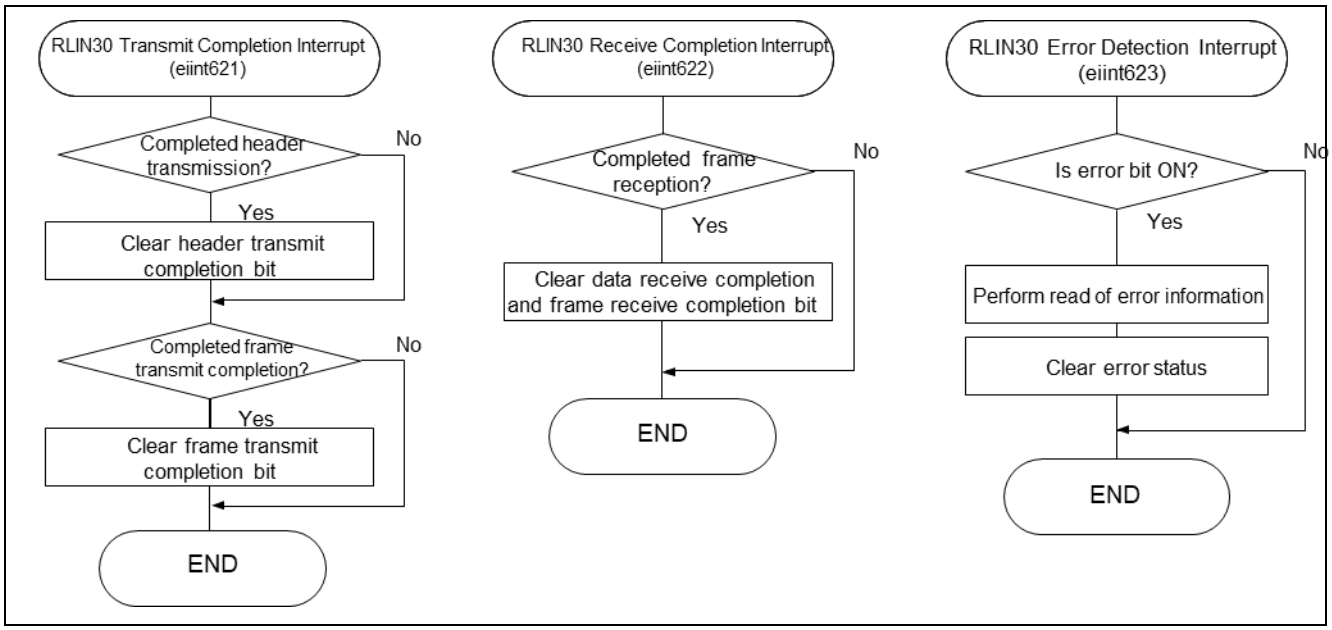

Figure 2-8 RLIN30 Interrupt

2.2 LIN Master Header Transmission/ Slave Response Transmission

2.2.1 Specification

LIN master (RLIN30) transmits “header. When the frame ID that is included in the received header is 0x36, LIN slave (RLIN31) transmits “response”. In this operation example, the transmit start request is performed after performed the sequences (1) to (8).

As the setting example, the following shows the setting contents of the sample code.

- (1)Transmit/Receive Port Setting
  Port for transmission: Set P34_0 (RLIN30TX) to the sharing output mode 8.
  Port for reception: Set P34_2 (RLIN30RX) to the sharing output mode 8.
  Port for reception: Set P20_6 (RLIN31RX) to the sharing output mode 8
  Port for transmission: Set P20_7 (RLIN31TX) to the sharing output mode 8

- (2)Transmission Baud Rate Setting: 9600bps
  <RLIN30>
  Communication Baud Rate
  =LIN communication clock source / Prescaler / LIN baud rate prescaler
  / LIN system clock / Bit sampling number
  ＝80MHz / 2 / 130 / 2 / 16
  ≒9600bps

  Prescaler setting: Select 1/2
  LIN baud rate prescaler 0 setting: Specify 1/(129+1)
  LIN baud rate prescaler 1 setting: Unused
  LIN system clock selection: Select fb(1/2)
  Number of bit sampling selection: Select 16 samplings

Figure 2-9 shows the connection of the baud rate setting.

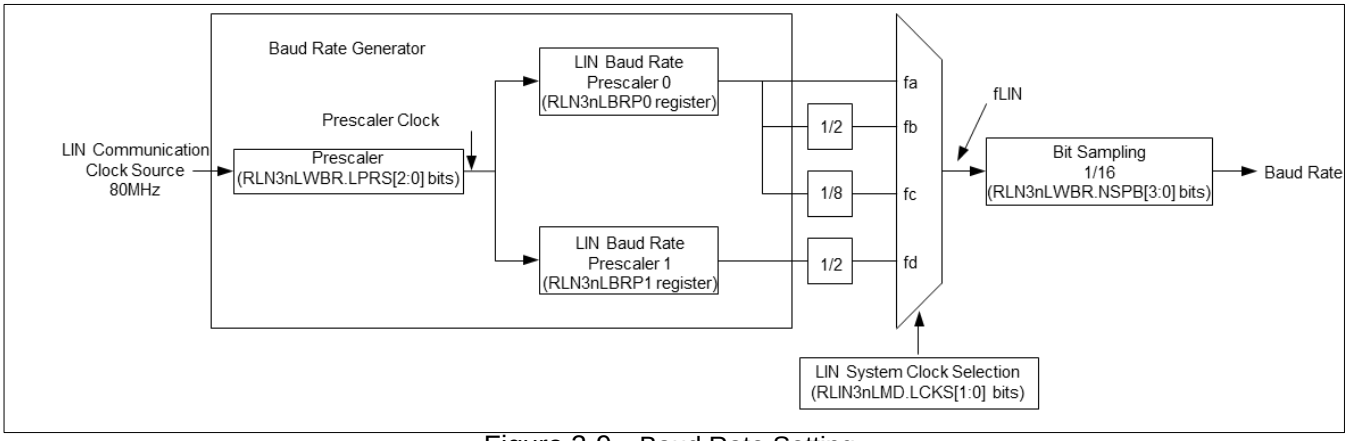

Figure 2-9 Baud Rate Setting

<RLIN31>
Communication Baud Rate
=LIN communication clock source / Prescaler / LIN baud rate prescaler
/ LIN system clock / Bit sampling number
＝80MHz / 8 / 65 / 1 / 16
≒9600bps

Prescaler setting: Select 1/8
LIN baud rate prescaler setting: Specify 1/(64+1)
LIN system clock selection: Select fa(1/1)
Number of bit sampling selection: Select 16 samplings

shows the connection of the baud rate setting.

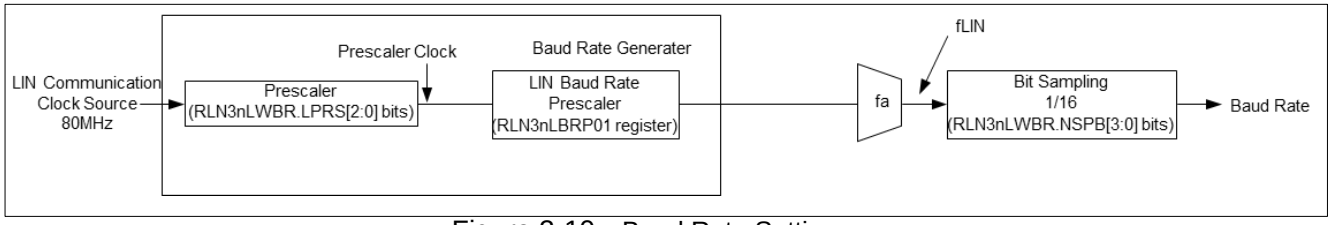

Figure 2-10 Baud Rate Setting

- (3)Interrupt Setting
- RLIN30 receive completion/Transmit completion/Error detection interrupt: Enable (ch622, ch621, ch623)
  RLIN31 receive completion/Transmit completion/Error detection interrupt: Enable (ch627, ch626, ch628)

- (4)Error Detection Setting
  Frame timeout error (response): Enable
  Framing error: Enable
  Physical Bus Error: Enable
  Bit error: Enable

- (5) Frame Configuration Setting
  Transmit break width: 13Tbits
  Transmit break delimiter width: 1Tbit
  Interbyte space (response): 0Tbit
  Interbyte space (header) / response space: 0Tbit

Figure 2-11 shows the frame configuration.

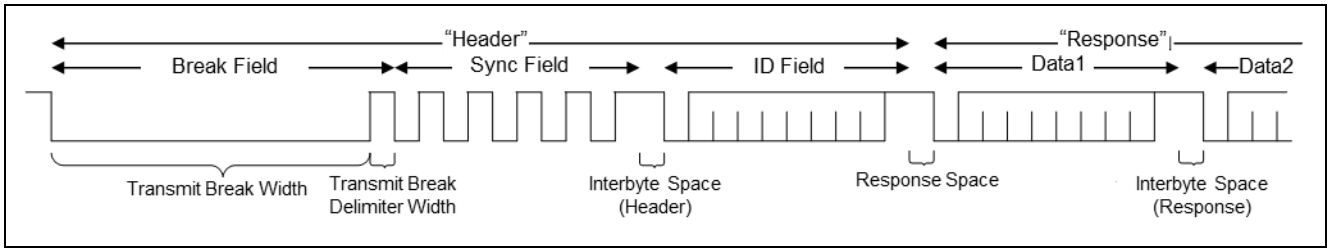

Figure 2-11 Frame Configuration

- (6) Mode Switching
  LIN mode selection bit: LIN operation mode
  LIN reset bit: Release LIN reset mode

- (7) Config Setting of Data Field
  <RLIN30>
  Frame separate mode: Disable
  Check sum selection: Classic
  Response field communication destination: Transmission
  Response filed length: 8 bytes + check sum

  <RLIN31>
  Check sum selection: Classic
  Response field communication destination: Transmission
  Response filed length: 8 bytes + check sum

- (8)”Header” Transmit Data Setting
  Parity Bit (2bits): 11b
  ID (6 bits): 0x35
-

2.2.2 Communication Operation

Figure 2-12 shows the frame transmit/receive operation.

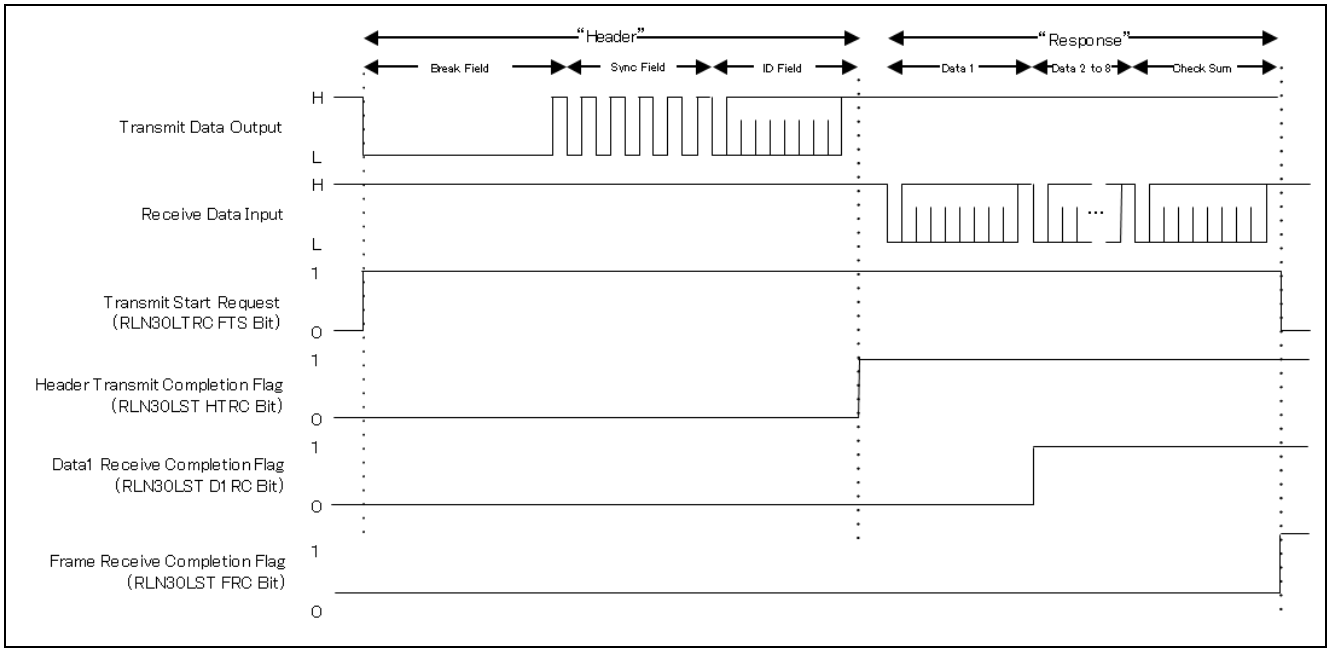

Figure 2-12 Frame Transmit/Receive Operation of Master

The following shows the overview of the operation.

- (1) Start the transmission to set 1 to the transmission start request by the software.
- (2) The transmit completion flag becomes 1 when the "header" transmission is completed.
  At this time, the transmit completion interrupt is generated in this setting example.
- (3) The data 1 receive completion flag becomes 1 when the "data 1" transmission is completed.
- (4) The transmit completion flag becomes 1 when the "response" transmission is completed.
  Also, the transmit start request that is set 1 in sequence (1) becomes 0.
  At this time, the transmit completion interrupt is generated in this setting example.

Figure 2-13 shows the frame transmit/receive operation of the slave.

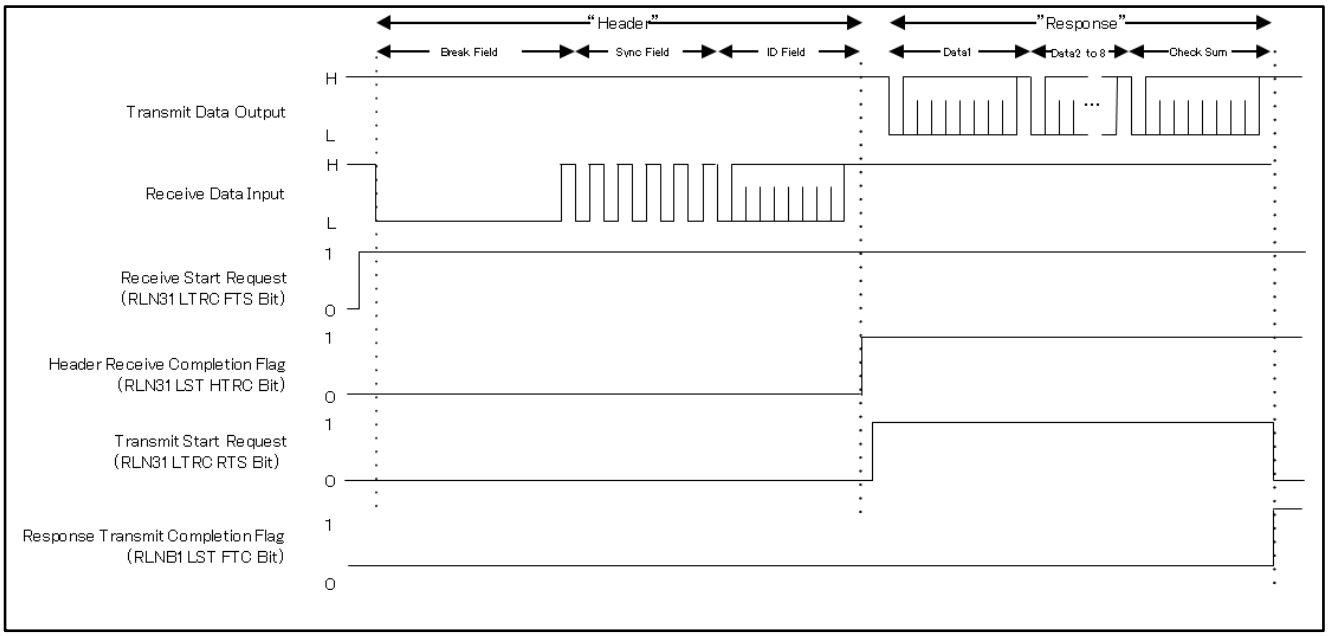

Figure 2-13 Frame Transmit/Receive Operation of Slave

The following shows the overview of the operation.

- (1) Start the transmission to set 1 to the transmission start request by the software.
- (2) The transmit completion flag becomes 1 when the "header" transmission is completed.
  At this time, the transmit completion interrupt is generated in this setting example.
- (3) The response transmission is started by setting 1 to the transmit start request by the software.
- (4) The transmit completion flag becomes 1 when the "response" transmission is completed.
  Also, the transmit start request that is set 1 in sequence (1) becomes 0.
  At this time, the transmit completion interrupt is generated in this setting example.
-

2.2.3 Register Setting

The following shows the setting value of the register and the sample code used in the frame transmit setting.

Table 2-9 shows the register setting value of the transmit/receive port setting.

Table 2-9 Register Setting Value (Port)

Register Name	Setting Value	Function
PCR34_2	0x00000057	Drive strength：very low
		Port mode control: Sharing mode
		Port mode: Input mode
		Port function control: Sharing mode 8 (RLIN30RX)
PCR34_0	0x00000047	Drive strength：very low
		Port output: Low level
		Port mode control: Sharing mode
		Port mode: Output mode
		Port function control: Sharing mode 8 (RLIN30TX)
PCR20_6	0x00000057	Drive strength：very low
		Port mode control: Sharing mode
		Port mode: Input mode
		Port function control: Sharing mode 8 (RLIN31RX)
PCR20_7	0x00000047	Drive strength：very low
		Port output: Low level
		Port mode control: Sharing mode
		Port mode: Output mode
		Port function control: Sharing mode 8 (RLIN31TX)

Table 2-10 shows the register setting value of the communication baud rate setting and the frame configuration setting.

Table 2-10 Register Setting Value (RLIN30 Operation)

Register Name	Setting Value	Function
RLN30LWBR	0x02	Number of bit sampling selection: Select 16 sampling Prescaler division ratio: 1/2
RLN30LBRP0	129	Baud rate prescaler division ratio: 1/(129+1)
RLN30LMD	0x14	Noise filter: Use LIN interrupt output selection: Use transmit completion/ receive completion/status interrupt LIN system clock selection: fb LIN/UART mode selection: LIN master mode
RLN30LBFC	0x00	Transmit break delimiter width: 1Tbit Transmit brake width: 13Tbits
RLN30LSC	0x00	Interbyte space (response) setting: 0Tbit Interbyte space (header) / response space setting: 0Tbit

Table 2-11 shows the register setting value of the communication baud rate setting and the frame configuration setting.

Table 2-11 Register Setting Value (RLIN31 Operation)

Register Name	Setting Value	Function
RLN31LWBR	0x06	Number of bit sampling selection: Select 16 sampling Prescaler division ratio: 1/8
RLN31LBRP01	64	Baud rate prescaler division ratio: 1/(64+1)
RLN31LMD	0x13	Noise filter: Use LIN interrupt output selection: Use transmit completion/ receive completion/status interrupt LIN/UART mode selection: LIN slave mode
RLN31LBFC	0x00	Detect 9.5T bits or 10 Tbits by the break (low level).
RLN31LSC	0x00	Interbyte space (response) setting: 0Tbit Interbyte space (header) / response space setting: 0Tbit

Table 2-12 shows the register setting value of the interrupt controller.

Table 2-12 Register Setting Value (interrupt)

Register Name	Setting Value	Function
EIBD621	0x00000000	Simultaneous notification interrupt enable bit: Disable
		Simultaneous notification interrupt port number setting bit: not necessary
		Host/Guest partition selection bit: Not necessary to set because it corresponds to INTC1 virtualization configuration register (IHVCFG)
		Interrupt bind destination PEID: PE0(CPU0)
EIC621	0x040	Interrupt request flag: No interrupt request
		Interrupt mask bit: No mask
		Interrupt vector method: Table reference method
		Interrupt priority: 0 (highest)
EIBD622	0x00000000	Simultaneous notification interrupt enable bit: Disable
		Simultaneous notification interrupt port number setting bit: not necessary
		Host/Guest partition selection bit: Not necessary to set because it corresponds to INTC1 virtualization configuration register (IHVCFG)
		Interrupt bind destination PEID: PE0(CPU0)
EIC622	0x040	Interrupt request flag: No interrupt request
		Interrupt mask bit: No mask
		Interrupt vector method: Table reference method
		Interrupt priority: 0 (highest)
EIBD623	0x00000000	Simultaneous notification interrupt enable bit: Disable
		Simultaneous notification interrupt port number setting bit: not necessary
		Host/Guest partition selection bit: Not necessary to set because it corresponds to INTC1 virtualization configuration register (IHVCFG)
		Interrupt bind destination PEID: PE0(CPU0)
EIC623	0x040	Interrupt request flag: No interrupt request
		Interrupt mask bit: No mask

		Interrupt vector method: Table reference method
		Interrupt priority: 0 (highest)
EIBD626	0x00000000	Simultaneous notification interrupt enable bit: Disable
		Simultaneous notification interrupt port number setting bit: not necessary
		Host/Guest partition selection bit: Not necessary to set because it corresponds to INTC1 virtualization configuration register (IHVCFG)
		Interrupt bind destination PEID: PE0(CPU0)
EIC626	0x040	Interrupt request flag: No interrupt request
		Interrupt mask bit: No mask
		Interrupt vector method: Table reference method
		Interrupt priority: 0 (highest)
EIBD627	0x00000000	Simultaneous notification interrupt enable bit: Disable
		Simultaneous notification interrupt port number setting bit: not necessary
		Host/Guest partition selection bit: Not necessary to set because it corresponds to INTC1 virtualization configuration register (IHVCFG)
		Interrupt bind destination PEID: PE0(CPU0)
EIC627	0x040	Interrupt request flag: No interrupt request
		Interrupt mask bit: No mask
		Interrupt vector method: Table reference method
		Interrupt priority: 0 (highest)
EIBD628	0x00000000	Simultaneous notification interrupt enable bit: Disable
		Simultaneous notification interrupt port number setting bit: not necessary
		Host/Guest partition selection bit: Not necessary to set because it corresponds to INTC1 virtualization configuration register (IHVCFG)
		Interrupt bind destination PEID: PE0(CPU0)
EIC628	0x040	Interrupt request flag: No interrupt request
		Interrupt mask bit: No mask
		Interrupt vector method: Table reference method
		Interrupt priority: 0 (highest)

Table 2-13 shows the register setting value of the interrupt enable setting and the error detection setting.

Table 2-13 Register Setting Value (Interrupt Enable and Error Detection)

Register Name	Setting Value	Function
RLN30LIE	0xFF	Header transmit interrupt enable bit: Enable
		Error detection interrupt enable bit: Enable
		Frame receive completion interrupt enable bit: Enable
		Frame transmit completion interrupt enable bit: Enable
RLN30LEDE	0x8F	Timeout error selection bit: Response timeout error selection
		Framing error detection enable bit: Enable
		Timeout error detection enable bit: Enable
		Physical bus error detection enable bit: Enable
		Bit error detection enable bit: Enable
RLN31LIE	0xFF	Header transmit interrupt enable bit: Enable
		Error detection interrupt enable bit: Enable
		Frame receive completion interrupt enable bit: Enable

		Frame transmit completion interrupt enable bit: Enable
RLN31LEDE	0xDD	Timeout error selection bit: Response timeout error selection
		ID parity error detection enable bit: Enable
		Sync-field error detection enable bit: Enable
		Framing error detection enable bit: Enable
		Timeout error detection enable bit: Enable
		Bit error detection enable bit: Enable

Table 2-14 shows the register setting value of the mode switching.

Table 2-14 Register Setting Value (RLIN3 Mode)

Register Name	Setting Value	Function
RLN30LCUC	0x03	LIN mode selection bit: LIN operation mode
		LIN reset bit: Release LIN reset mode
RLN31LCUC	0x03	LIN mode selection bit: LIN operation mode
		LIN reset bit: Release LIN reset mode

Table 2-15 shows the register setting value of the frame recieve of RLIN30.

Table 2-15 Register Setting Value (Frame Reception Setting)

Register Name	Setting Value	Function
RLN30LDFC	0x08	Continuous selection bit: Data group that is transmitted/received next is the last Communication direction: Reception Not Frame separate mode Check sum: Classic Response field data length: 8byte+check sum
RLN30LIDB	0x76	Parity bit P1:1 Parity bit P0:1 ID：0x36
RLN30LTRC（FTS）	1	Frame receive/transmit start request

Table 2-16 shows the register setting value of the frame transmit of RLIN31.

Table 2-16 Register Setting Value (Frame Transmit Setting)

Register Name	Setting Value	Function
RLN31LDFC	0x18	Continuous selection bit: Data group that is transmitted/received next is the last Communication direction: Transmission Check sum: Classic Response field data length: 8byte+check sum
RLN31LTRC（FTS）	1	Header receive start request
RLN31LTRC（RTS）	1	Response transmit/receive start request

2.2.4 Sample Code

Table 2-17 shows the global variable of the sample code.

Table 2-17 Global Variable List

Variable Name	Size	Contents
g_rcvdata[10]	1byte × 10	Save the received response to the index 1 to 9 when the frame receive completion interrupt is generated. (The index 0 is not used)
g_errstatus	1byte	When the status interrupt is generated, save the error status if the error is generated. (RLN30LEST register value)

Table 2-18 shows the function list of the sample code.

Table 2-18 Function List

Module Name	Function Name	Function
Maine function	main_pe0	Main processing for LIN. After performing the initial setting, perform the communication start request and it becomes the interrupt waiting status.
RLIN30 initial setting function	Init_RLIN30M	Perform the initial setting for performing the communication processing.
RLIN31 initial setting function	Init_RLIN31M	Perform the initial setting for performing the communication processing.
RLIN30LIN frame communication start function	Start_RLIN30Frame	Perform the communication setting of the header and the response.
RLIN31LIN frame communication start function	Start_RLIN31Frame	Perform the communication setting of the header and the response.
PID calculation processing function	get_pid	Calculate PID form the frame.
RLIN30 error detection interrupt function	eiint623	Perform the interrupt processing when detecting the error.
RLIN30 receive completion interrupt function	eiint622	Perform the receive completion interrupt processing of LIN frame.
RLIN30 transmit completion interrupt function	eiint621	Perform the transmit completion interrupt processing of LIN frame.
RLIN31 error detection interrupt function	eiint628	Perform the interrupt processing when detecting the error.
RLIN31 receive completion interrupt function	eiint627	Perform the receive completion interrupt processing of LIN frame.
RLIN31 transmit completion interrupt function	eiint626	Perform the transmit completion interrupt processing of LIN frame.

Figure 2-14 shows the flowchart of the main function.

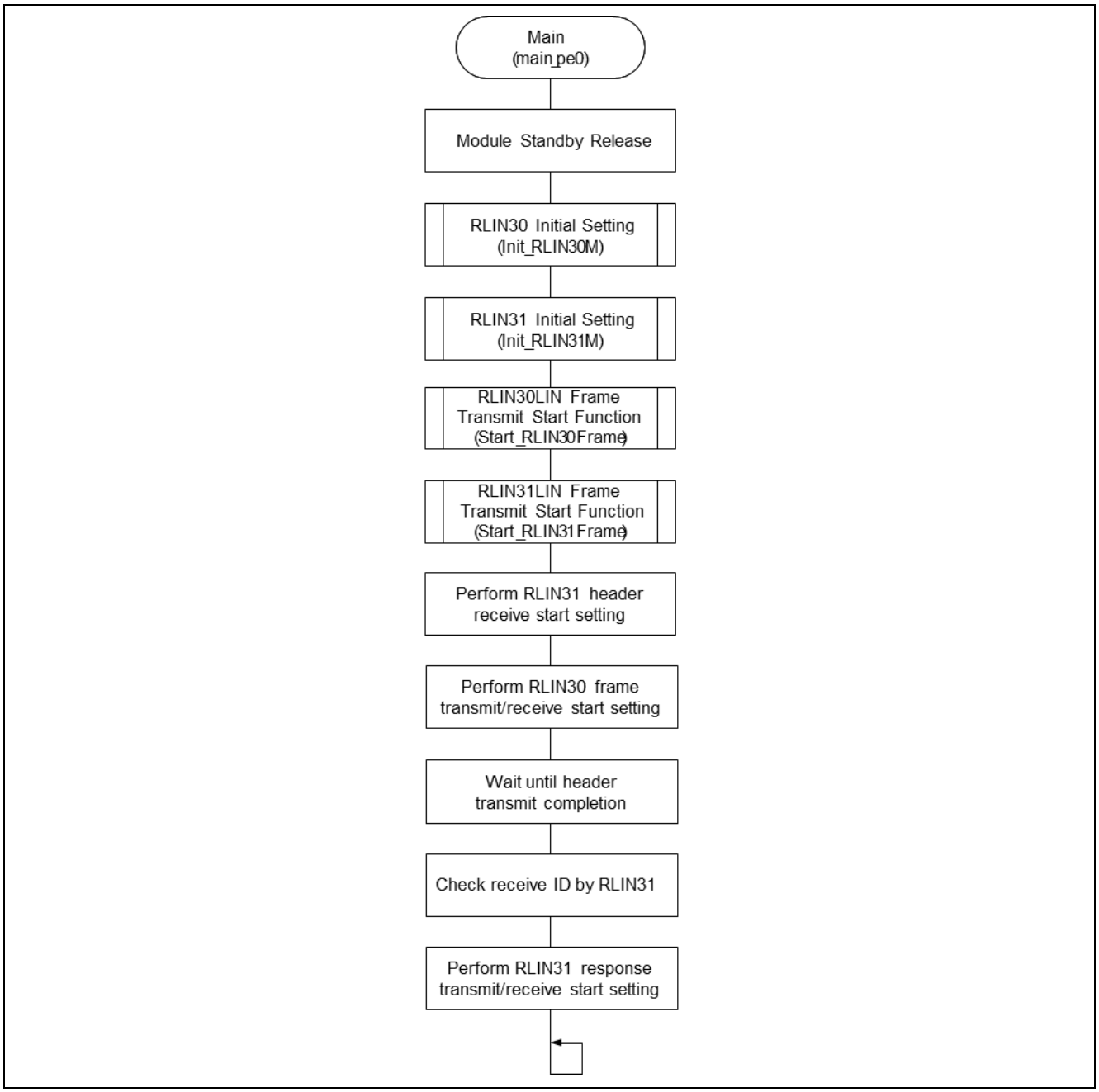

Figure 2-14 Main

Figure 2-15 shows the initial setting function of RLIN30.

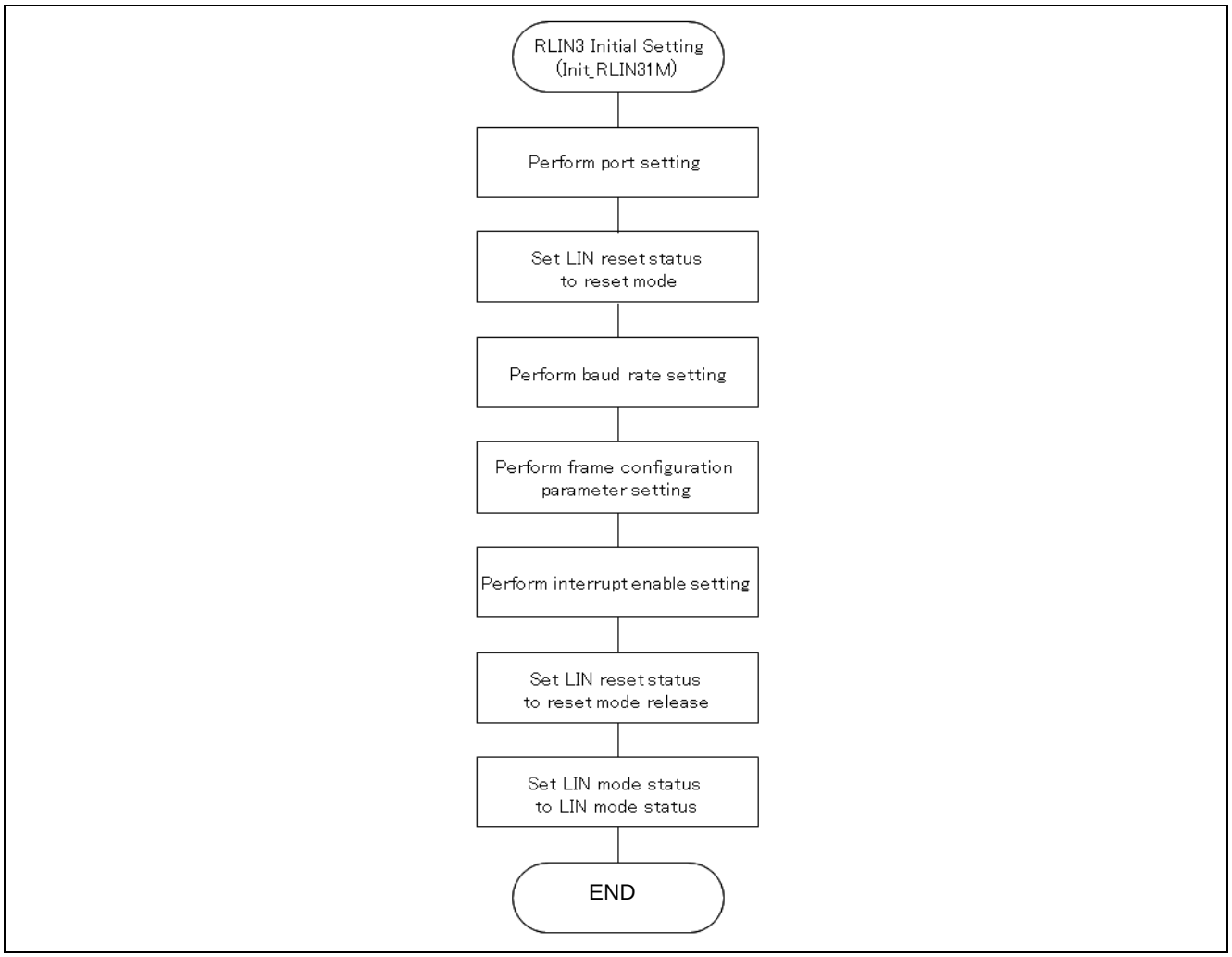

Figure 2-15 RLIN30 Initial Setting

Figure 2-16 shows the flowchart of the RLIN31 initial setting function.

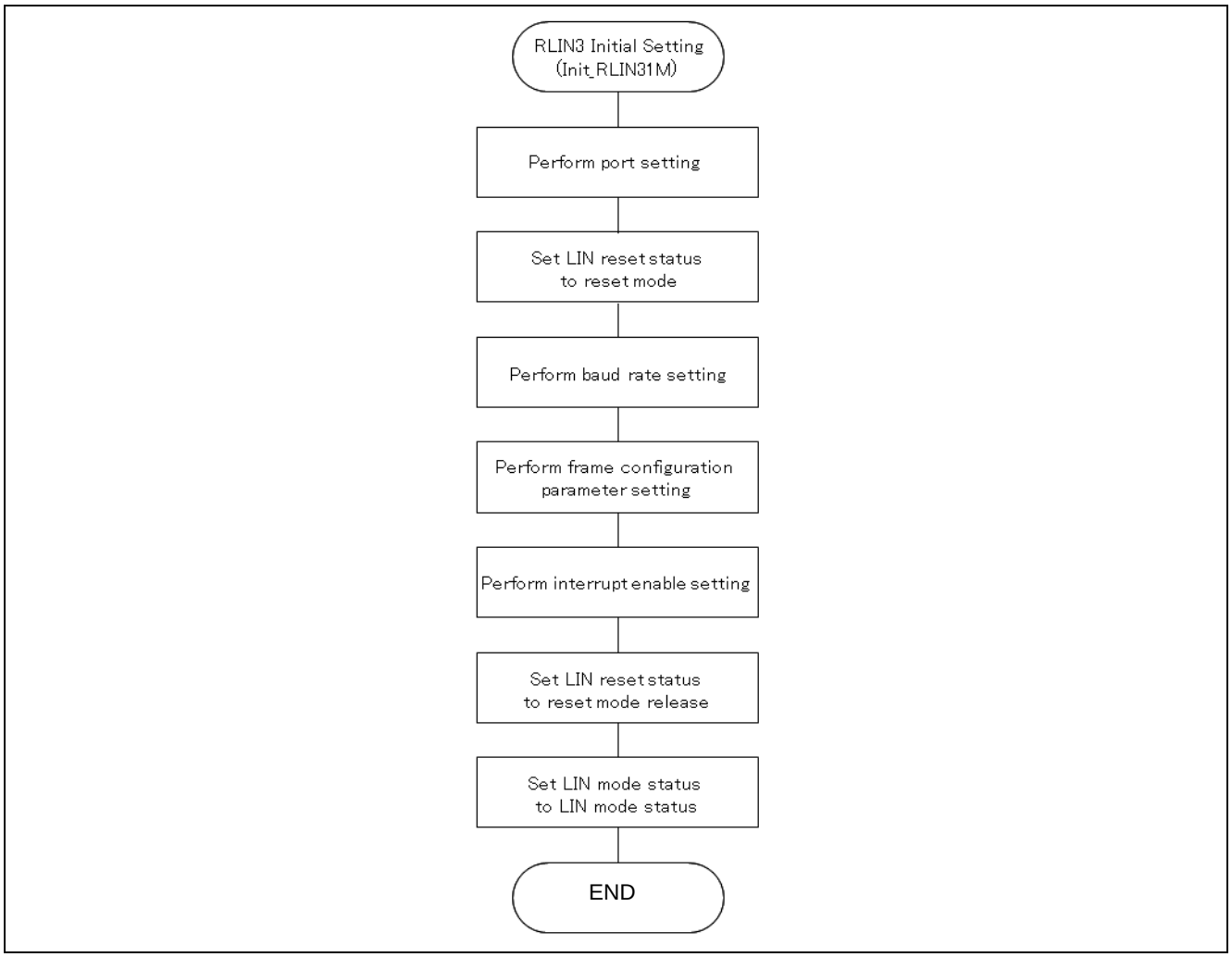

Figure 2-16 RLIN Initial Setting

Figure 2-17 shows the flowchart of RLIN30 frame communication start function.

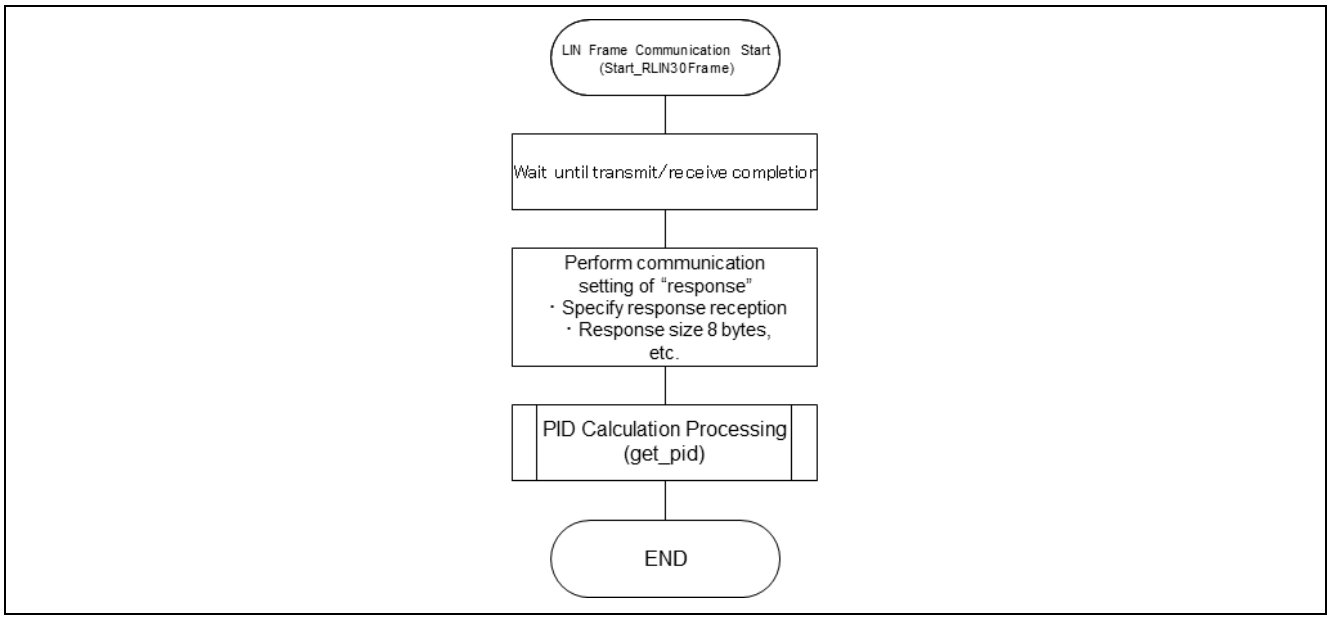

Figure 2-17 LIN Frame Communication Start

Figure 2-18 shows the flowchart of RLIN31 frame communication start function.

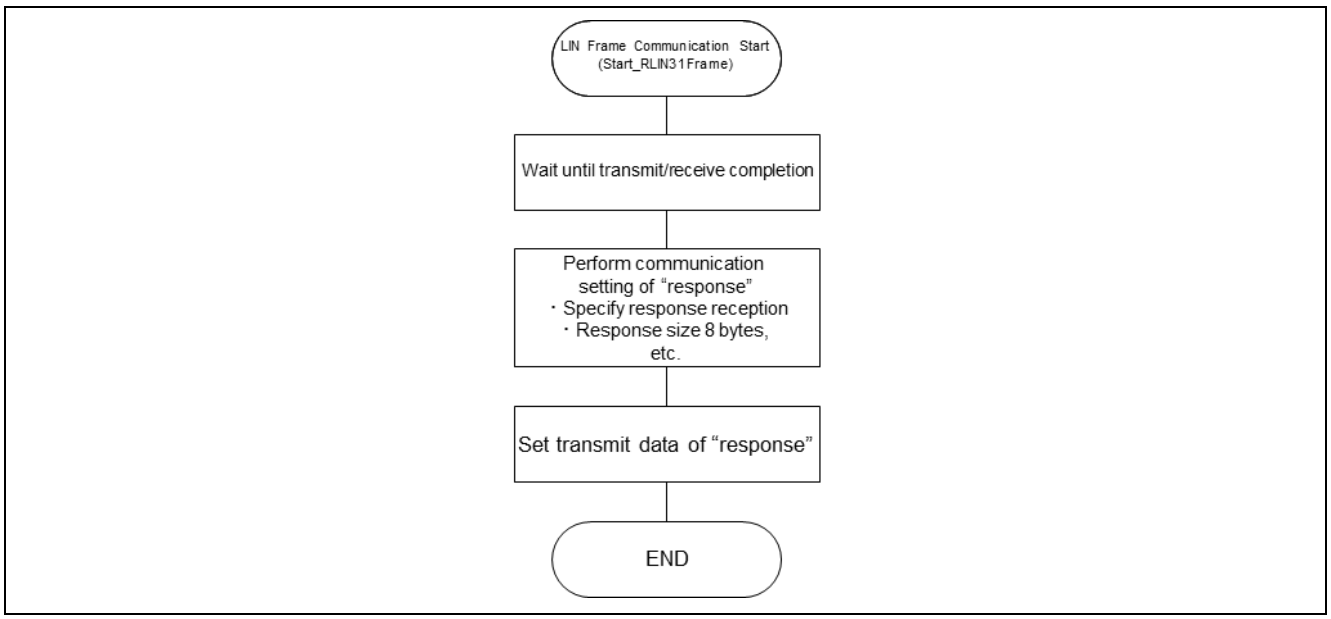

Figure 2-18 LIN Frame Communication Start

Figure 2-19 shows the flowchart of the PID calculation function.

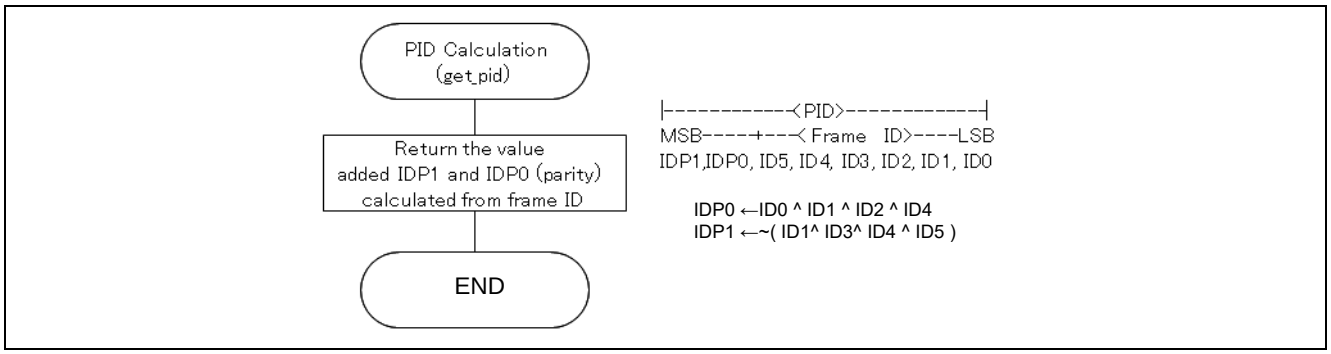

Figure 2-19 PID Calculation

Figure 2-20 shows the flowchart of the RLIN30 transmit completion/receive completion/error detection interrupt function.

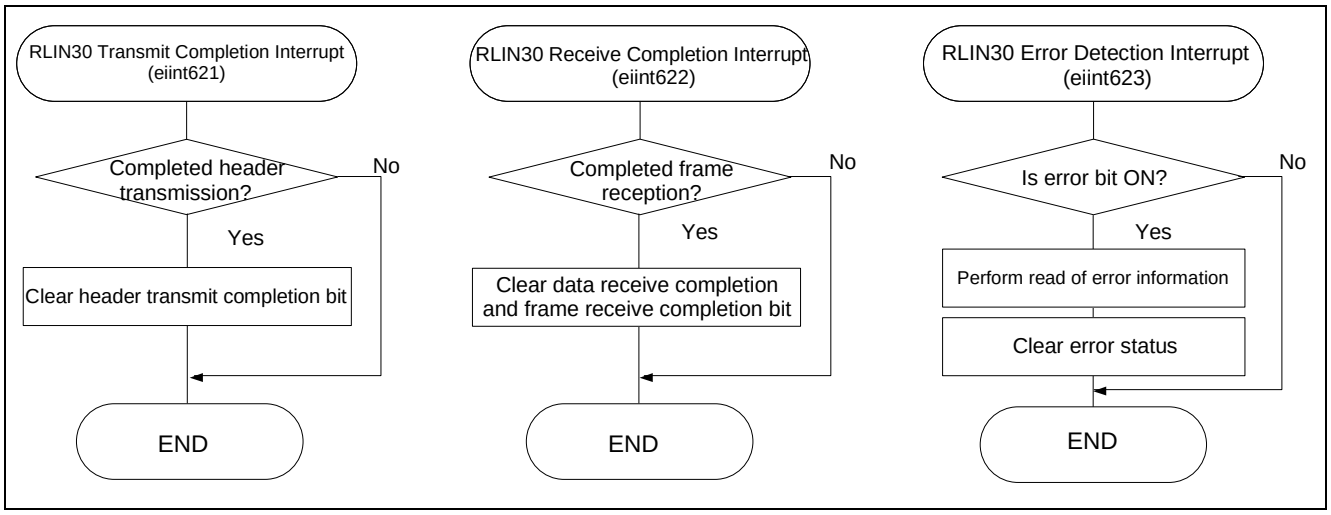

Figure 2-20 RLIN30 Interrupt

Revision History

Rev.	Data	Description	
		Page	Summary
1.00	2023.3.16	—	Initial issue
1.10	2024.2.22	1	Target Integrated Development Environment and Reference Document is changed

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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