RH850/U2B

UVW phase PWM output using GTM

Introduction

This application note describes how to perform U / V / W phase PWM output using the RH850 / U2Bx series.

Target Device

RH850/U2Bx

When applying this application note to another microcomputer, change it according to the specifications of that microcomputer and evaluate it sufficiently.

Contents

1. Introduction

This application note provides an implementation example of U / V / W phase PWM output using the RH850 / U2B Generic Timer Module (GTM).

1.1 Functions

The hardware functions of the RH850 / U2B used in this application note are shown below.

Generic Timer Module (GTM)

2. Operation example

2.1 Three-phase PWM output (method without using the dead time function of DTM)

2.1.1 Specification overview

This operation example uses ATOM of GTM to output complemented 3-phase PWM.

Set the carrier cycle to 125us (8kHz) and dead time to 2.5µs, and update the duty with a valley interrupt.

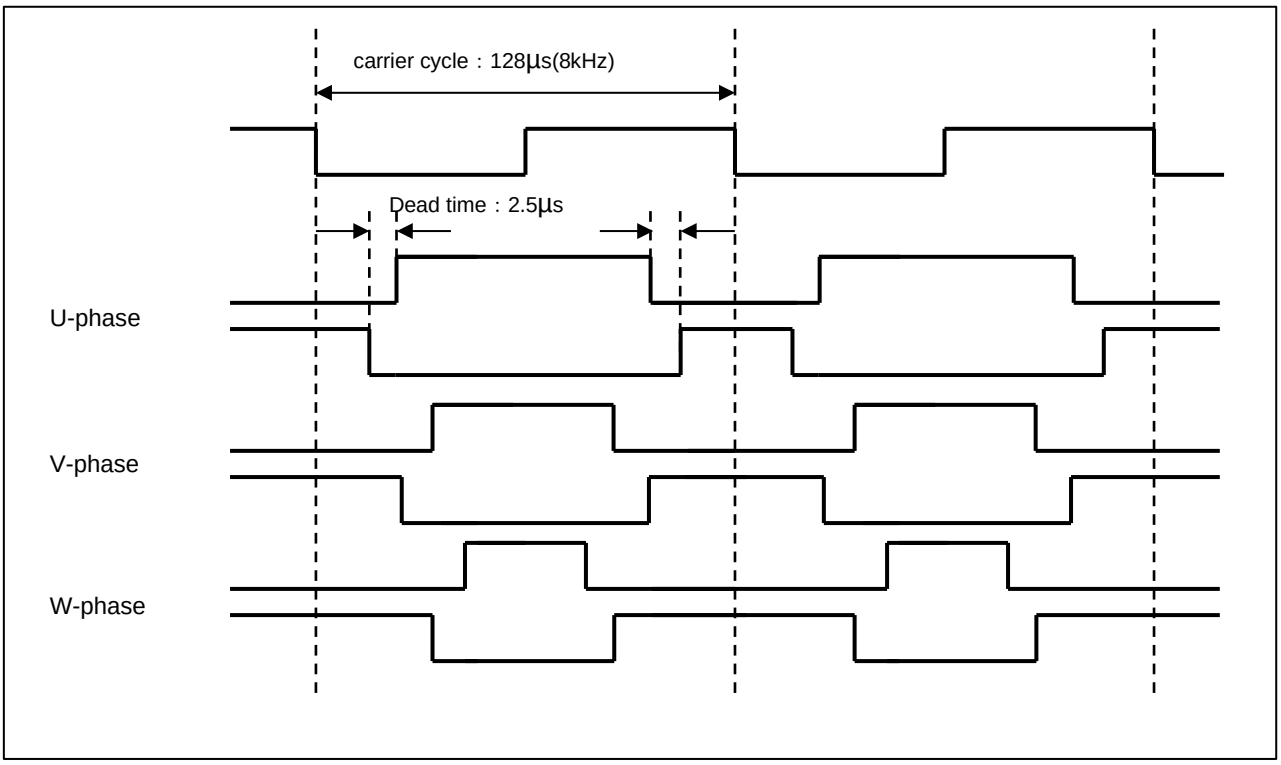

Figure 2.1 Schematic

2.1.2 Operating Conditions of Features Used

Operating conditions of features used in this operation example are shown below.

Table 2.1 Port Settings

Item	Description
Ports to be used	P12_0 : ATOM0_CH0_OUT P12_1 : ATOM0_CH1_OUT P12_2 : ATOM0_CH2_OUT P12_3 : ATOM0_CH3_OUT P12_4 : ATOM0_CH0_OUT_N P12_5 : ATOM0_CH1_OUT_N P12_6 : ATOM0_CH2_OUT_N P12_7 : ATOM0_CH3_OUT_N

Table 2.2 Interrupt Feature Settings

Item	Description
Cycle interrupt	Table reference method, Priority 15

Table 2.3 GTM(common) setting

Item	Description
Main clock	160MHz
Use cluster	Cluster 0
Skipping rate	1/2
Interrupt	ATOM0_CH0 cycle interrupt

Table 2.4 GTM(CMU) setting

Item	Description
Skipping rate into the cluster	1/1

Table 2.5 GTM(ARU) setting

Item	Description
Reload control with cycle interrupts	Reload with cycle interrupts

Table 2.6 GTM(ATOM) setting

Item	Description
Carrier cycle	125µs
Use mode	SOCP mode
Up/down counter mode	Used (valley update)

Table 2.7 GTM(DTM) setting

Item	Description
Dead time	0µs
Input and output signal	Output DTM_IN to DTM_OUT Invert DTM_IN_T and output to DTM_OUT_N

2.1.3 Operating

In this operation example, INTGTM000 interrupt (valley interrupt) is enabled and reload operation at valley timing is enabled. The INTGTM000 interrupt updates the duty of the complementary three-phase PWM output. At the next reload timing, the update value is transferred to the compare register (CH0_CM1, CH1_SR1, CH2_SR1), and the duty of the complementary three-phase PWM output changes.

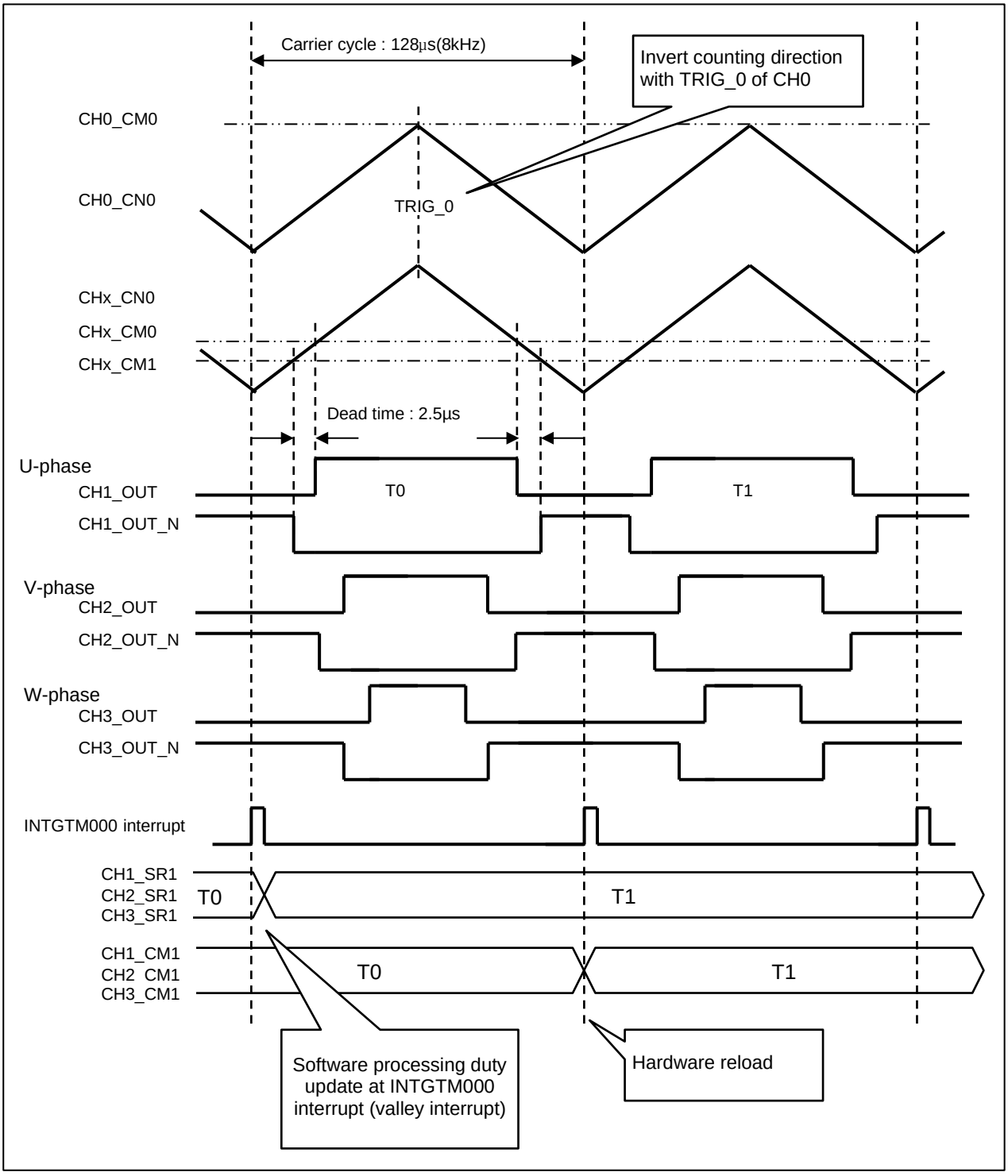

Figure 2.2 Operation explanation

2.1.4 Description of Software

Table 2.8 to Table 2.15 show setting examples of each register used in this operation example.

Table 2.8 Port setting

Register Name	Set Value	Description
PCR12_0	0x0000004D	ATOM0ch0 output
PCR12_1	0x0000004D	ATOM0ch1 output
PCR12_2	0x0000004D	ATOM0ch2 output
PCR12_3	0x0000004D	ATOM0ch3 output
PCR12_4	0x0000004D	ATOM0ch0_N output
PCR12_5	0x0000004D	ATOM0ch1_N output
PCR12_6	0x0000004D	ATOM0ch2_N output
PCR12_7	0x0000004D	ATOM0ch3_N output

Table 2.9 INTC2 setting

Register Name	Set Value	Description
EIC086	0x804F	Enable ch0 to ch2

Table 2.10 GTM common setting

Register Name	Set Value	Description
GTM_CLS_CLK_CFG	0x00000015	Select whether to supply the clock to each cluster
GTM_IRQ_SEL000	0x00080000	Enable to ATOM0 CH3 interrupt output

Table 2.11 CMU setting

Register Name	Set Value	Description
CMU_CLK_EN	0x0000002A	Enable ch0 to ch2
CMU_GCLK_NUM	0x00000001	Default value. Don’t change the frequency division.
CMU_GCLK_DEN	0x00000001	Default value. Don’t change the frequency division.
CMU_CLK_0_CTRL	0x00000000	Default value. Don’t change the frequency division.
CMU_CLK_1_CTRL	0x00000000	Default value. Don’t change the frequency division.
CMU_CLK_2_CTRL	0x00000000	Default value. Don’t change the frequency division.
CMU_CLK_CTRL	0x00000000	Default value.

Table 2.12 ATOM unit setting

Register Name	Set Value	Description
ATOM0_AGC_GLB_CTRL	0x00550000	Enable reloading of CM0, CM1, SL, CLK_SRC from ch0 to ch3
ATOM0_AGC_ENDIS_CTRL	0x000000AA	Enable ch0 to ch3
ATOM0_AGC_OUTEN_CTRL	0x000000AA	Enable channel output ch0 to ch3
ATOM0_AGC_FUPD_CTRL	0x005500AA	Enable forced update of CN0 ch0 to ch3
ATOM0_AGC_INT_TRIG	0x000000AA	Enable interrupt trigger ch0 to ch3

Table 2.13 ATOM CH0 setting

Register Name	Set Value	Description
ATOM0_CH0_CTRL	0x01040802	Select SOMP mode Select High as the initial signal level Select CM0 compare match as reset trigger Select TRIG_CCU0 as trigger output
ATOM0_CH0_CN0	0x00000000	Counter starts at 0
ATOM0_CH0_CM0	0x00001388	Since CN0 goes up and down by 1, set a value that is half of the target cycle.
ATOM0_CH0_SR0	0x00001388	
ATOM0_CH0_CM1	0x000009A4	Set 1/4 of target period
ATOM0_CH0_SR1	0x000009A4	
ATOM0_CH0_IRQ_NOTIFY	0x00000003	Clear interrupt source
ATOM0_CH0_IRQ_EN	0x00000003	Enable interrupt

Table 2.14 ATOM CH1 to CH3 setting

Register Name	Set Value	Description
ATOM0_CHx_CTRL	0x00140002	Select SOMP mode Select High as the initial signal level Select up / down mode (valley update) Select TRIG_[x-1] for reset trigger Select TRIG_[x-1] for trigger output
ATOM0_CHx_CN0	0x00000000	Counter starts at 0
ATOM0_CHx_CM0	0x00001388	Compare value for positive phase output. Set the value to 0%.
ATOM0_CHx_SR0	0x00001388	
ATOM0_CHx_CM1	0x00000001	A compare value for the output. Set to a non-zero value for initial compare match
ATOM0_CHx_SR1	0x00000001	
ATOM0_CHx_IRQ_NOTIFY	0x00000003	Clear interrupt source
ATOM0_CHx_IRQ_EN	0x00000000	Disable interrupt

Table 2.15 DTM setting

Register Name	Set Value	Description
CDTM0_DTM4_CTRL	0x00000001	Do not update CTRL2 Clock selects CMU_CLK0
CDTM0_DTM4_CH_CTRL1	0x31313100	Route DTM_IN_T to DTM_OUT_N
CDTM0_DTM4_CH_CTRL2	0x98989800	Set DTM_IN to DTM_OUT Let DTM_IN_T be DTM_OUT_N DTM_IN_T is inverted
CDTM0_DTM4_CH_CTRL3	0x00000000	Default value
CDTM0_DTM4_CH0_DTV	0x00000000	Set 0 because the dead time function of DTM is not used.
CDTM0_DTM4_CH1_DTV	0x00000000	
CDTM0_DTM4_CH2_DTV	0x00000000	
CDTM0_DTM4_CH0_DTV_SR	0x00000000	
CDTM0_DTM4_CH1_DTV_SR	0x00000000	
CDTM0_DTM4_CH2_DTV_SR	0x00000000	

2.1.5 Operation Flow

The flowchart of this operation example is shown below.

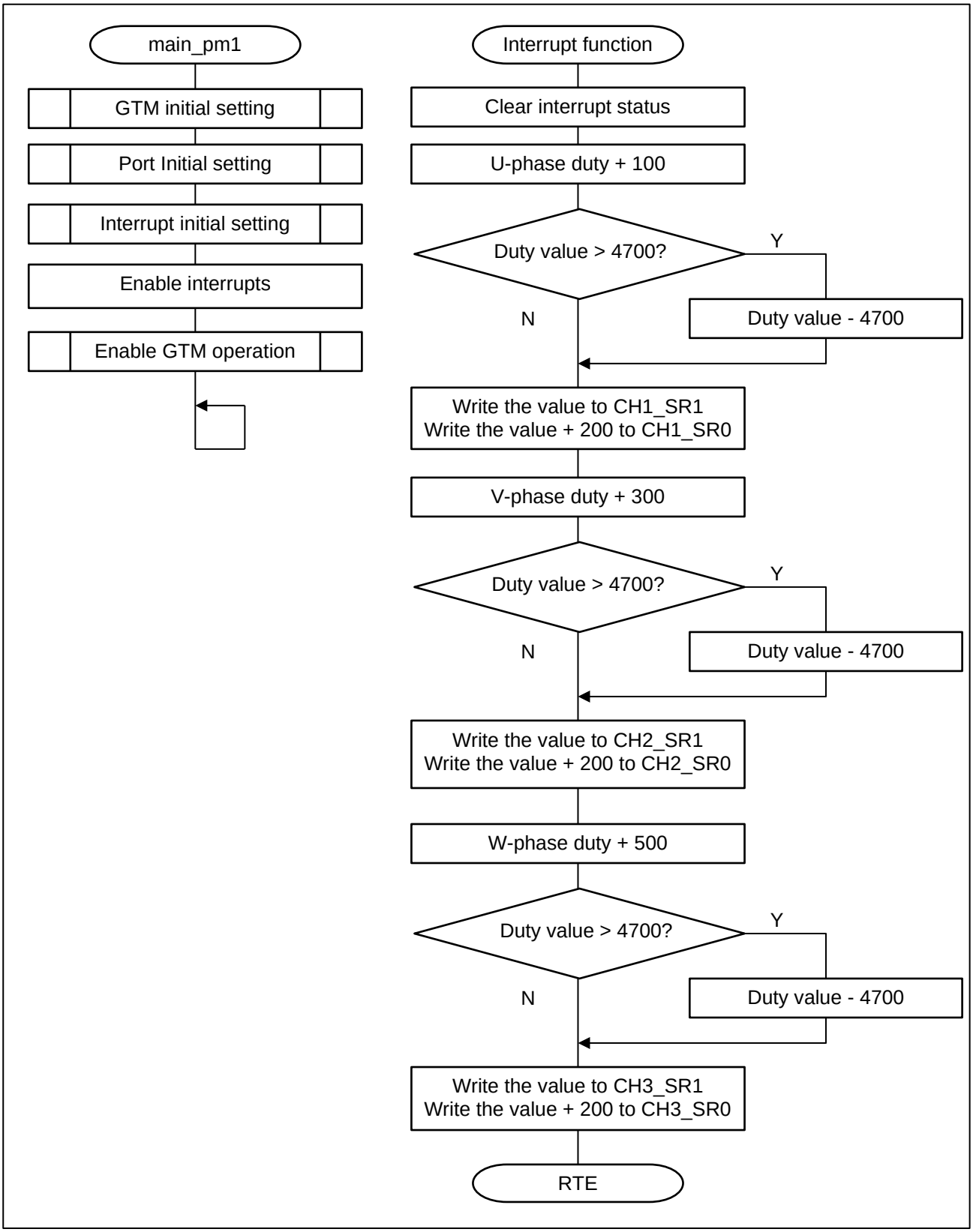

Figure 2.3 Operation flow

2.2 Three-phase PWM output (method with using the dead time function of DTM)

2.2.1 Specification overview

This operation example uses ATOM of GTM to output complemented 3-phase PWM.

Set the carrier cycle to 125us (8kHz) and dead time to 2.5µs, and update the duty with a valley interrupt.

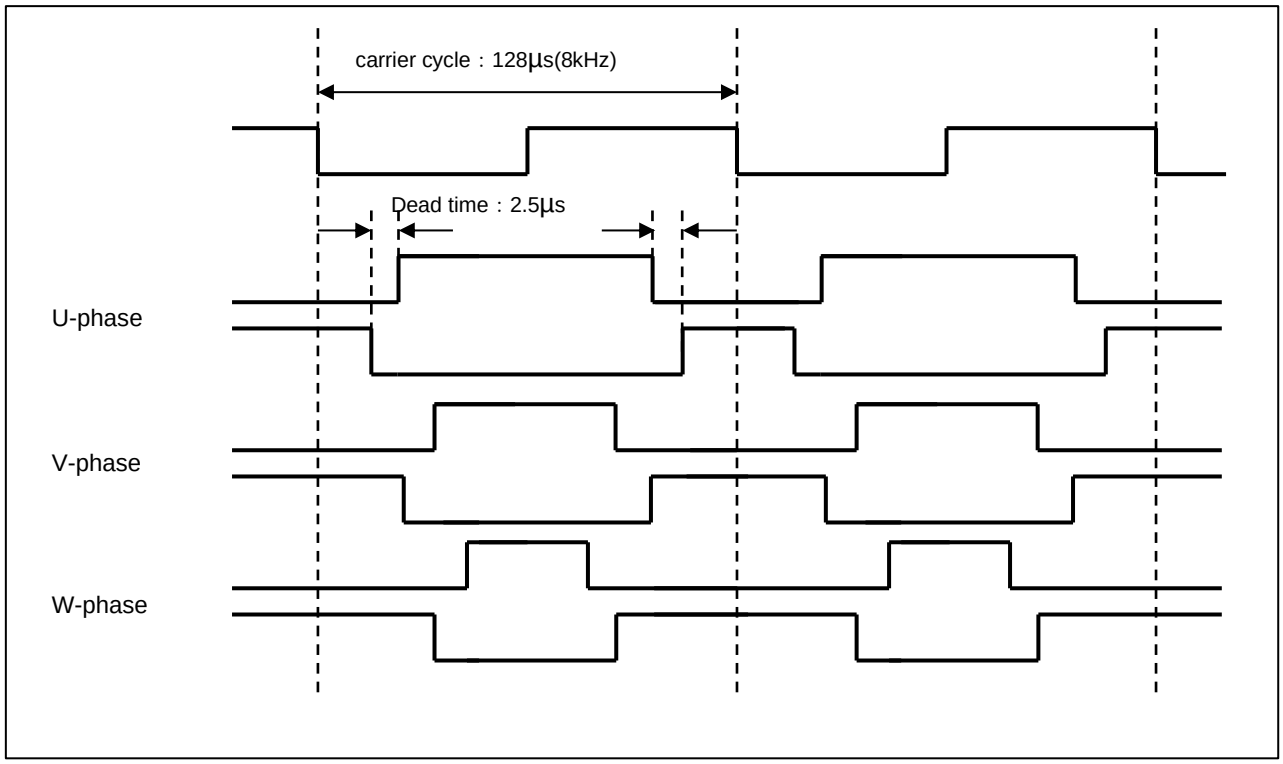

Figure 2.4 Schematic

2.2.2 Operating Conditions of Features Used

Operating conditions of features used in this operation example are shown below.

Table 2.16 Port Settings

Item	Description
Ports to be used	P12_0 : ATOM0_CH0_OUT P12_1 : ATOM0_CH1_OUT P12_2 : ATOM0_CH2_OUT P12_4 : ATOM0_CH0_OUT_N P12_5 : ATOM0_CH1_OUT_N P12_6 : ATOM0_CH2_OUT_N

Table 2.17 Interrupt Feature Settings

Item	Description
Cycle interrupt	Table reference method, Priority 15

Table 2.18 GTM(common) setting

Item	Description
Main clock	160MHz
Use cluster	Cluster 0
Skipping rate	1/2
Interrupt	ATOM cycle interrupt

Table 2.19 GTM(CMU) setting

Item	Description
Skipping rate into the cluster	1/1

Table 2.20 GTM(ATOM) setting

Item	Description
Carrier cycle	125µs
Use mode	SOCP mode
Up/down counter mode	Used (valley update)

Table 2.21 GTM(DTM) setting

Item	Description
Dead time	2.5µs
Input and output signal	Dead time function for DTM_IN

2.2.3 Operating

In this operation example, INTGTM000 interrupt (valley interrupt) is enabled and reload operation at valley timing is enabled. The INTGTM000 interrupt updates the duty of the complementary three-phase PWM output. At the next reload timing, the update value is transferred to the compare register (CH0_CM1, CH1_CM1, CH2_CM1), and the duty of the complementary three-phase PWM output changes.

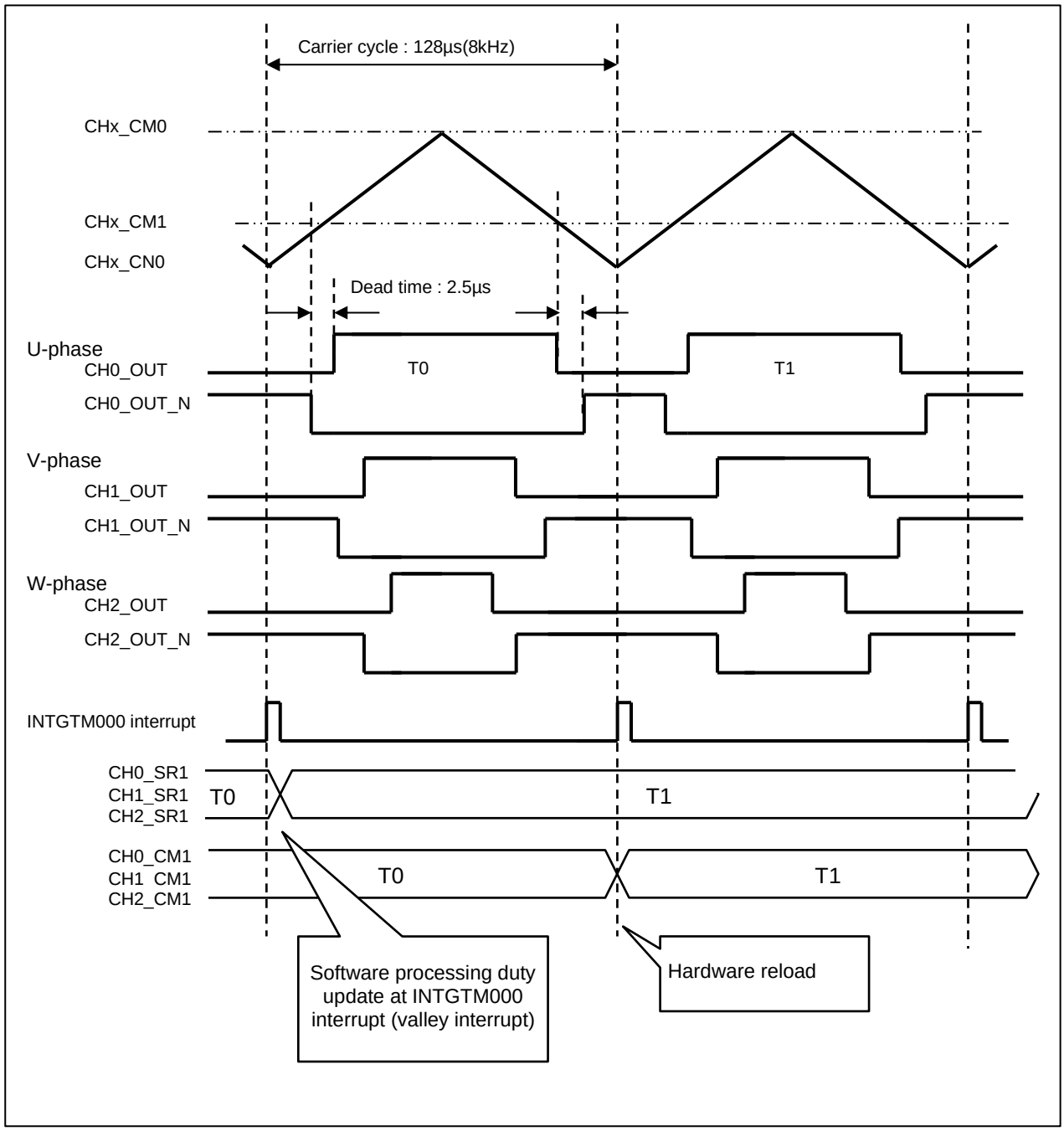

Figure 2.5 Operation explanation

2.2.4 Description of Software

Table 2.22 to Table 2.28 show setting examples of each register used in this operation example.

Table 2.22 Port setting

Register Name	Set Value	Description
PCR12_0	0x0000004D	ATOM0ch0 output
PCR12_1	0x0000004D	ATOM0ch1 output
PCR12_2	0x0000004D	ATOM0ch2 output
PCR12_4	0x0000004D	ATOM0ch0_N output
PCR12_5	0x0000004D	ATOM0ch1_N output
PCR12_6	0x0000004D	ATOM0ch2_N output

Table 2.23 INTC2 setting

Register Name	Set Value	Description
EIC086	0x804F	Enable ch0 to ch2

Table 2.24 GTM common setting

Register Name	Set Value	Description
GTM_CLS_CLK_CFG	0x00000015	Select whether to supply the clock to each cluster
GTM_IRQ_SEL000	0x00010000	Enable to ATOM0 CH0 interrupt output

Table 2.25 CMU setting

Register Name	Set Value	Description
CMU_CLK_EN	0x0000002A	Enable ch0 to ch2
CMU_GCLK_NUM	0x00000001	Default value. Don’t change the frequency division.
CMU_GCLK_DEN	0x00000001	Default value. Don’t change the frequency division.
CMU_CLK_0_CTRL	0x00000000	Default value. Don’t change the frequency division.
CMU_CLK_1_CTRL	0x00000000	Default value. Don’t change the frequency division.
CMU_CLK_2_CTRL	0x00000000	Default value. Don’t change the frequency division.
CMU_CLK_CTRL	0x00000000	Default value.

Table 2.26 ATOM unit setting

Register Name	Set Value	Description
ATOM0_AGC_GLB_CTRL	0x00150000	Enable reloading of CM0, CM1, SL, CLK_SRC from ch0 to ch2
ATOM0_AGC_ENDIS_CTRL	0x0000002A	Enable ch0 to ch2
ATOM0_AGC_OUTEN_CTRL	0x0000002A	Enable channel output ch0 to ch2
ATOM0_AGC_FUPD_CTRL	0x0015002A	Enable forced update of CN0 ch0 to ch2
ATOM0_AGC_INT_TRIG	0x0000002A	Enable interrupt trigger ch0 to ch2

Table 2.27 ATOM CH0 to CH2 setting

Register Name	Set Value	Description
ATOM0_CHx_CTRL	0x01040002	Select SOMP mode Select High as the initial signal level Select CM0 compare match as reset trigger Select TRIG_CCU0 as trigger output
ATOM0_CHx_CN0	0x00000000	Counter starts at 0
ATOM0_CHx_CM0	0x00001388	Since CN0 goes up and down by 1, set a value that is half of the target cycle.
ATOM0_CHx_SR0	0x00001388	
ATOM0_CHx_CM1	0x00000001	A compare value for the output. Set to a non-zero value for initial compare match
ATOM0_CHx_SR1	0x00000001	
ATOM0_CHx_IRQ_NOTIFY	0x00000003	Clear interrupt source
ATOM0_CHx_IRQ_EN	0x00000003	Enable interrupt

Table 2.28 DTM setting

Register Name	Set Value	Description
CDTM0_DTM4_CTRL	0x00000001	Do not update CTRL2 Clock selects CMU_CLK0
CDTM0_DTM4_CH_CTRL1	0x00000000	Do not route DTM_IN_T to DTM_OUT_N
CDTM0_DTM4_CH_CTRL2	0x00888888	Use dead time function from ch0-ch2
CDTM0_DTM4_CH_CTRL3	0x00000000	Default value
CDTM0_DTM4_CH0_DTV	0x00CB00CB	Set 2.5us dead time on both edges
CDTM0_DTM4_CH1_DTV	0x00CB00CB	
CDTM0_DTM4_CH2_DTV	0x00CB00CB	
CDTM0_DTM4_CH0_DTV_SR	0xC0CBC0CB	Set 2.5us reload value on both edges
CDTM0_DTM4_CH1_DTV_SR	0xC0CBC0CB	
CDTM0_DTM4_CH2_DTV_SR	0xC0CBC0CB	

2.2.5 Operation Flow

The flowchart of this operation example is shown below.

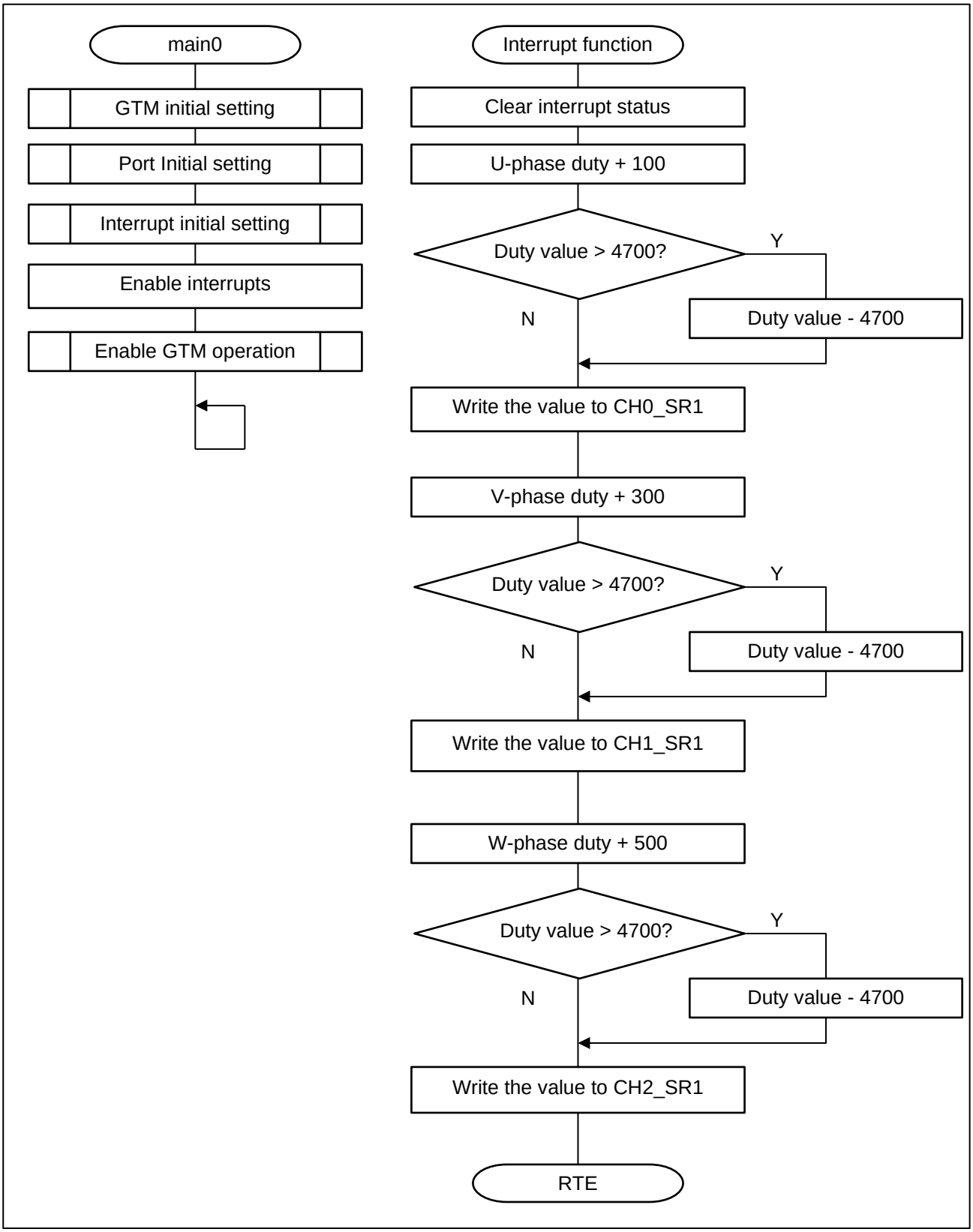

Figure 2.6 Operation flow

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2022.10.05	-	First edition

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2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
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   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
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   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
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   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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