RL78/G13

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Timer Array Unit (Pulse Interval Measurement (Both edges) CC-RL

Introduction

This application note describes how the timer array unit measures time intervals between pulses. This unit detects both the rising and falling edges of the pulses that are input to the timer input pin (TI00) and measures the high-level width and low-level width of the signal to determine the time intervals between pulses. The unit stores the measurement results in the RAM.

Target Device

RL78/G13

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

This application note describes the measurement of the high-level width and low-level width of the input pulse by using channel 0 of the timer array unit 0 (TAU0).

Each time a valid edge is detected on the timer input pin (TI00), the count value of the timer is captured to measure the pulse interval. The measurement result is stored in the on-chip RAM. The type of the detected edge is determined by reading the input data in the P0 register when a valid edge is detected on the timer input pin (TI00).

Table 1.1 shows the required peripheral functions and applications. Figure 1.1 presents an overview of the pulse interval measurement.

Table 1.1 Peripheral Functions and Applications

Peripheral Function	Application
Timer array unit 0 (TAU0) channel 0	Measurement of the interval of the pulse input to the timer input pin (TI00)
TI00	Input pin for pulse signals

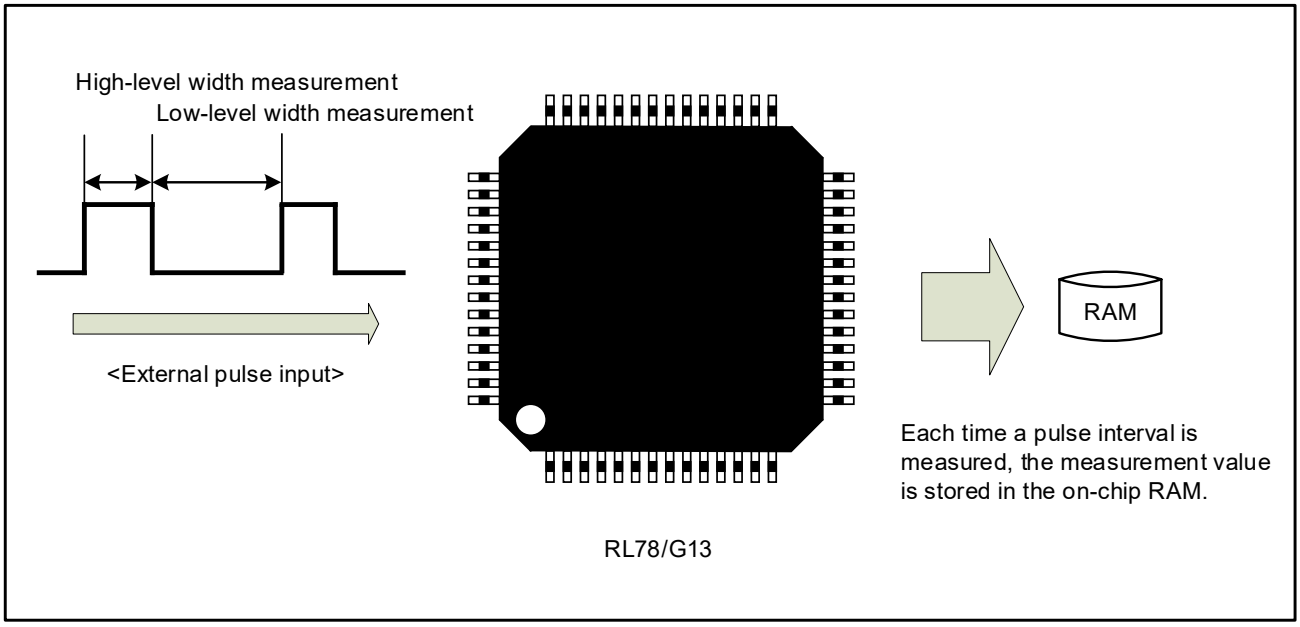

Figure 1.1 Overview of Pulse Interval Measurement

2. Operation Confirmation Conditions

The operation of the sample code provided with this application note has been tested under the following conditions.

Table 2.1 Operation Confirmation Conditions

Item	Description
MCU used	RL78/G13 (R5F100LEA)
Board used	RL78/G13 (R5F100LE) Target Board (QB-R5F100LE-TB)
Operating frequency	High-speed on-chip oscillator clock: 32 MHz CPU/peripheral hardware clock: 32 MHz
Operating voltage	3.3 V (can be operated at 2.7 V to 5.5 V) LVD detection voltage: Reset mode At rising edge TYP. 2.81 V (2.76 V to 2.87 V) At falling edge TYP. 2.75 V (2.70 V to 2.81 V)
Integrated development environment (CS+)	CS+ V8.06.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.10.00 from Renesas Electronics Corp.
Integrated development environment (e2studio)	e2 studio V2021-07 (21.7.0) from Renesas Electronics Corp.
C compiler (e2studio)	CC-RL V1.10.00 from Renesas Electronics Corp.
Code Generator Plug-in	CS+ Code Generator for RL78 (CS+ for CC) V2.21.00 from Renesas Electronics Corp.

3. Related Application Note

Application notes related to this document are shown below. Please refer to these as needed.

- RL78/G13 Initialization CC-RL（R01AN2575E）Application Note
- RL78/G13 Timer Array Unit (Pulse Interval Measurement) CC-RL（R01AN2702E）Application Note

4. Hardware Explanation

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration used in the application note.

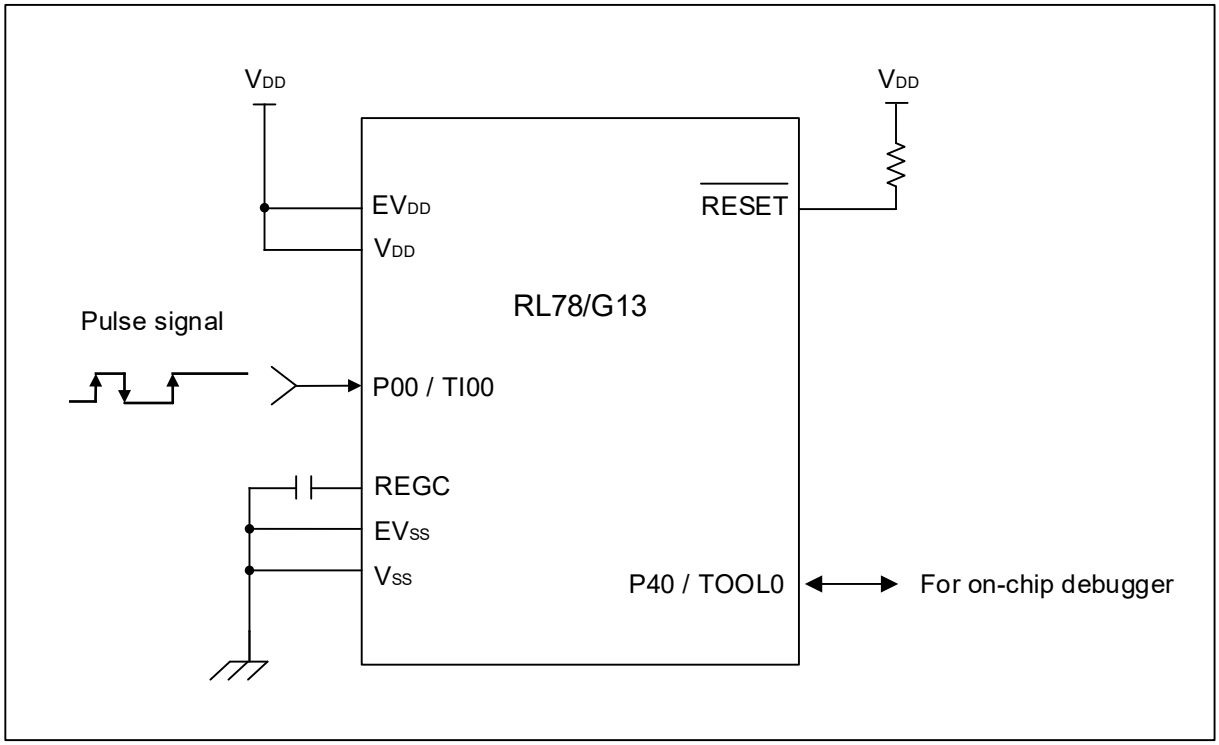

Figure 4.1 Hardware Configuration

Notes: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to VDD or V_{SS} via a resistor).
2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

4.2 Used Pin List

Table 4.1 provides List of Pins and Functions.

Table 4.1 List of Pins and Functions

Pin name	I/O	Function
P00 / TI00	Input	Timer input pin of Timer array unit 0 channel 0

5. Software Explanation

5.1 Operation Outline

In this sample code, each time a rising edge or a falling edge is detected on the timer input pin (TI00), the counter value of the timer is captured and a high-level width or a low-level width of the pulse input to the timer input pin (TI00) is measured.

To measure the pulse interval accurately, the capture end interrupts (INTTM00) of Timer array unit 0 channel 0 after the first capture end interrupt are used. When capture end interrupts occur after the first capture end interrupt, the type of the detected edge (rising or falling) is determined, and the determination result is reflected in the edge determination flag. Then, according to the edge determination flag, the measured high-level width or low-level width is stored in the appropriate variable in the on-chip RAM.

Note that if a short pulse is detected and a counter value of the timer is captured before the measurement result is stored in the variable in the on-chip RAM, the measurement result is discarded.

(1) Initialize Timer Array Unit (TAU0)

- Use the P00/TI00 pin for inputting capture trigger.
- Set the operation clock of TAU0 channel 0 to f_{CLK}.
- Set TAU0 channel 0 to the capture mode.
- Set the TI00 pin input valid edge to “Both edges”.
- Set the capture trigger of TAU0 channel 0 to “Valid edge of the TI00 pin input”.
- Use the capture end interrupt (INTTM00) from TAU0 channel 0.

(2) Set the TS00 bit of the timer channel start register 0 (TS0) to 1 to enable count operation. This clears the timer count register (TCR00) to 0000H and starts counting.

(3) Switch to a HALT mode and wait for a detection of a valid edge.

(4) When a valid edge is detected, the count value of the TCR00 register is captured to the timer data register (TDR00), at the same time, the TCR00 register is cleared to 0000H, and the capture end interrupt (INTTM00) is requested, and then a HALT mode is released. After a HALT mode is released, the capture end interrupt request flag is cleared. The first capture value of the TDR00 register is invalid and cannot be used.

(5) Set the numbers of measurement times of the high-level width and low-level width.

(6) Enable interrupt requests.

(7) Switch to a HALT mode and wait for a detection of a valid edge.

(8) When a valid edge is detected, a HALT mode is released, and in the capture end interrupt processing, the capture value of the TDR00 register is temporarily stored in the on-chip RAM.

(9) Read the data of the P0 register twice to determine the detected edge.

(10) If a valid edge is not detected during the capture end interrupt processing and the two data of the P0 register are same, the determination result (00H or 01H) of the P0 register is set to the edge determination flag. According to the value of the edge determination flag, either a high-level width or a low-level width is selected, and the capture value temporarily stored is stored in the variable in the on-chip RAM appropriately for the selected width type.

If a valid edge is detected during the capture end interrupt processing or the two data of the P0 register are not same, the capture value temporarily stored is not stored in the variable in the on-chip RAM, and the capture end interrupt request flag is cleared, and the number of the discarded edge is incremented.

(11) Repeat steps (7) to (10) until high-level widths and low-level widths are measured four times each.

(12) After the measurement of the setting number is finished, set the TT00 bit of the timer channel stop register 0 (TT0) to 1 to disable count operation, and switch to a HALT mode.

5.2 Option Byte Settings

Table 5.1 shows the option byte settings. Set the values that are most suited to your system as necessary.

Table 5.1 Option Byte Settings

Address	Setting Value	Contents
000C0H / 010C0H	11101111B	Disables the watchdog timer. (Counting stopped after reset)
000C1H / 010C1H	01111111B	LVD detection voltage: reset mode At rising edge TYP. 2.81 V (2.76 V to 2.87 V) At falling edge TYP. 2.75 V (2.70 V to 2.81 V)
000C2H / 010C2H	11101000B	HS mode, High-speed on-chip oscillator clock (f_{IH}): 32 MHz
000C3H / 010C3H	10000100B	Enables on-chip debugging

5.3 Constants

Table 5.2 shows the constants that are used in this sample program.

Table 5.2 Constants for the Sample Program

Constant	Setting	Contents
_0001_TAU_OVERFLOW_OCCURS	0x0001U	Detects an overflow

5.4 Variables

Table 5.3 lists the variables.

Table 5.3 Variables

Type	Variable Name	Description	Function Used
uint8_t	g_count	Number of times to measure pulse interval	main r_tau0_channel0_interrupt
uint8_t	g_times_high	Number of times to measure high-level width	main r_tau0_channel0_interrupt
uint8_t	g_times_low	Number of times to measure low-level width	main r_tau0_channel0_interrupt
uint8_t	e_edge_flag	Edge determination flag	r_tau0_channel0_interrupt
uint8_t	g_port_data[2]	Storage of input level of P00/TI00 pin	r_tau0_channel0_interrupt
uint32_t	g_width_high[4]	Storage of measurement value of high-level width	r_tau0_channel0_interrupt
uint32_t	g_width_low[4]	Storage of measurement value of low-level width	r_tau0_channel0_interrupt
volatile uint8_t	g_times_invalid	Number of times of discarded measurement value	r_tau0_channel0_interrupt
volatile uint32_t	g_tau0_ch0_width	Temporary storage of measurement value of pulse interval	r_tau0_channel0_interrupt

5.5 Functions

Table 5.4 lists the functions.

Table 5.4 Functions

Function name	Outline
main	Main processing
R_MAIN_UserInit	Main initial setting
R_TAU0_Channel0_Start	Timer Array Unit 0 channel 0 start processing
R_TAU0_Channel0_Stop	Timer Array Unit 0 channel 0 stop processing
r_tau0_channel0_interrupt	Timer Array Unit 0 channel 0 capture end interrupt processing

5.6 Function Specifications

This part describes function specifications of the sample code.

[Function Name] main

Outline	Main processing
Header	r_cg_macrodriver.h, r_cg_cgc.h, r_cg_port.h, r_cg_timer.h, r_cg_userdefine.h
Declaration	—
Description	After executing the main user initialization function, enables the timer array unit operation. Discards the result of the first pulse width measurement. Sets the numbers of measurement times and enables the maskable interrupts. Stops the timer array unit operation when the pulse width measurement is completed for the preset number of times.
Arguments	None
Remarks	None
Outline	None

[Function Name] R_MAIN_UserInit

Outline	Main initial setting
Header	r_cg_macrodriver.h, r_cg_cgc.h, r_cg_port.h, r_cg_timer.h, r_cg_userdefine.h
Declaration	void R_MAIN_UserInit(void)
Description	Maskable interrupts is disabled
Arguments	None
Remarks	None
Outline	None

[Function Name] R_TAU0_Channel0_Start

Outline	Timer array unit 0 channel 0 start processing
Header	r_cg_macrodriver.h, r_cg_timer.h, r_cg_userdefine.h
Declaration	void R_TAU0_Channel0_Start(void)
Description	Timer array unit channel 0 starts count operation.
Arguments	None
Remarks	None
Outline	None

[Function Name] R_TAU0_Channel0_Stop

Outline	Timer array unit 0 channel 0 stop processing
Header	r_cg_macrodriver.h, r_cg_timer.h, r_cg_userdefine.h
Declaration	void R_TAU0_Channel0_Stop(void)
Description	Timer array unit channel 0 stops count operation.
Arguments	None
Remarks	None
Outline	None

[Function Name] r_tau0_channel0_interrupt

Outline	Timer array unit 0 channel 0 capture end interrupt processing
Header	r_cg_macrodriver.h, r_cg_timer.h, r_cg_userdefine.h
Declaration	static void __near r_tau0_channel0_interrupt(void)
Description	Determines the type of the input pulse edge and stores the measured pulse interval in the variable accordingly.
Arguments	None
Remarks	None
Outline	None

5.7 Flowcharts

Figure 5.1 shows an overall flow of the sample code.

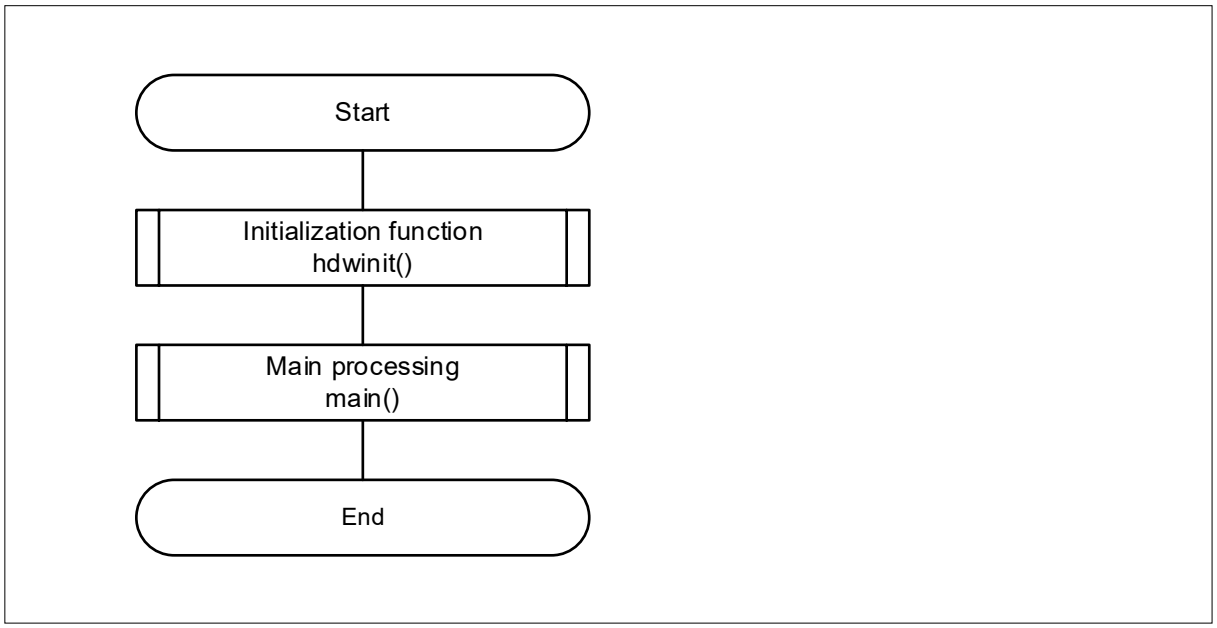

Figure 5.1 Overall Flow

5.7.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

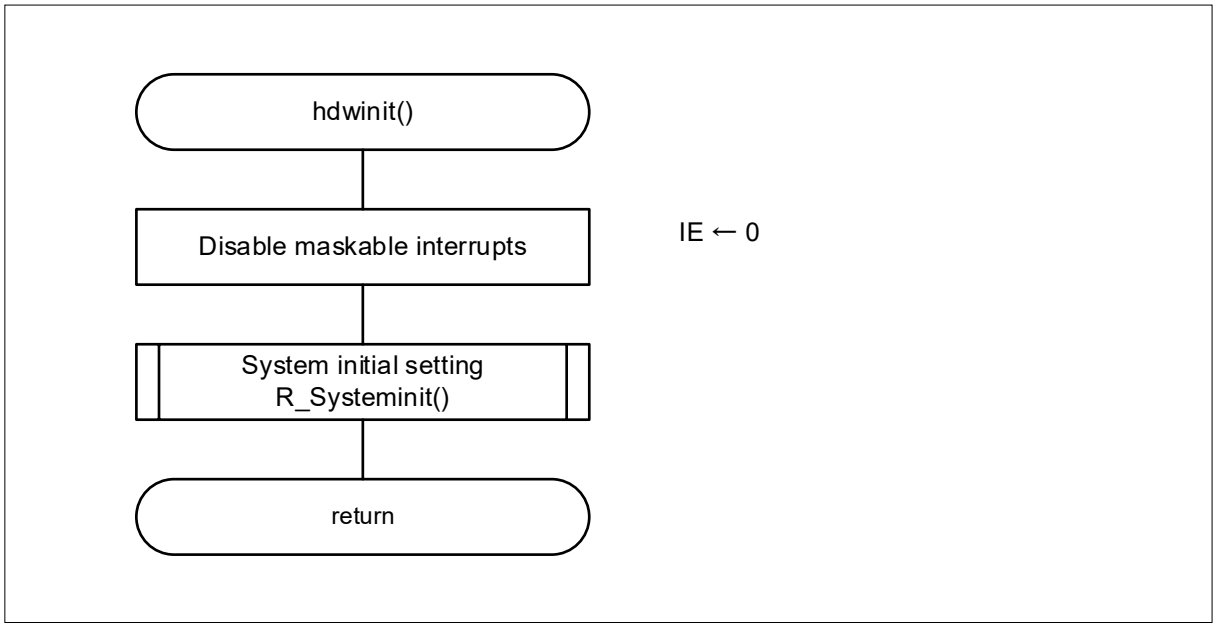

Figure 5.2 Initialization Function

5.7.2 System Initial Settings

Figure 5.3 shows the flowchart for the system initial setting.

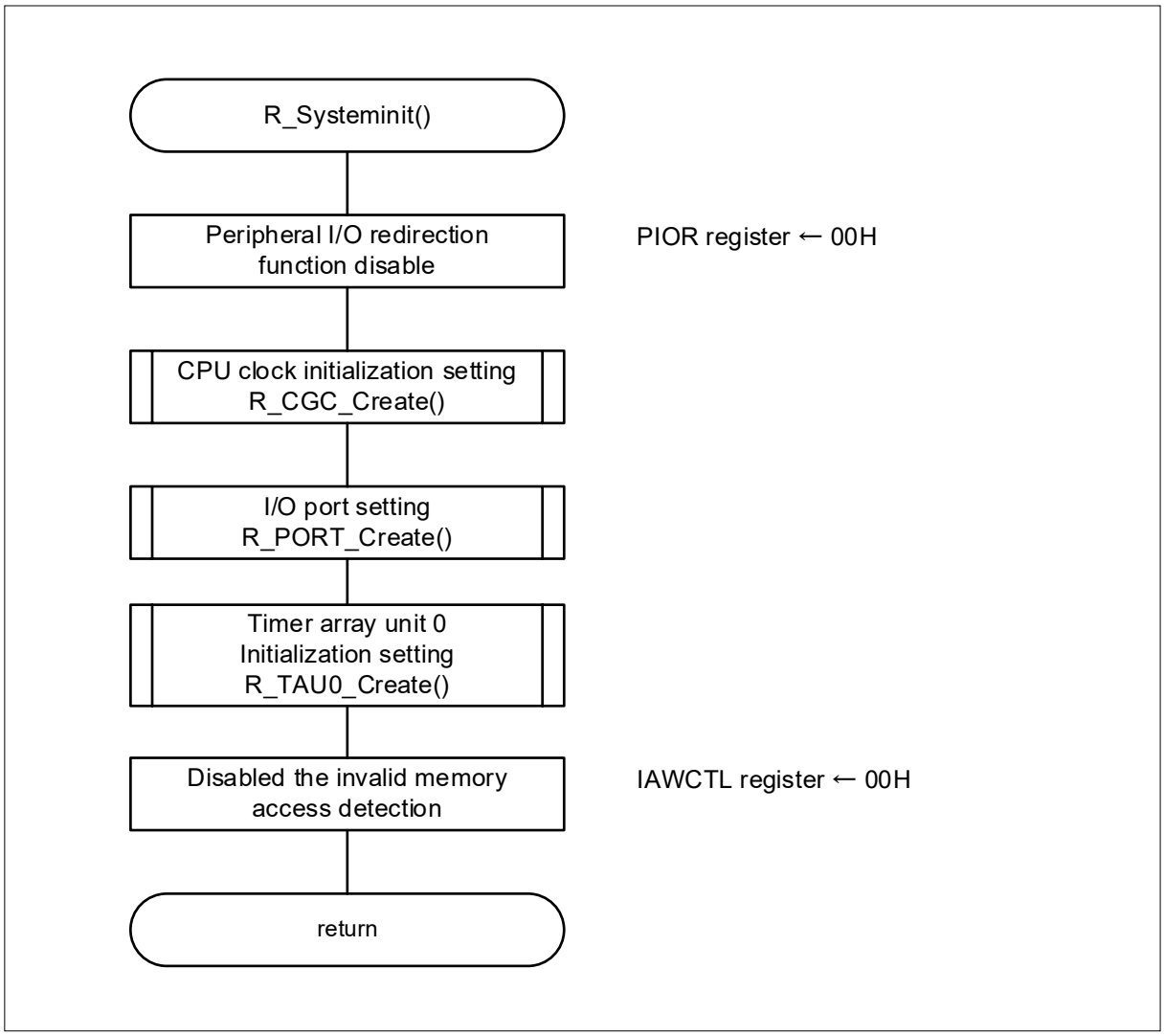

Figure 5.3 System Initial Setting

5.7.3 Ports Initial Setting

Figure 5.4 shows the flowchart for the ports initial setting.

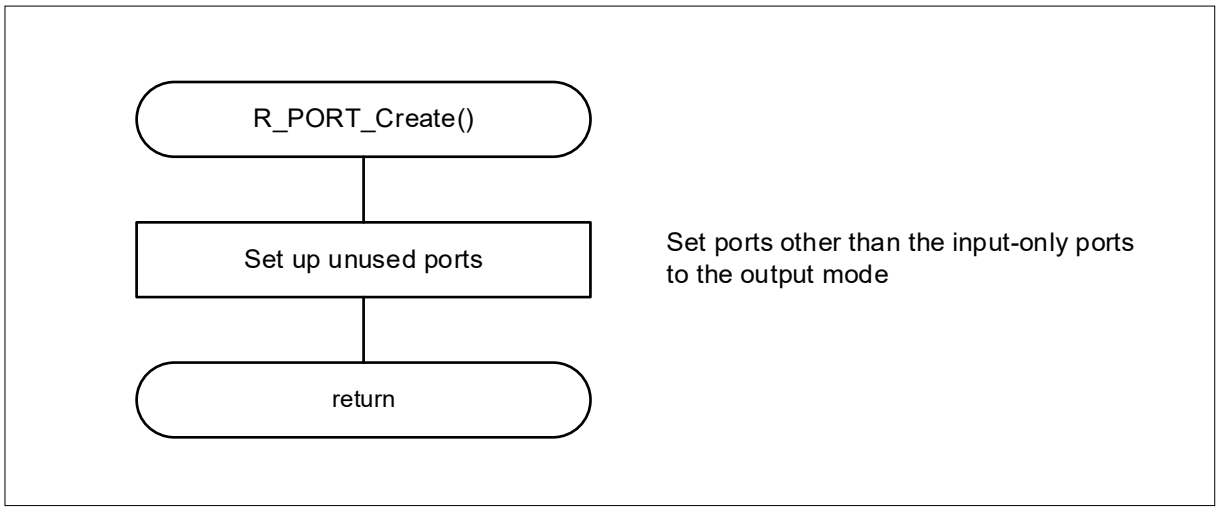

Figure 5.4 Port Initial Setting

Note: Refer to the initialization flowchart in the RL78/G13 Initialization CC-RL (R01AN2575E) Application Note for details on how to set unused ports.

Caution: When designing circuits, always make sure unused ports are properly processed and all electrical characteristics are met. Also make sure each unused input-only port is connected to V_{DD} or V_{SS} through a resister.

5.7.4 CPU Clock Initial Setting

Figure 5.5 shows the flowchart of the CPU Clock initial setting.

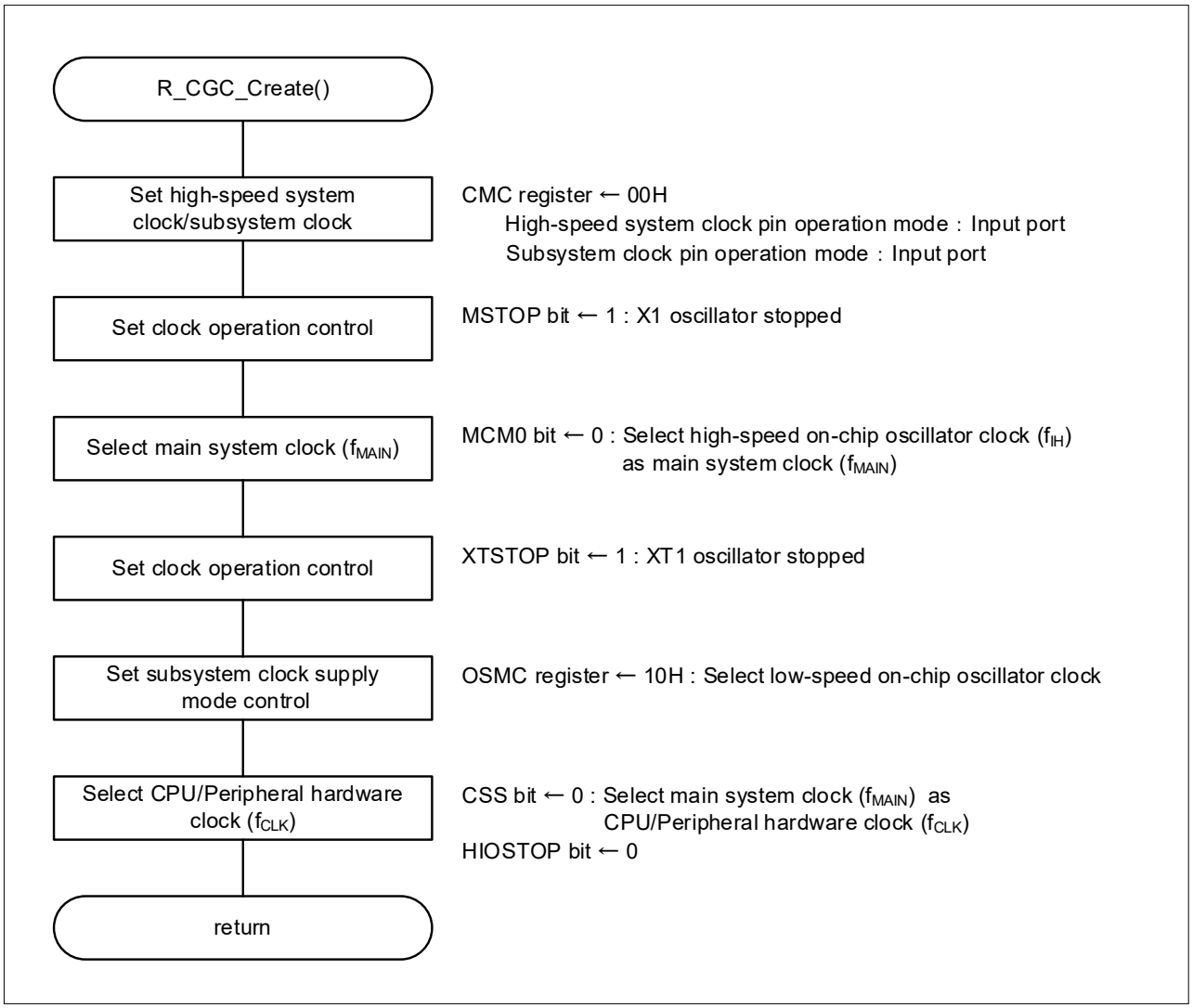

Figure 5.5 CPU Clock Initial Setting

Caution: For details on the procedure for setting up the CPU clock (R_CGC_Create()), refer to the section entitled “Flowcharts” in RL78/G13 Initialization Application Note (R01AN2575E).

5.7.5 Timer Array Unit 0 Initial Setting

Figure 5.6 and Figure 5.7 shows the flowchart for the timer array unit 0 initial setting.

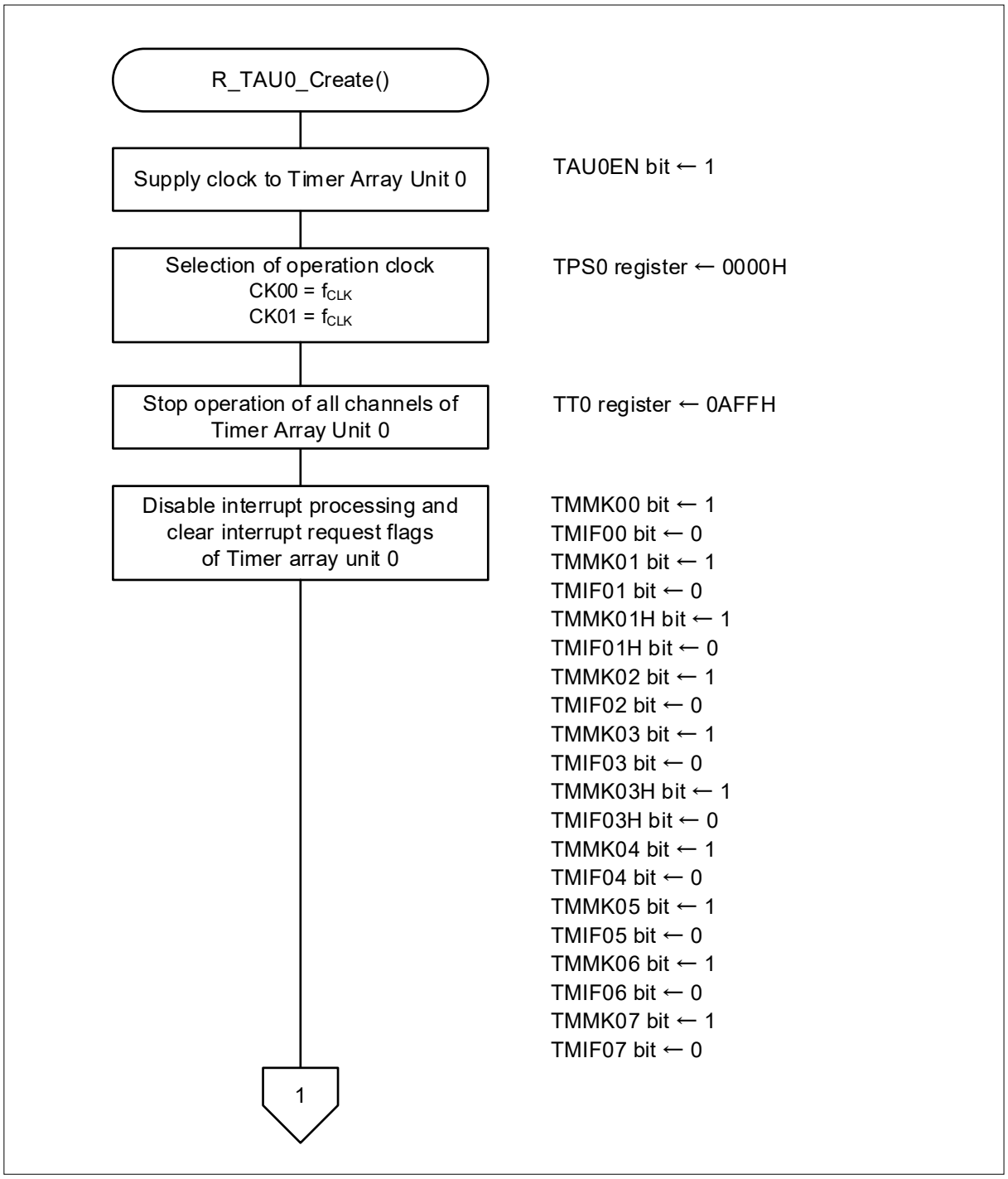

Figure 5.6 Timer Array Unit 0 Initial Setting (1/2)

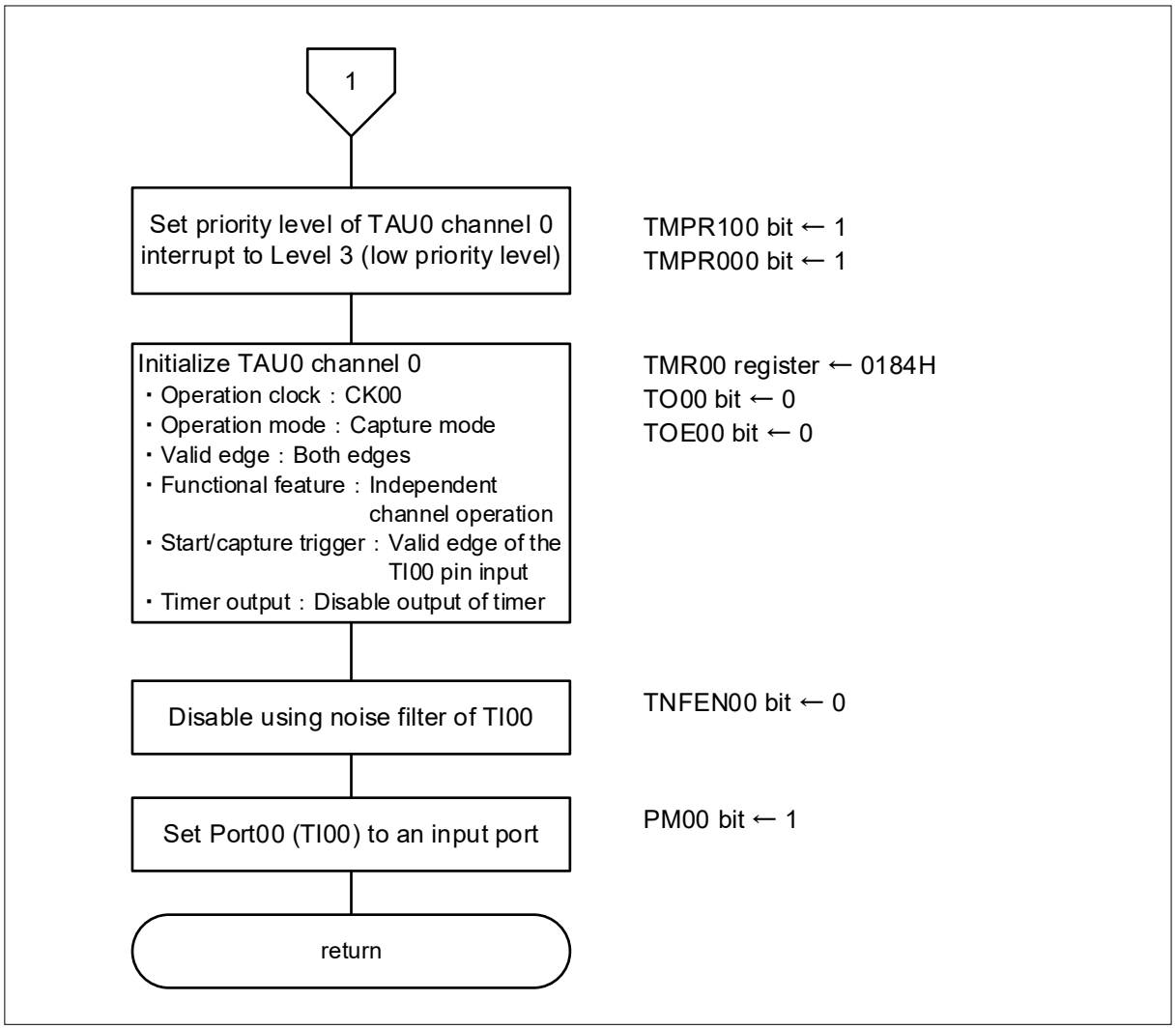

Figure 5.7 Timer Array Unit 0 Initial Setting (2/2)

Clock supply to timer array unit 0 started

- Peripheral enable register 0 (PER0)

Clock supply to timer array unit 0

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
0	0	0	0	0	0	0	**1**

Bit 0

TAU0EN	Control of timer array unit 0 input clock
0	Stops supply of input clock.
1	**Supplies input clock.**

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

Operation clock setting

- Timer clock select register 0 (TPS0)

Selection of operation clock (CK00)

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS 031	PRS 030	0	0	PRS 021	PRS 020	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
0	0	**0**	**0**	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

PRS 003	PRS 002	PRS 001	PRS 000		Operation Clock (CK00) Selection				
					f_{CLK} = 2MHz	f_{CLK} = 5MHz	f_{CLK} = 10MHz	f_{CLK} = 20MHz	f_{CLK} = 32MHz
0	**0**	**0**	**0**	**f_{CLK}**	**2MHz**	**5MHz**	**10MHz**	**20MHz**	**32MHz**
0	0	0	1	$f_{CLK}/2$	1MHz	2.5MHz	5MHz	10MHz	16MHz
0	0	1	0	$f_{CLK}/2^2$	500kHz	1.25MHz	2.5MHz	5MHz	8MHz
0	0	1	1	$f_{CLK}/2^3$	250kHz	625kHz	1.25MHz	2.5MHz	4MHz
0	1	0	0	$f_{CLK}/2^4$	125kHz	312.5kHz	625kHz	1.25MHz	2MHz
0	1	0	1	$f_{CLK}/2^5$	62.5kHz	156.2kHz	312.5KHz	625KHz	1MHz
0	1	1	0	$f_{CLK}/2^6$	31.25kHz	78.1kHz	156.2kHz	312.5kHz	500kHz
0	1	1	1	$f_{CLK}/2^7$	15.62kHz	39.1kHz	78.1kHz	156.2kHz	250kHz
1	0	0	0	$f_{CLK}/2^8$	7.81kHz	19.5kHz	39.1kHz	78.1kHz	125kHz
1	0	0	1	$f_{CLK}/2^9$	3.91kHz	9.76kHz	19.5kHz	39.1kHz	62.5kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95kHz	4.88kHz	9.76kHz	19.5kHz	31.25kHz
1	0	1	1	$f_{CLK}/2^{11}$	976Hz	2.44kHz	4.88kHz	9.76kHz	15.63kHz
1	1	0	0	$f_{CLK}/2^{12}$	488Hz	1.22kHz	2.44kHz	4.88kHz	7.81kHz
1	1	0	1	$f_{CLK}/2^{13}$	244Hz	610Hz	1.22kHz	2.44kHz	3.91kHz
1	1	1	0	$f_{CLK}/2^{14}$	122Hz	305Hz	610Hz	1.22kHz	1.95kHz
1	1	1	1	$f_{CLK}/2^{15}$	61Hz	153Hz	305Hz	610Hz	976Hz

Channel stop control

- Timer channel stop register 0 (TT0)

Stop the counting operation of each channel

Symbol: TT0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TT H03	0	TT H01	0	TT 07	TT 06	TT 05	TT 04	TT 03	TT 02	TT 01	TT 00
0	0	0	0	1	0	1	0	1	1	1	1	1	1	1	**1**

Bits 7-0

TT0n	Operation stop trigger (n=0-7)
0	TE00 bit is cleared to 0 and the count operation is stopped.
1	**Operation is stopped (stop trigger is generated).**

Bits 11, 9

TTH0n	Operation stop trigger (n=1,3 8-bit timer mode)
0	TE00 bit is cleared to 0 and the count operation is stopped.
1	**Operation is stopped (stop trigger is generated).**

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

Timer array unit 0 channel 0 initialization

- Timer mode register 00 (TMR00)

Selection of operation mode, Selection start trigger,
Selection of operation clock

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	**0**	0	**0**	0	**0**	**0**	**1**	**1**	**0**	0	0	**0**	**1**	**0**	**0**

Bits 15-14

CKS001	CKS000	Selection of operation clock (f_{MCK}) for channel 0
0	**0**	**Operation clock CKm0 set in timer clock selection register m (TPSm)**
0	1	Operation clock CKm2 set in timer clock selection register m (TPSm)
1	0	Operation clock CKm1 set in timer clock selection register m (TPSm)
1	1	Operation clock CKm3 set in timer clock selection register m (TPSm)

Bit 12

CCS00	Selection of channel 0 operation clock (f_{TCLK})
0	**Operation clock (f_{MCK}) set in bits CKS000 and CKS001**
1	Valid edge of input signal from TI00 pin

Bits 10-8

STS 002	STS 001	STS 000	Setting start or capture trigger of channel 0
0	0	0	Only software trigger start is valid (other trigger sources are unselected)
0	**0**	**1**	**Valid edge of TI00 pin input is used as both the start trigger and capture trigger**
0	1	0	Both edges of TI00 pin input are used as the start trigger and capture trigger
1	0	0	Interrupt signal of master channel is used (when using slave channel with simultaneous channel operation function)

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	**0**	0	**0**	0	**0**	**0**	**1**	**1**	**0**	0	0	**0**	**1**	**0**	**0**

Bits 7-6

CIS 001	CIS 000	Selection of TI00 pin input valid edge
0	0	Falling edge
0	1	Rising edge
1	**0**	**Both edges (when low-level width is measured)**
1	1	Both edges (when high-level width is measured)

Bits 3-0

MD 003	MD 002	MD 001	MD 000	Operation mode of channel 0
0	0	0	0	Interval timer mode (Timer interrupt is not generated when counting is started).
			1	Interval timer mode (Timer interrupt is generated when counting is started）.
0	**1**	**0**	**0**	**Capture mode** **(Timer interrupt is not generated when counting is started).**
			1	Capture mode (Timer interrupt is generated when counting is started).
0	1	1	0	Event counter mode (Timer interrupt is not generated when counting is started).
1	0	0	0	One-count mode (Start trigger is invalid during counting operation).
			1	One-count mode (Start trigger is valid during counting operation).
1	1	0	0	Capture & one-count mode (Timer interrupt is not generated when counting is started Start trigger is invalid during counting operation).

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers

5.7.6 Main Processing

Figure 5.8 shows the flowchart of the main processing.

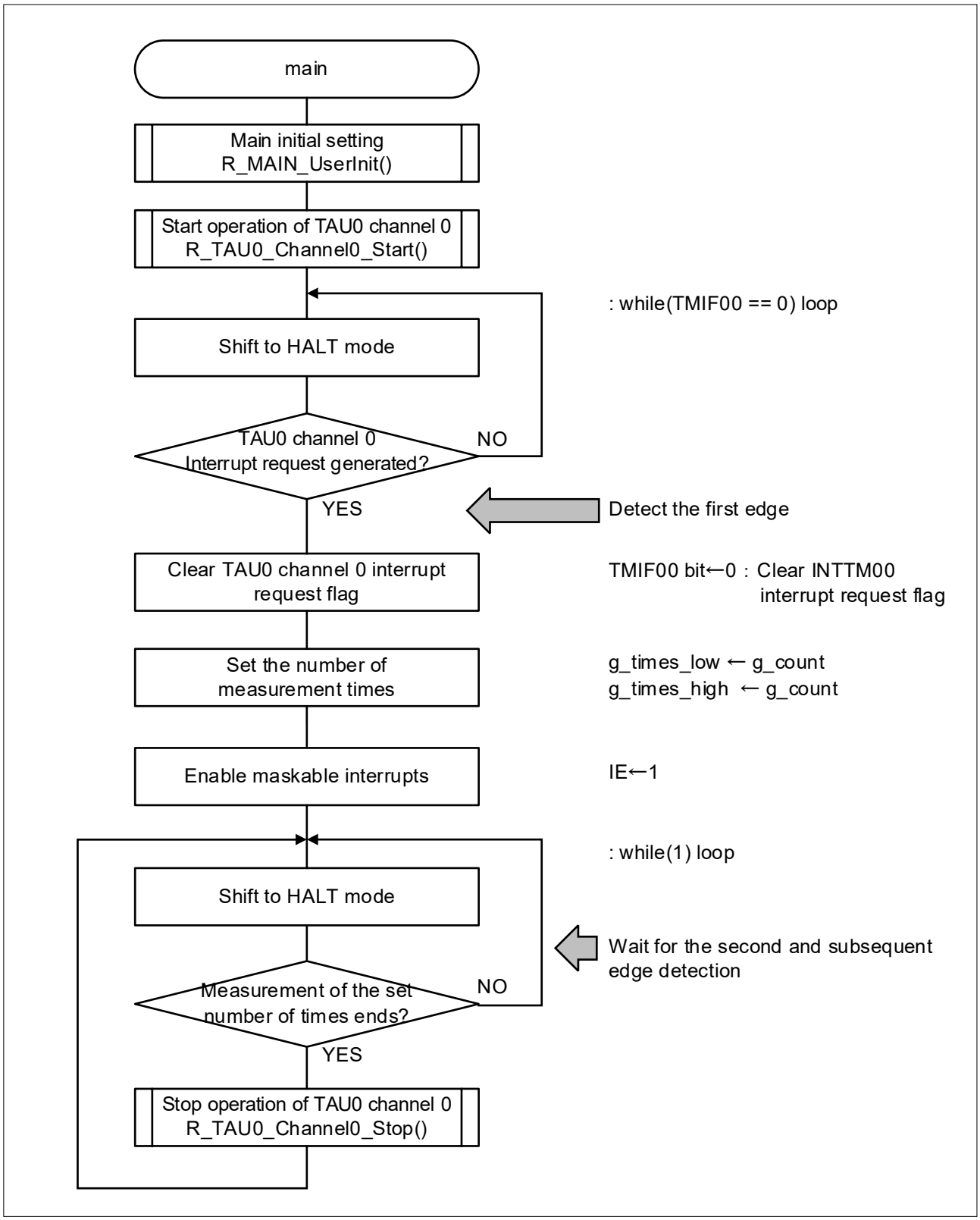

Figure 5.8 Main Processing

5.7.7 Main Initial Setting

Figure 5.9 shows the flowchart of the main initial setting.

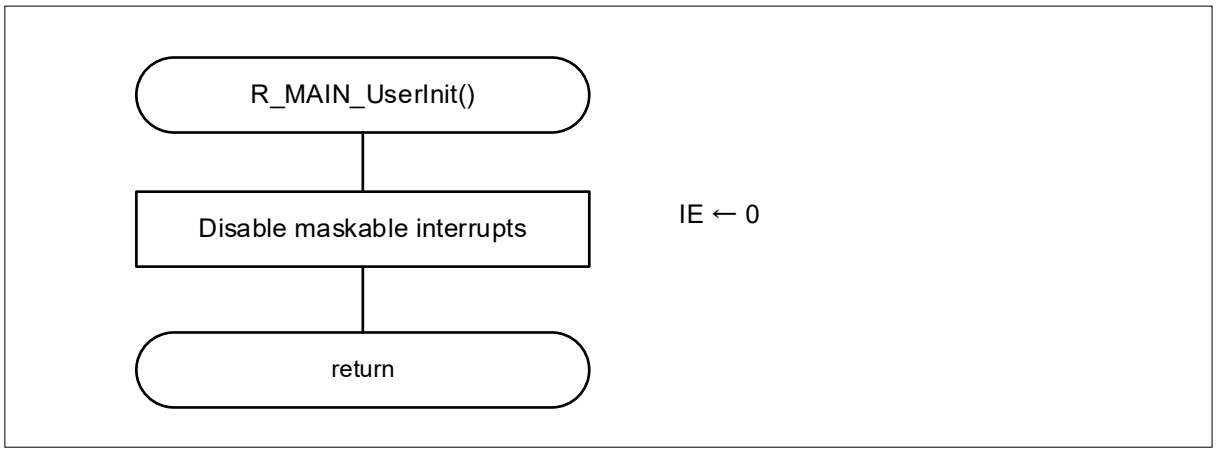

Figure 5.9 Main Initial Setting

5.7.8 Timer Array Unit 0 Channel 0 Start Processing

Figure 5.10 shows the flowchart of the timer array unit 0 channel 0 start processing.

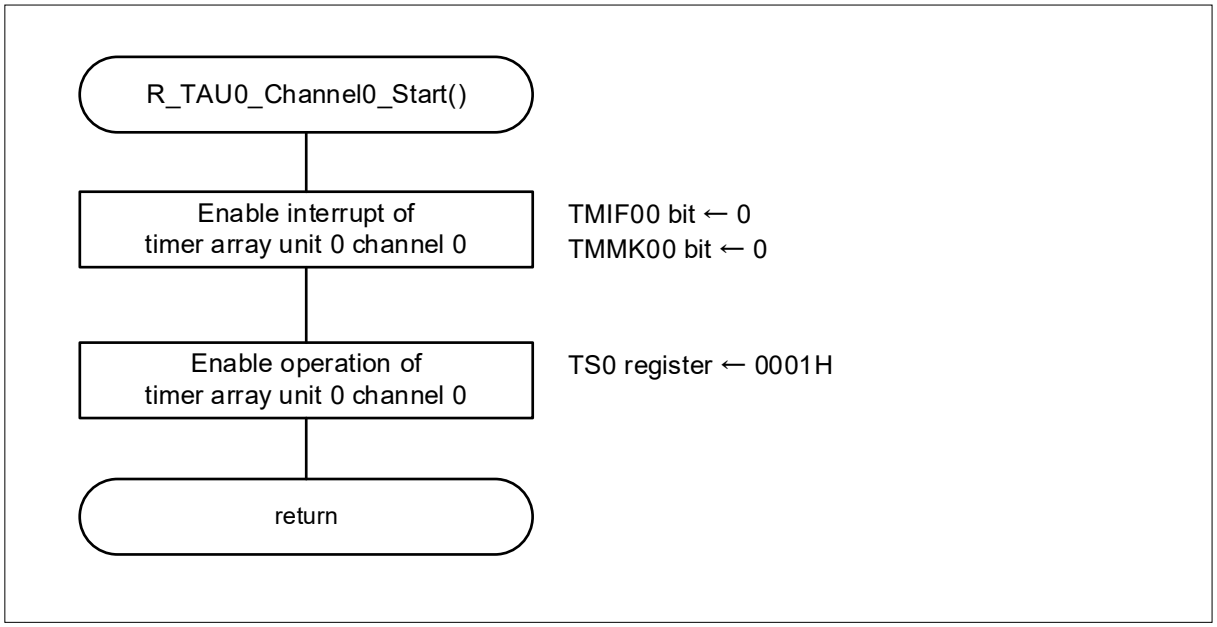

Figure 5.10 Timer Array Unit 0 Channel 0 Start Processing

Configuring the interrupt request flag

- Clear the timer interrupt request flag.

Symbol: IF1L

7	6	5	4	3	2	1	0
TMIF03	TMIF02	TMIF01	TMIF00	IICAIF0	SREIF1 TMIF03H	SRIF1 CSIIF11 IICIF11	STIF1 CSIIF10 IICIF10
0/1	0/1	0/1	**0**	0/1	0/1	0/1	0/1

Bit 4

TMIF00	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Configuring the interrupt mask

- Unmask timer interrupts.

Symbol: MK1L

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TMMK03	TMMK02	TMMK01	TMMK00	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
0/1	0/1	0/1	**0**	0/1	0/1	0/1	0/1

Bit 4

TMMK00	Interrupt processing control
0	**Enables interrupt processing.**
1	Disables interrupt processing.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Configuring the timer channel startup

- Enable timer count operation

略号： TS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TS H03	0	TS H01	0	TS 07	TS 06	TS 05	TS 04	TS 03	TS 02	TS 01	TS 00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**

Bit 0

TS00	Operation enable (start) trigger of channel 0
0	No trigger operation
1	**The TE00 bit is set to 1 and the count operation becomes enabled.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.9 Timer Array Unit 0 Channel 0 Stop Processing

Figure 5.11 shows the flowchart of the timer array unit 0 channel 0 stop processing.

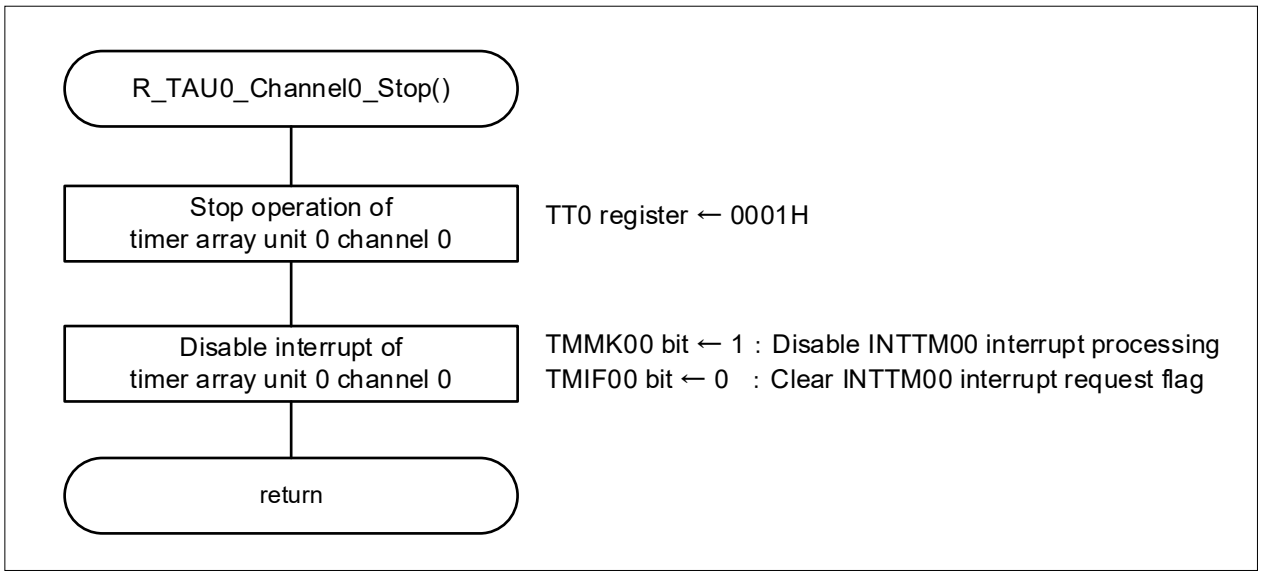

Figure 5.11 Timer Array Unit 0 Channel 0 Stop Processing

Configuring the timer channel stop

— Stop timer count operation.

Symbol: TT0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TT H03	0	TT H01	0	TT 07	TT 06	TT 05	TT 04	TT 03	TT 02	TT 01	TT 00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**

Bit 0

TT00	Operation stop trigger of channel 0
0	No trigger operation
1	**The TE00 bit is cleared to 0 and the count operation stopped.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.10 Timer Array Unit 0 Channel 0 Capture End Interrupt Processing

Figure 5.12 and Figure 5.13 show the flowchart of the timer array unit 0 channel 0 capture end interrupt processing.

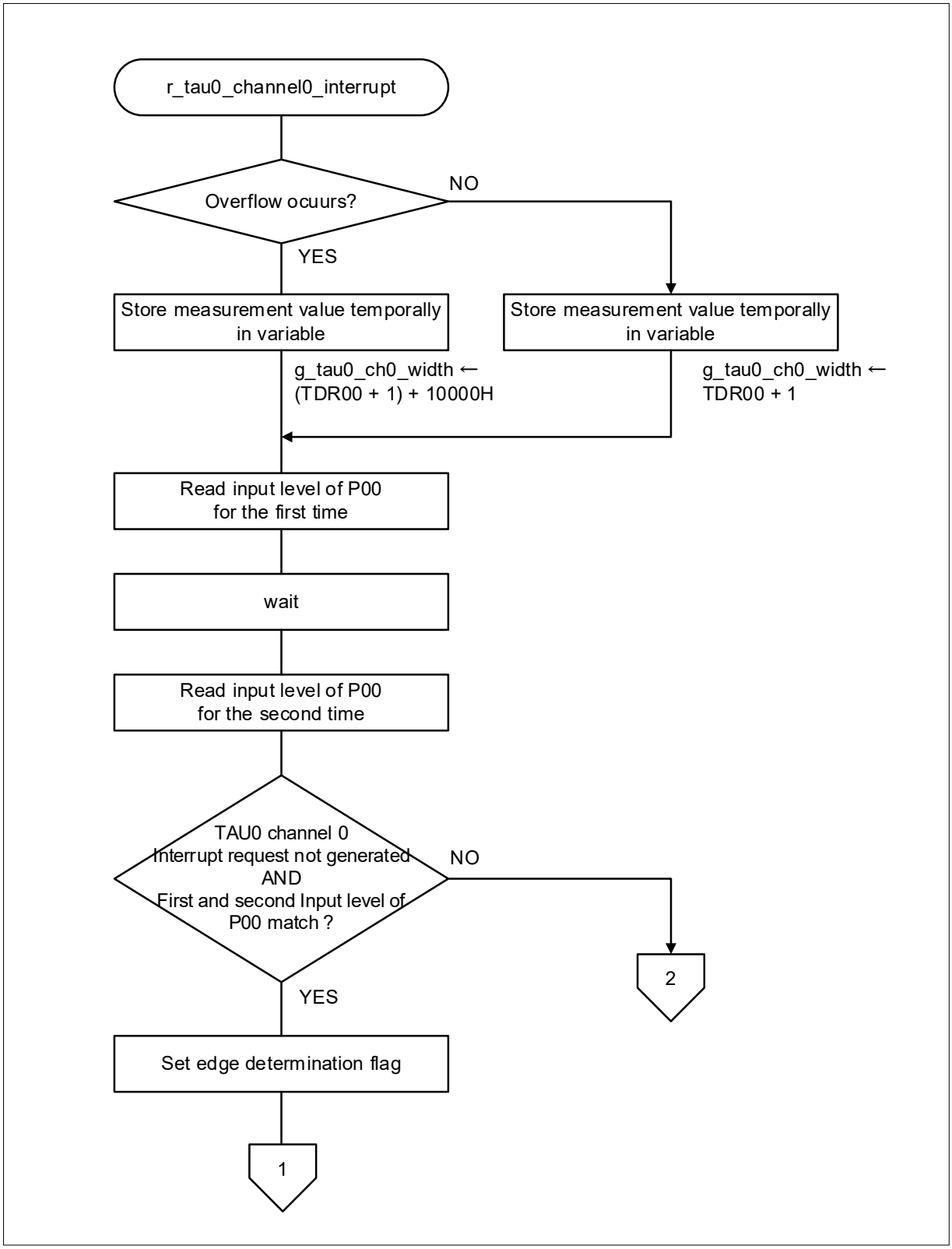

Figure 5.12 Timer Array Unit 0 Channel 0 Capture End Interrupt Processing (1/2)

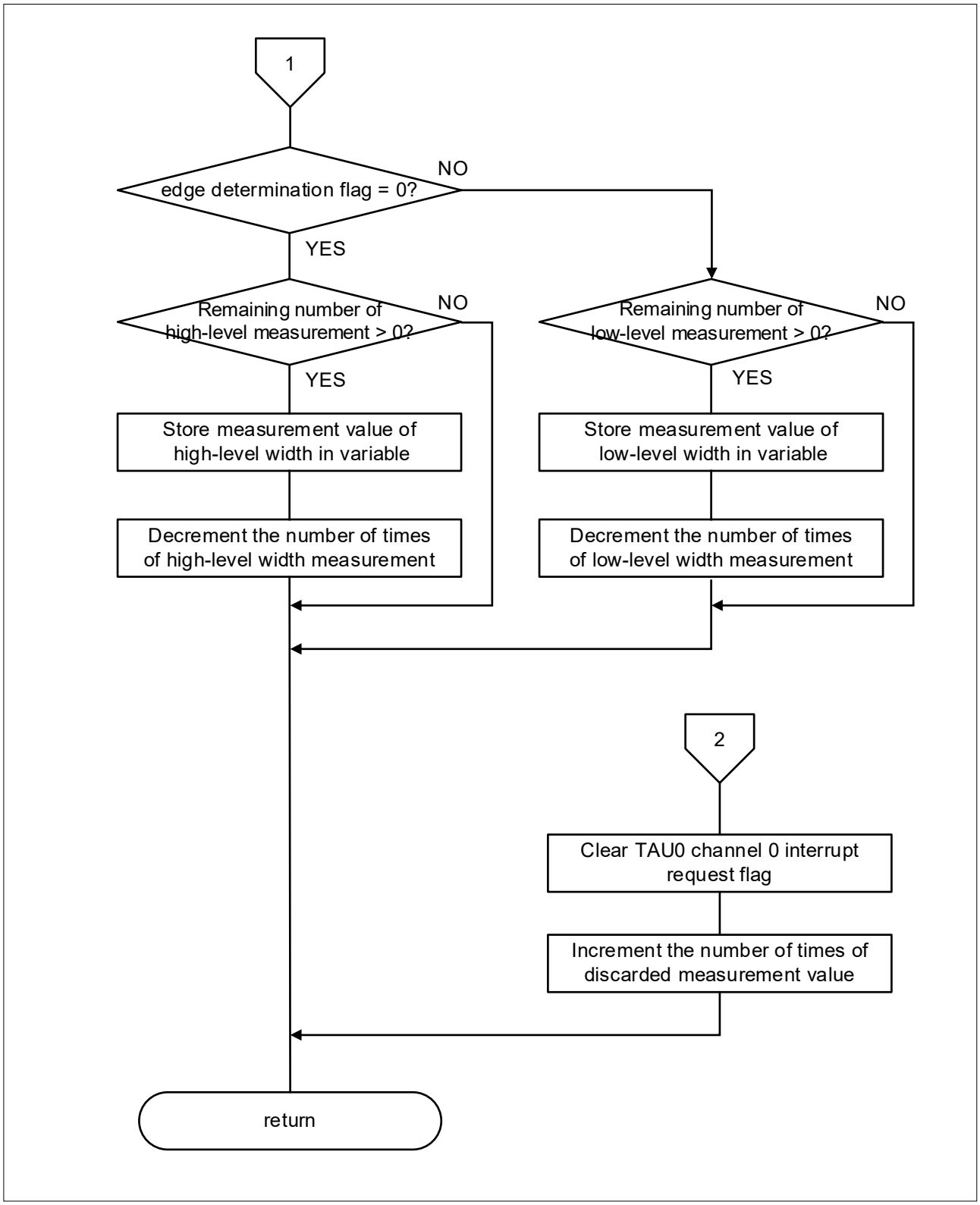

Figure 5.13 Timer Array Unit 0 Channel 0 Capture End Interrupt Processing (2/2)

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

RL78/G13 User's Manual: Hardware (R01UH0146J)
RL78 family user's manual software (R01US0015J)
The latest versions can be downloaded from the Renesas Electronics website.

Technical update
The latest versions can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jul.6,2018	-	First Edition
2.00	Aug 16, 2021	Throughout	Change from Timer Array Unit to Timer Array Unit 0
		3	Change of 1. Specifications
		4	Change of 2. Operation Confirmation Conditions
		5	Change of Notes in 4.1 Hardware Configuration Example
		5	Change of Function in Table 4.1 List of Pins and Functions
		6	Change of 5.1 Operation Outline
		7	Change of 5.2 Option Byte Settings
		7	Change of Table 5.3 Variables
		8	Change of Outline of r_tau0_channel0_interrupt in Table 5.4 Functions
		8	Change of Description of main
		8	Change of Description of R_MAIN_UserInit
		9	Change of Outline of r_tau0_channel0_interrupt
		9	Change of Declaration of r_tau0_channel0_interrupt
		11	Change of Figure 5.3 System Initial Setting
		12	Change of Figure 5.4 Port Initial Setting
		13	Change of the title of 5.7.4
		14,15	Change of Figure 5.6 Timer Array Unit 0 Initial Setting (1/2) and Figure 5.7 Timer Array Unit 0 Initial Setting (2/2)
		17	Change of the table of Controlling the channel trigger operation
		20	Change of Figure 5.8 Main Processing
		21	Change of Figure 5.9 Main Initial Setting
		22	Change of tables of Configuring the interrupt mask
		24	Change of Figure 5.11 Timer Array Unit 0 Channel 0 Stop Processing
		24	Add explanation of Configuring the timer channel stop
		25	Change of the title of 5.7.10
		25, 26	Change of Figure 5.12 Timer Array Unit 0 Channel 0 Capture End Interrupt Processing (1/2) and Figure 5.13 Timer Array Unit 0 Channel 0 Capture End Interrupt Processing (2/2)

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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