RL78/G14

AD Converter which Uses Timer RJ as Activation Source (SNOOZE mode) CC-RL

Introduction

This application note explains how to use the A/D converter (SNOOZE mode) which made the Timer RJ using a 16-bit counter the activation source. The A/D conversion can be performed, without activating CPU by use in SNOOZE mode. The changed value is stored in on-chip RAM, and keeps 10 times of the latest A/D conversion values.

Target Device

RL78/G14

When using this application note with other Renesas's MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

This application note provides an example of using an A/D converter (SNOOZE mode) which made the Timer RJ of a 16-bit counter the activation source.

The Timer RJ uses F_{IL} (low-speed OCO: TYP. 15 kHz) for count source, and generates an interrupt request every 4 seconds. Moreover, the interrupt request of the Timer RJ becomes a hardware trigger of an A/D converter via an event link controller (ELC).

When executes STOP command after setting “Use the SNOOZE mode function (ACW=1)”, it enters in an A/D conversion suspended state in STOP mode. If a hardware trigger is detected by an A/D conversion standby status, shifts to SNOOZE mode and starts the A/D conversion. If an A/D conversion is completed in the state of SNOOZE mode, returns to the normal mode from SNOOZE mode. Then converts the A/D conversion result (shifts data to 6-bit right), and stores a conversion value in on-chip RAM.
Table 1.1 shows peripheral functions and their applications, and Figure 1.1 shows the A/D converter operation outline (SNOOZE mode). In addition, the number at the bottom of Fig. 1.1 shows the processing number in “5.1 Operation Outline”.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
A/D converter	Converts analog signal input level of P20/ANI0 pin.

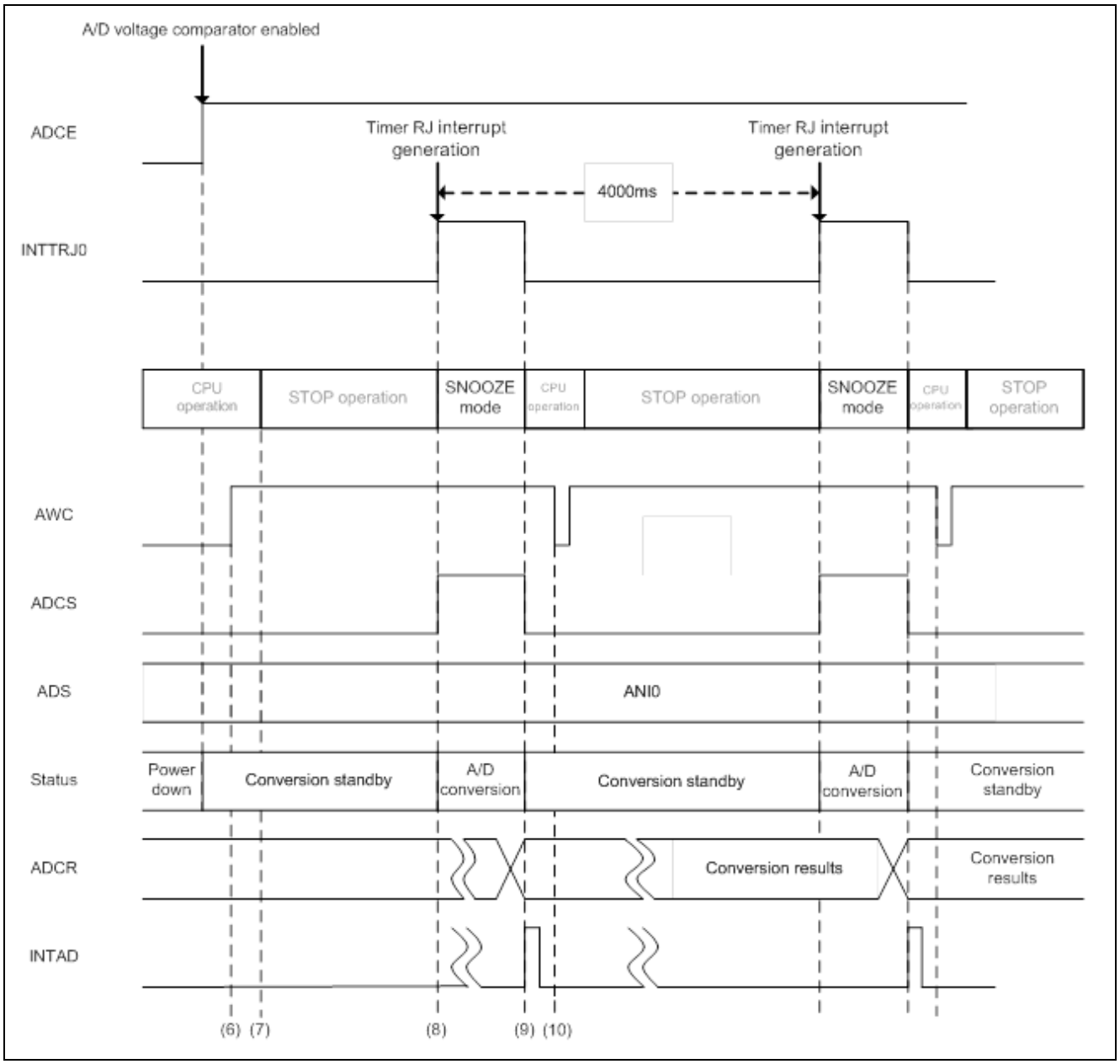

Figure 1.1 A/D Converter SNOOZE Operation Outline

Remark: Refer to “5.1 Operation Outline” for (6) to (10) in the figure 1.1.

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	RL78/G14 (R5F104PJA)
Operating frequency	• High-speed on-chip oscillator clock: 24 MHz • CPU/peripheral hardware clock: 24 MHz
Operating voltage	5.0 V (can run at a voltage range of 2.9 V to 5.5 V.) LVD operation(V_{LVD}): Reset mode which uses 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ V3.01.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V4.0.0.26 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V4.21.3 from IAR Systems
C compiler (IAR)	IAR C/C++ Compiler for Renesas RL78 V4.21.3.2447 from IAR Systems

3. Reference Application Note

For additional information associated with this document, refer to the following application note.

- RL78/G13 Initialization (R01AN2575E) Application note
- RL78/G13 A/D Converter (R01AN2581E) Application note
- RL78/G14 Pulse Output Forced Cutoff Using the Clock Alarm Function and ELC (R01AN2782E) Application note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 5.1 shows an example of hardware configuration that is used for this application note.

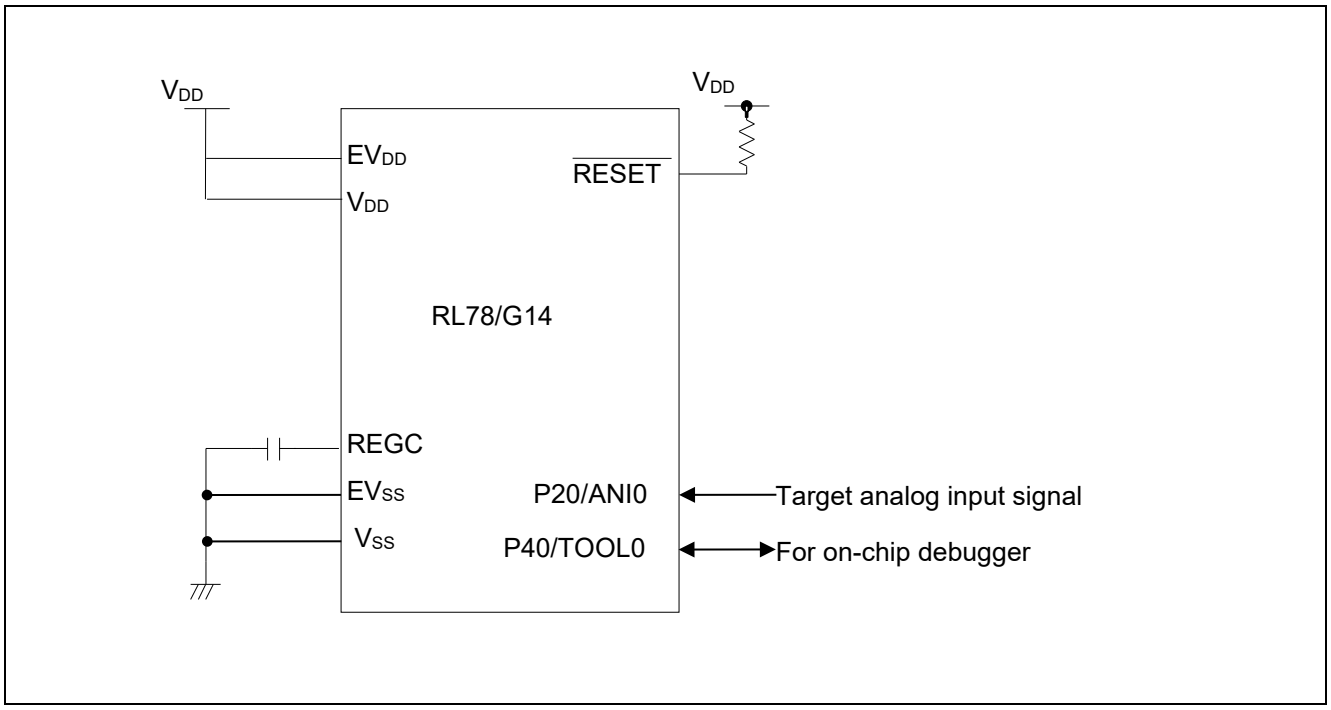

Figure 4.1 Hardware Configuration

Notes: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly.
When designing and implementing an actual circuit, provide proper pin treatment and make sure that the
hardware's electrical specifications are met (connect the input-dedicated ports separately to V_{DD} or V_{SS} via a resistor).
2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

4.2 List of Pins to be Used

Table 4.1 lists the Pins to be Used and Their Functions.

Table 4.1 Pins to be Used and Their Functions

Pin Name	I/O	Function
P20/ANI0	Input	A/D converter analog input port

5. Description of the Software

5.1 Operation Outline

This sample code performs A/D conversion on the analog voltage that is input to pin ANI0 by the hardware trigger input in the STOP mode and using the SNOOZE mode of the A/D converter. After A/D conversion is completed, the sample code shifts the result of A/D conversion 6 bits to the right and places the result in the internal RAM.

In addition, the timing by which the following processing is performed is specified in Fig. 1.1 lower part.

(1) **Initializes the A/D converter.**

<Setup conditions>

- Pin P20/ANI0 is used for the analog input.
- A/D conversion channel selection mode is set to select mode.
- A/D conversion operation mode is set to “one-shot conversion mode”.
- A/D conversion trigger mode is set to “hardware trigger wait mode”.
- Hardware trigger signal is set to “event signal selected by ELC”.
- The A/D conversion end interrupt (INTAD) is used.

(2) **Initializes Timer RJ (used as hardware trigger of A/D converter).**

<Setup conditions>

- Operation mode is set to “timer mode”.
- f_{IL} = 15 kHz(TYP.) is used as the count source.
- Timer RJ counter register 0 is set to ”EA5FH” (59999).

(3) **Initializes ELC.**

<Setup conditions>

- The event generation source of ELC is set to “Timer RJ0 underflow”.
- ELC link destination peripheral function is set to “A/D converter”.

  When an ELC program is automatically generated using Applilet3, a build error occurs when declaring variables in the R_ELC_Stop function. Please add __no_bit_access to the variable declaration to prevent build errors.

```
void R_ELC_Stop(uint32_t  event)
{
        Volatile uint32_t w_count;
        Volatile uint8_t __no_bit_access * sfr_addr;
        sfr_addr = &ELSELR00;
```

Addition

(4) **"1" (A/D conversion operation enabled) is set to the ADCE bit of ADM0 register after the end of initialization.**

(5) **Sets "1" (counter start) to TSTART bit of TRJCR0 register, and sets "1" (interruption processing disabled) to TRJMK0 bit of MK1H register.**

(6) **Makes the mode SNOOZE mode by setting “1” to AWC bit of ADM2 register.**

(7) **Moves to the STOP mode, and waits the hardware trigger.**

(8) **An input of a hardware trigger will start an A/D conversion.**

(9) **After completing the A/D conversion of the voltage input from pin ANI0, the A/D converter transfers the result of A/D conversion to the ADCR register and generates an A/D conversion end interrupt.**

(10) **Since an A/D converter will shift to normal operation mode from SNOOZE mode if an A/D conversion end interrupt occurs, "0" is set to the AWC bit of ADM2 register according to it. Then, reads an A/D conversion result from an ADCR register, shifts to 6-bit right, and stores in on-chip RAM.**

(11) **The sample code returns to step (6) to enter the SNOOZE mode again.**

Note: For the precautions in the use of the device, refer to RL78/G14 User's Manual: Hardware.

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release of the reset state.)
000C1H/010C1H	01111111B	LVD reset mode 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11100000B	HS mode, HOCO clock: 24 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger. Erases data of flash memory in case of failures in authenticating on-chip debug security ID.

5.3 List of Constants

Table 5.2 lists the Constant Used in the Sample Code.

Table 5.2 Constant Used in the Sample Code

Constant	Value	Description
MAX_BUFFER	0AH	Number of buffers to retain A/D conversion results

5.4 List of Variables

Table 5.3 lists the Global Variables.

Table 5.3 Global Variables

Type	Variable Name	Description	Function Used
uint8_t	g_buffer_count	The buffer number to be used	main()
uint16_t	g_result_buffer [MAX_BUFFER]	Area for storing the A/D conversion results	main()

5.5 List of Functions

Table 5.4 lists the functions.

Table 5.4 Functions

Function Name	Outline
R_ADC_Set_OperationOn	Enables the A/D voltage comparator.
R_ADC_Start	Starts waiting for an A/D conversion trigger.
R_ADC_Get_Result	Gets A/D conversion results.
R_ADC_Set_SnoozeOn	Starts Snooze function of A/D conversion.
R_ADC_Set_SnoozeOff	Stops Snooze function of A/D conversion.
R_TMR_RJ0_Start	Starts Timer RJ operation.

5.6 Function Specifications

This section describes the specifications for the functions that are used in the sample code.

[Function Name] R_ADC_Set_OperationOn

Outline	Enable A/D voltage comparator.
Header	r_cg_adc.h
Declaration	void R_ADC_Set_OperationOn(void)
Description	Sets A/D converter operation enabled (ADCE = 1).
Argument	None
Return Value	None
Remarks	None

[Function Name] R_ADC_Start

Outline	Starts waiting for an A/D conversion trigger.
Header	r_cg_adc.h
Declaration	void R_ADC_Start (void)
Description	Clears A/D conversion end interrupt flag (ADIF＝0), and disables A/D conversion end interrupt (ADMK＝0).
Argument	None
Return Value	None
Remarks	None

[Function Name] R_ADC_Get_Result

Outline	Gets A/D conversion results.	
Header	r_cg_adc.h	
Declaration	void R_ADC_Get_Result(uint16_t * const buffer)	
Description	Shifts the A/D conversion results 6 bits to the right and stores the results in the area designated by the argument.	
Argument	buffer	Address of the area for storing the A/D conversion results.
Return Value	None	
Remarks	None	

[Function Name] R_ADC_Set_SnoozeOn

Outline	Starts Snooze function of A/D conversion.
Header	r_cg_adc.h
Declaration	void R_ADC_Set_SnoozeOn(void)
Description	Sets SNOOZE mode function of A/D conversion to use (AWC＝1).
Argument	None
Return Value	None
Remarks	None

[Function Name] R_ADC_Set_SnoozeOff

Outline	Stops Snooze function of A/D conversion.
Header	r_cg_adc.h
Declaration	void R_ADC_Set_SnoozeOff(void)
Description	Sets SNOOZE mode function of A/D conversion to stop (AWC＝0).
Argument	None
Return Value	None
Remarks	None

[Function Name] R_TMR_RJ0_Start

Outline	Starts Timer RJ operation.
Header	r_cg_timer.h
Declaration	void R_TMR_RJ0_Start (void)
Description	Sets Timer RJ operation start (TSTART＝1).
Argument	None
Return Value	None
Remarks	None

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

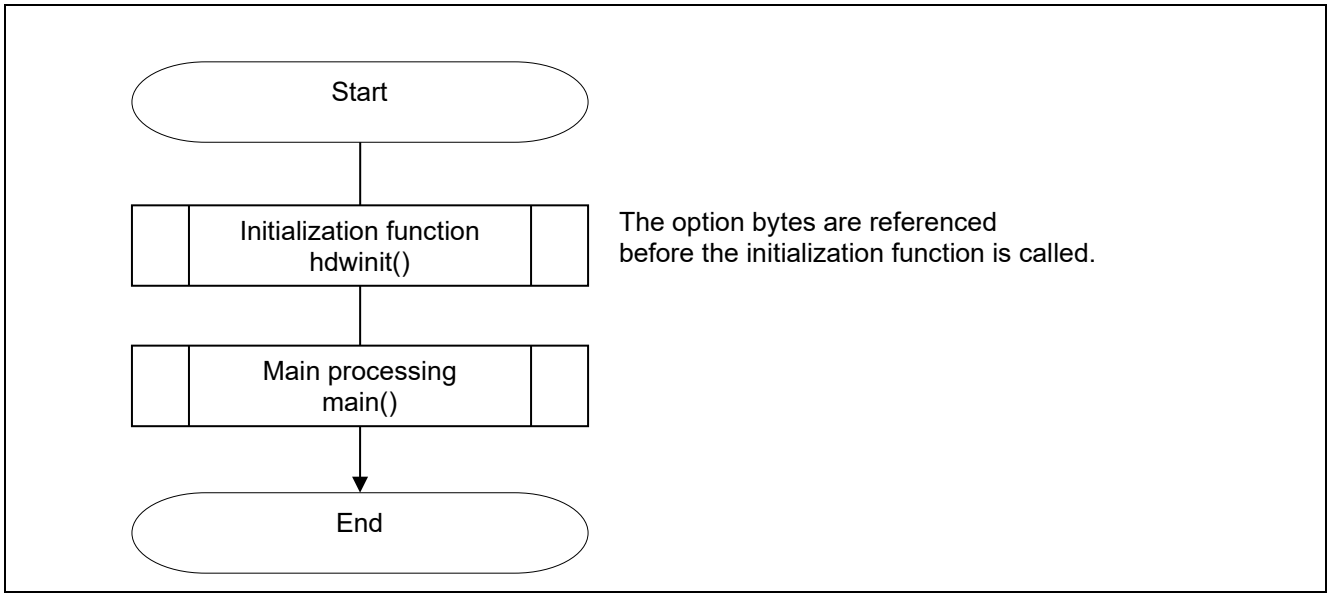

Figure 5.1 Overall Flow

5.7.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

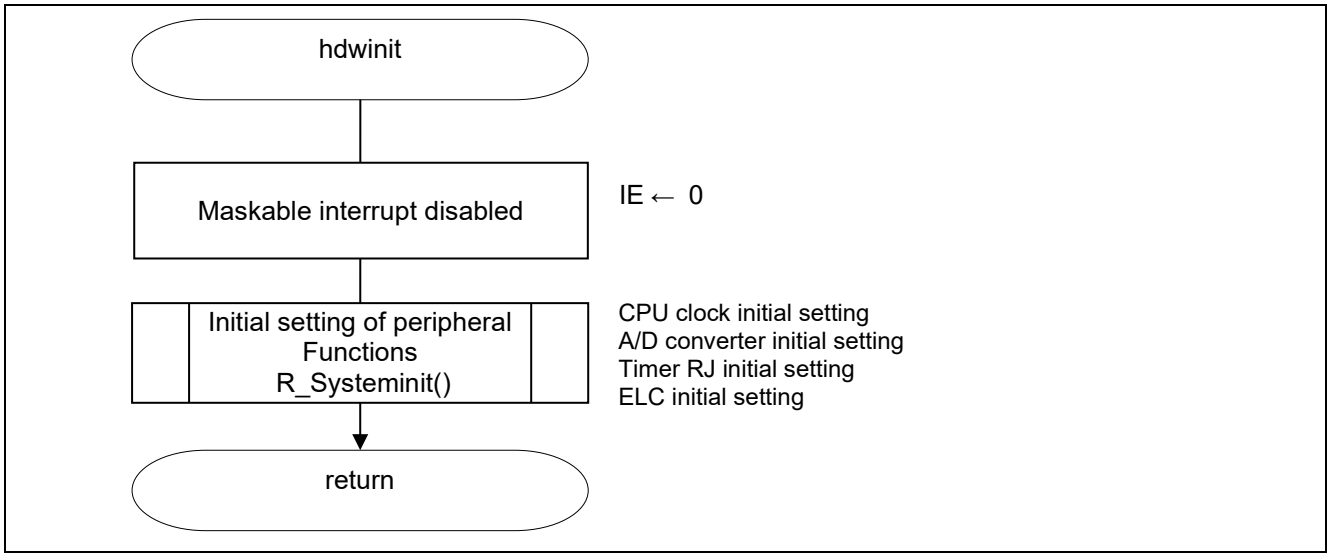

Figure 5.2 Initialization Function

5.7.2 Initialization System Function

Figure 5.3 shows the flowchart for the system initialization function.

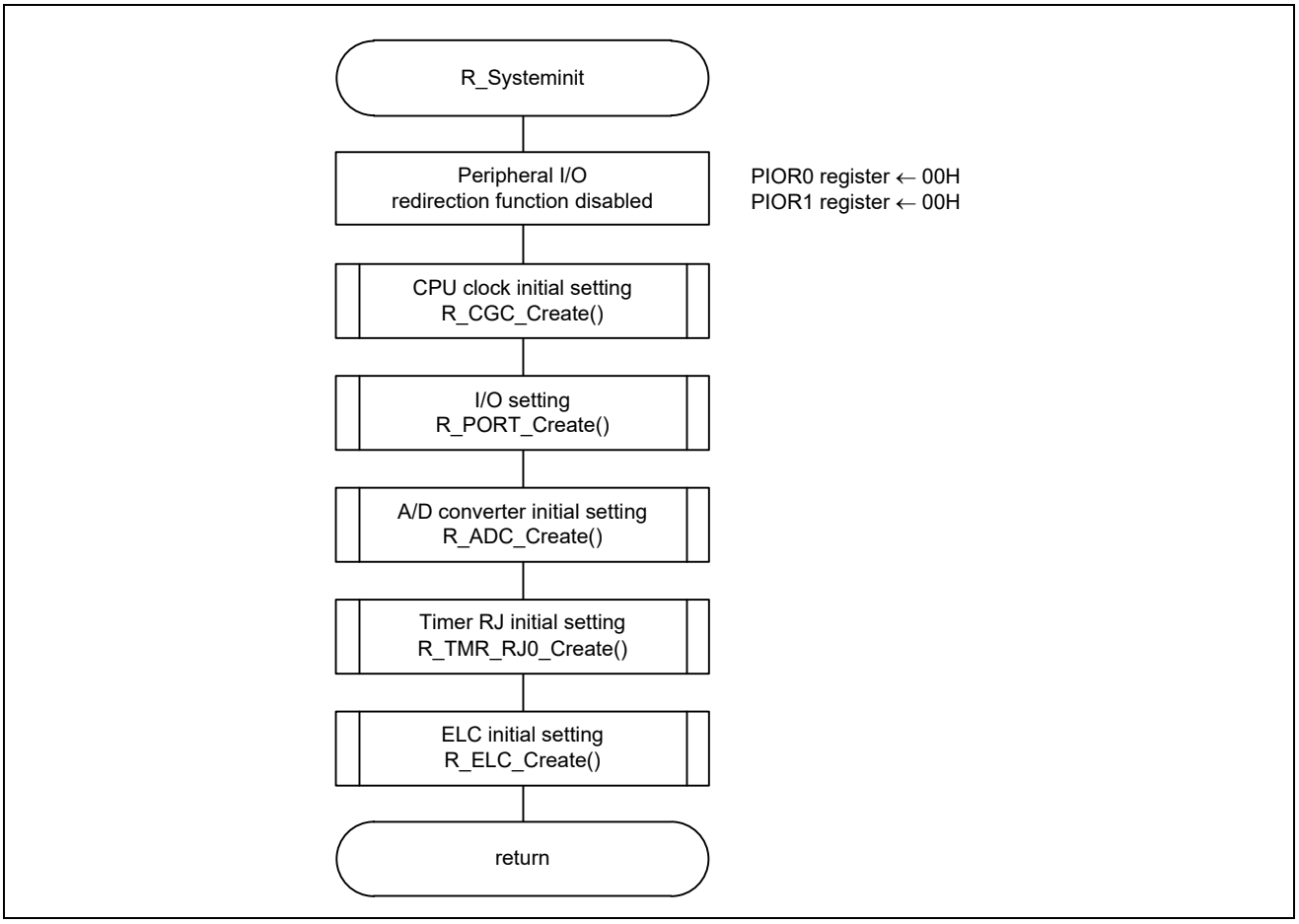

Figure 5.3 Initialization System Function

5.7.3 I/O Port Setup

Figure 5.3 shows the flowchart for I/O port setup.

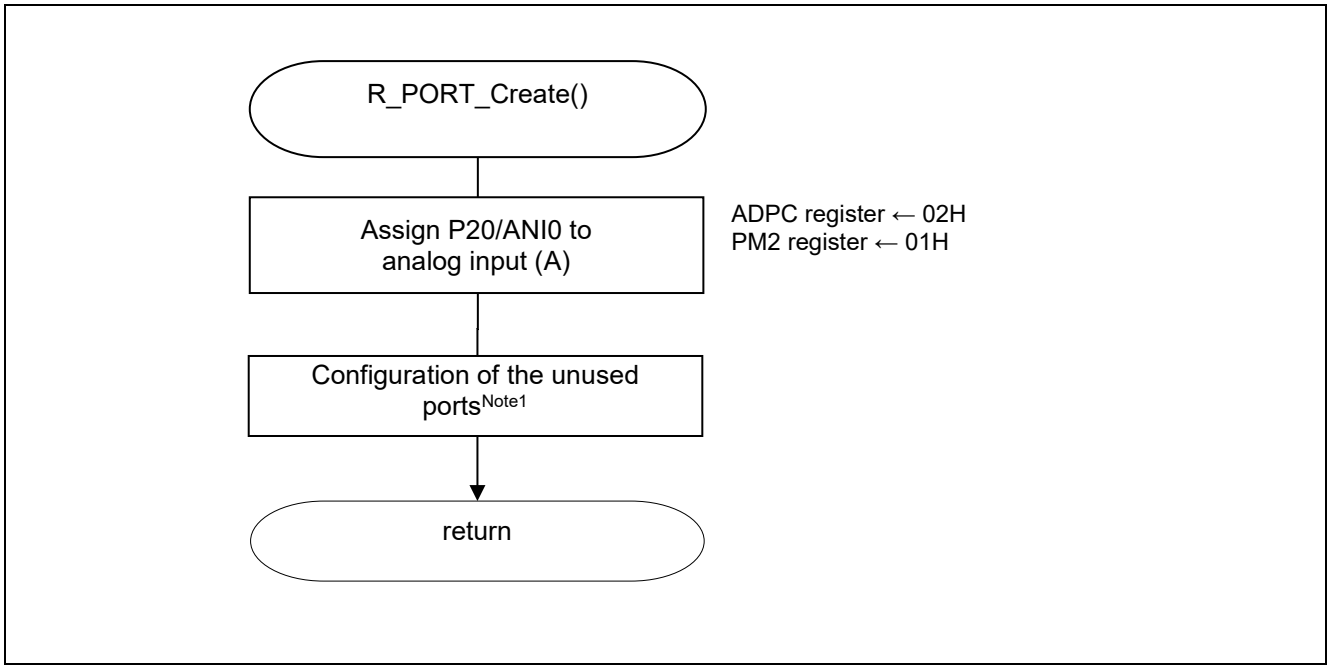

Figure 5.4 I/O Port Setup

Note 1: Refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E) for the configuration of the unused ports.

Note: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of
any unused input-only ports to V_{DD} or V_{SS} via separate resistors.

Setting up the channel to be used for A/D conversion

- A/D port configuration register (ADPC)
  Switches between A/D converter analog input and port digital I/O.
- Port mode register 2 (PM2)
  Selects I/O mode of PM2.

Symbol: ADPC

7	6	5	4	3	2	1	0
0	0	0	0	ADPC3	ADPC2	ADPC1	ADPC0
0	0	0	0	**0**	**0**	**1**	**0**

Bits 3 to 0

ADPC3	ADPC2	ADPC1	ADPC0	Available Analog Input
0	**0**	**1**	**0**	**ANI0**

Symbol: PM2

7	6	5	4	3	2	1	0
PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20
x	x	x	x	x	x	x	**1**

Bit 0

PM20	PM20 I/O Mode Select
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

Note: For details on the procedure for setting up the registers, refer to RL78/G14 User's Manual: Hardware.

5.7.4 CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock.

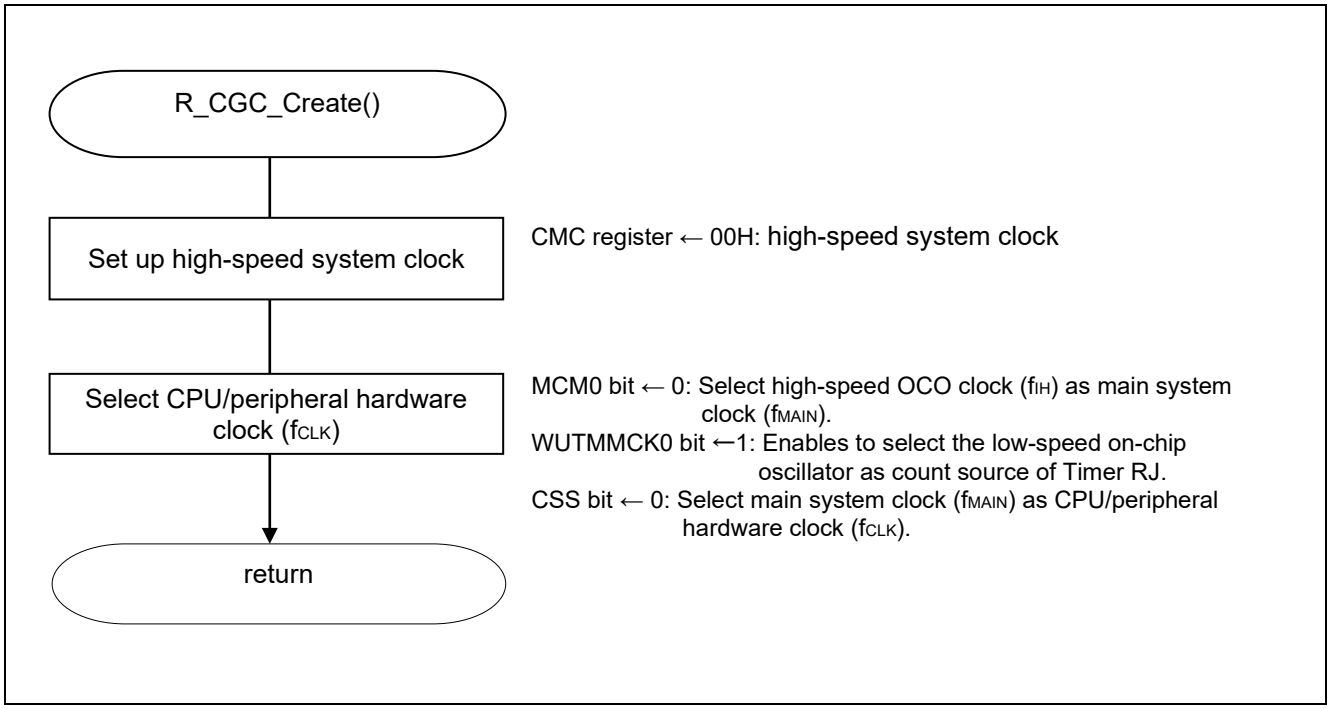

Figure 5.5 CPU Clock Setup

Note: For details on the procedure for setting up the CPU clock (R_CGC_Create ()), refer to the section entitled
"Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E).

5.7.5 A/D Converter Setup

Figure 5.6 shows the flowchart for setting up the A/D converter.

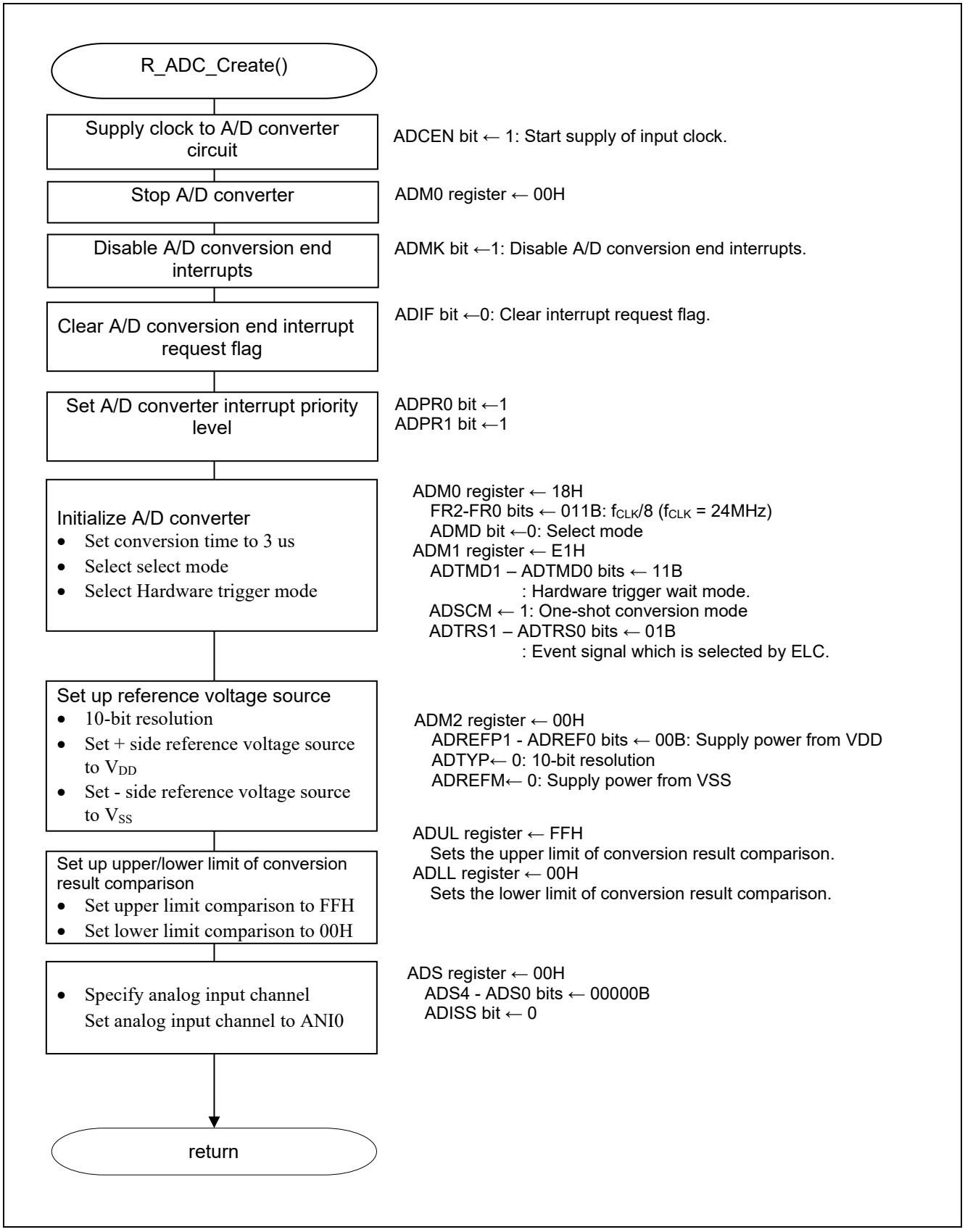

Figure 5.6 A/D Converter Setup Flowchart

Starting the supply of clock to the A/D converter

- Peripheral enable register 0 (PER0)
  Starts the supply of the clock to the A/D converter.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
x	x	**1**	x	x	x	x	x

Bit 5

ADCEN	A/D converter input clock control
0	Stops input clock supply.
1	**Enables input clock supply.**

Setting up the A/D conversion time and operation mode

- A/D converter mode register 0 (ADM0)
  Controls the A/D conversion operation.
  Specifies the A/D conversion channel selection mode.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
x	**0**	**0**	**1**	**1**	**0**	**0**	x

Bit 6

ADMD	Specification of the A/D conversion channel selection mode
0	**Select mode**
1	Scan mode

Bits 5 - 1

ADM0					Mode	Conversion Clock (f_{AD})	The number of Stabilization Wait Clock	The Number of Conversion Clock	Stabilization Wait Time + Conversion Time	Selection of Stabilization Wait Time + Conversion Time (f_{CLK}=24MHz)
FR2	FR1	FR0	LV1	LV2						
0	**1**	**1**	**0**	**0**	**Normal1**	**f_{CLK}/8**	**8f_{AD}**	**19 f_{AD} (the number of Sampling clock:7 f_{AD})**	**216/f_{CLK}**	**9µs**

Note: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting up the A/D conversion trigger mode

- A/D converter mode register 1 (ADM1)
  Selects the A/D conversion trigger mode.
  Selects the A/D conversion mode.
  Selects the hardware trigger signal.

Symbol: ADM1

7	6	5	4	3	2	1	0
ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0
1	**1**	**1**	x	x	x	**1**	**0**

Bit 7 - 6

ADTMD1	ADTMD0	Selection of the A/D conversion trigger mode
0	x	Software trigger mode
1	0	Hardware trigger no-wait mode
1	**1**	**Hardware trigger wait mode**

Bit 5

ADSCM	Specification of the A/D conversion mode
0	Sequential conversion mode
1	**One-shot conversion mode**

Bit 1 - 0

ADTRS1	ADTRS0	Selection of the hardware trigger signal
0	0	End of timer channel 01 count or capture interrupt signal (INTTM01)
0	**1**	**Event signal selected by ELC**
1	0	Real-time clock interrupt signal (INTRTC)
1	1	12-bit interval timer interrupt signal (INTIT)

Note: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting up the reference voltage

- A/D converter mode register 2 (ADM2)
  Selection of the + side reference voltage source of the A/D converter.
  Selection of the - side reference voltage source of the A/D converter.
  Checking the upper limit and lower limit conversion result values.
  Specification of the SNOOZE mode.

Symbol: ADM2

7	6	5	4	3	2	1	0
ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADYTP
0	**0**	**0**	x	**0**	**0**	**0**	**0**

Bit 7 - 6

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	**0**	**Supplied from V_{DD}.**
0	1	Supplied from P20/AV_{REFP}/ANI0.
1	0	Supplied from internal reference voltage (1.45 V).
1	1	Setting prohibited

Bit 5

ADREFM	Selection of the - side reference voltage source of the A/D converter
0	**Supplied from V_{SS}.**
1	Supplied from P21/AV_{REFM}/ANI1.

Bit 3

ADRCK	Checking the upper limit and lower limit conversion result values
0	**The interrupt signal (INTAD) is output when the ADLL register ≤ the ADCR register ≤ the ADUL register (AREA1)**
1	Interrupt signal (INTAD) is output when ADCR register < ADLL register and ADUL register < ADCR register.(AREA3)

Bit 2

AWC	Specification of the SNOOZE mode
0	**Do not use the SNOOZE mode function.**
1	Use the SNOOZE mode function.

Bit 0

ADTYP	Selection of the A/D conversion resolution
0	**10-bit resolution**
1	8-bit resolution

Note: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting up the conversion result comparison upper limit/lower limit

- Conversion result comparison upper limit setting register (ADUL)
- Conversion result comparison lower limit setting register (ADLL)
  Sets up the conversion result comparison upper- and lower-limit values.

Symbol: ADUL

7	6	5	4	3	2	1	0
ADUL7	ADUL6	ADUL5	ADUL4	ADUL3	ADUL2	ADUL1	ADUL0
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Symbol: ADLL

7	6	5	4	3	2	1	0
ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Specifying the input channel

- Analog input channel specification register (ADS)
  Specifies the input channel for the analog voltage to be subjected to A/D conversion.

Symbol: ADS

7	6	5	4	3	2	1	0
ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0
0	x	x	**0**	**0**	**0**	**0**	**0**

Bit 7, 4 - 0

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	**0**	**0**	**0**	**0**	**0**	**ANI0**	**P20/ANI0/AV$_{REFP}$ pin**

Note: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting up end of A/D conversion interrupts

- Interrupt request flag register (IF1H)
  Clears the interrupt request flag.
- Interrupt mask flag register (MK1H)
  Disables interrupts.

Symbol: IF1H

7	6	5	4	3	2	1	0
TMIF10	TRJIF0	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
x	x	x	x	x	x	x	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated.**
1	Interrupt request is generated, interrupt request status.

Symbol: MK1H

7	6	5	4	3	2	1	0
TMMK10	TRJMK0	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
x	x	x	x	x	x	x	**1**

Bit 0

ADMK	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Note: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

5.7.6 Timer RJ Setup

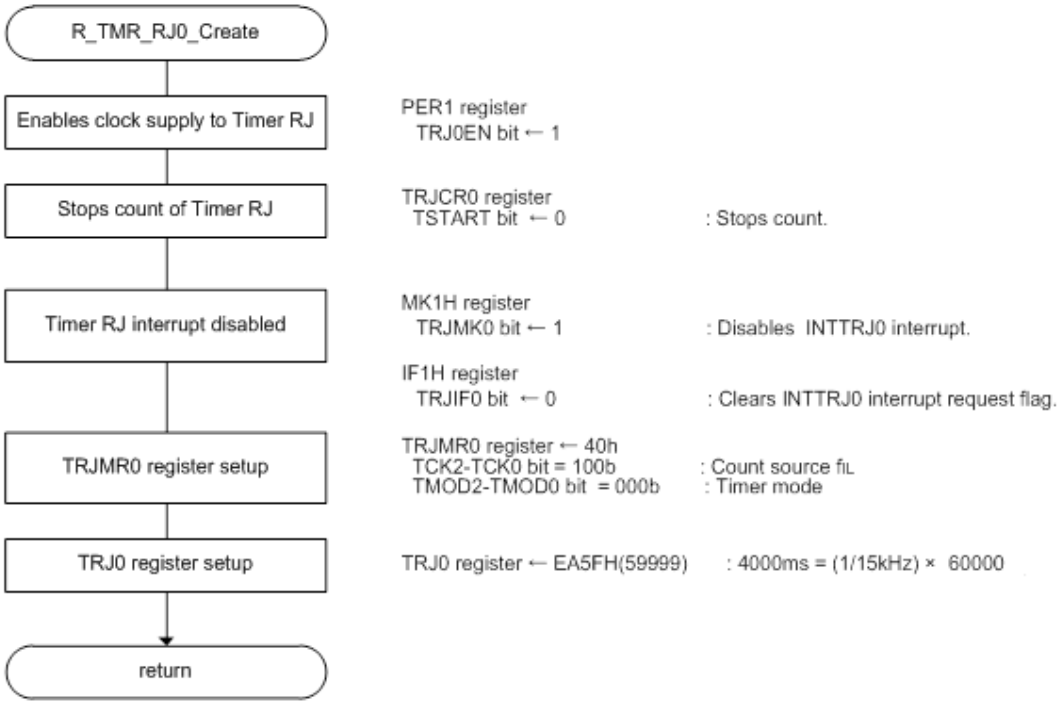

Figure 5.7 shows Timer RJ setup.

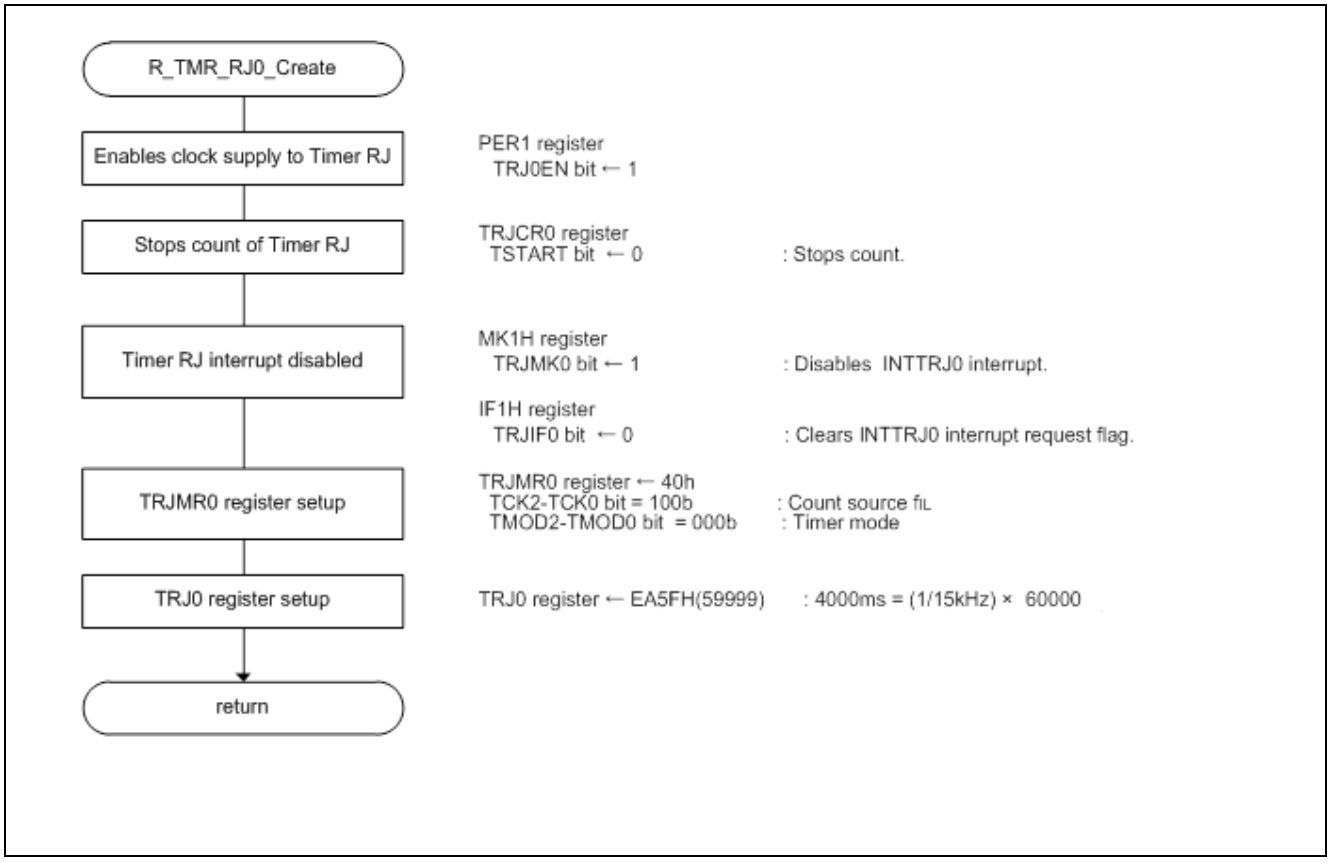

Figure 5.7 Setup of Timer RJ

Start supplying clock to Timer RJ

- Peripheral enable register 1 (PER1)
  Starts supplying clock to Timer RJ.

Symbol: PER1

7	6	5	4	3	2	1	0
DACEN	TRGEN	CMPEN	TRD0EN	DTCEN	0	0	TRJ0EN
x	x	x	x	x	x	x	**1**

Bit 0

TRJ0EN	Control of timer RJ0 input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Setup of Timer RJ operation and interrupt level

- Timer RJ control register 0 (TRJCR0)
  Stops Timer RJ counter operation.
  Sets the interrupt cycle.

Symbol: TRJCR0

7	6	5	4	3	2	1	0
0	0	TUNDF	TEDGF	0	TSTOP	TCSTF	TSTART
x	x	x	x	x	x	x	**0**

Bit 0

TSTART	Timer RJ count start
0	**Count stops**
1	Count starts

Note: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setup of Timer RJ interrupt

- Interrupt request flag register (IF1H)
  Clears interrupt request flag.
- Interrupt mask flag register (MK1H)
  Interrupt processing disabled.

Symbol: IF1H

7	6	5	4	3	2	1	0
TMIF10	TRJIF0	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
x	**0**	x	x	x	x	x	x

Bit 6

TRJIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK1H

7	6	5	4	3	2	1	0
TMMK10	TRJMK0	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
x	**1**	x	x	x	x	x	x

Bit 6

TRJMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Note: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Timer RJ setup

- Timer RJ mode register 0 (TRJMR0)
  Count source selection and operation mode selection.
- Timer RJ counter register 0 (TRJ0)
  Setup of Timer RJ interrupt cycles.

Symbol: TRJMR0

7	6	5	4	3	2	1	0
0	TCK2	TCK1	TCK0	TEDGPL	TMOD2	TMOD1	TMOD0
x	**1**	**0**	**0**	x	x	x	x

Bit 6 - 4

TCK2	TCK1	TCK0	Timer RJ count source select
0	0	0	f_{CLK}
0	0	1	$f_{CLK}/8$
0	1	1	$f_{CLK}/2$
1	**0**	**0**	**f_{IL}**
1	0	1	Event input from ELC
1	1	0	f_{SUB}
Other than above			Setting prohibited

Bit 2 - 0

TMOD2	TMOD1	TMOD0	Timer RJ operating mode select
0	**0**	**0**	**Timer mode**
0	0	1	Pulse output mode
0	1	0	Event counter mode
0	1	1	Pulse width measurement mode
1	0	0	Pulse period measurement mode
Other than above			Setting prohibited

Symbol: TRJ0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Generation of Timer RJ interrupt (INTTRJ0) = (Setup value of TRJ0 + 1) × Count clock period

Note: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

5.7.7 ELC Initialization

Figure 5.8 shows ELC initialization.

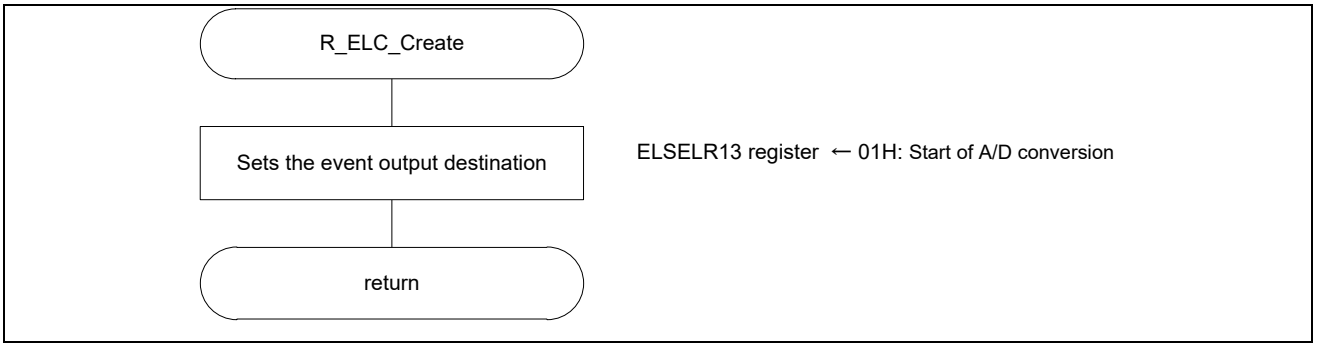

Figure 5.8 ELC Initialization

Setup of event output destination

- Event output destination select register 13 (ELSELR13)

Symbol: ELSELR13

7	6	5	4	3	2	1	0
0	0	0	0	ELSELR133	ELSELR132	ELSELR131	ELSELR130
x	x	x	x	**0**	**0**	**0**	**1**

Bit 3 - 0

ELSELR133	ELSELR132	ELSELR131	ELSELR130	Event Link Selection
0	0	0	0	Event link disabled
0	**0**	**0**	**1**	**Link destination peripheral function : A/D converter** **Operation when receiving event : A/D conversion starts**
0	0	1	0	Select operation of peripheral function to link.
0	0	1	1	Select operation of peripheral function to link.
0	1	0	0	Select operation of peripheral function to link.
0	1	0	1	Select operation of peripheral function to link.
0	1	1	0	Select operation of peripheral function to link.
0	1	1	1	Select operation of peripheral function to link.
1	0	0	0	Select operation of peripheral function to link.
1	0	0	1	Select operation of peripheral function to link.

5.7.8 Main Processing

Figure 5.9 shows the main processing.

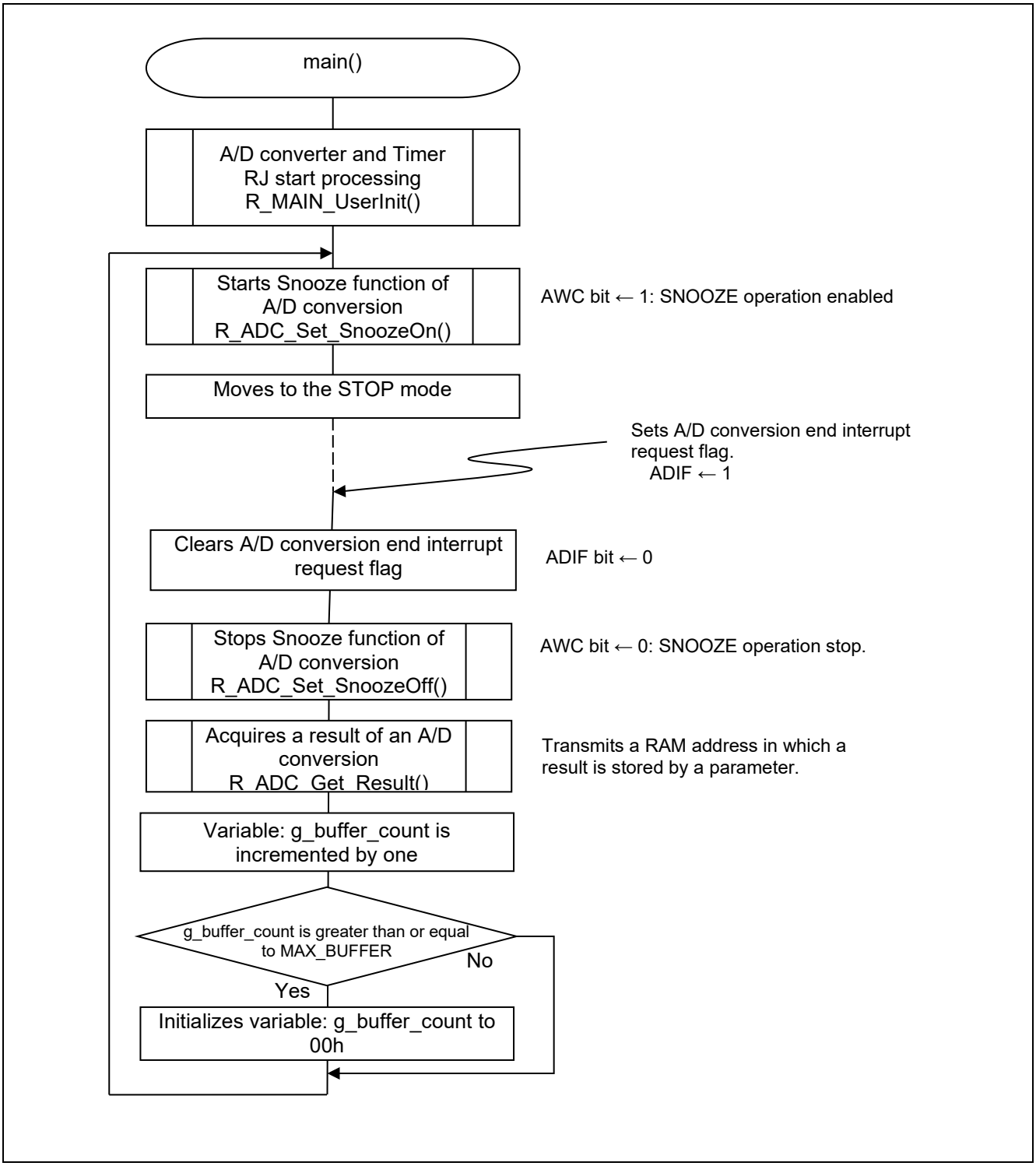

Figure 5.9 Main Processing

Setup of interrupt request flag

- Interrupt request flag register (IF1H)
  Clears the interrupt request flag.

Symbol: IF1H

7	6	5	4	3	2	1	0
TMIF10	TRJIF0	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
x	x	x	x	x	x	x	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated.**
1	Interrupt request is generated, and enters into interrupt request status.

Note: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

5.7.9 Operation Start Processing of A/D Converter and Timer RJ

Figure 5.10 shows the operation start processing of A/D converter and Timer RJ.

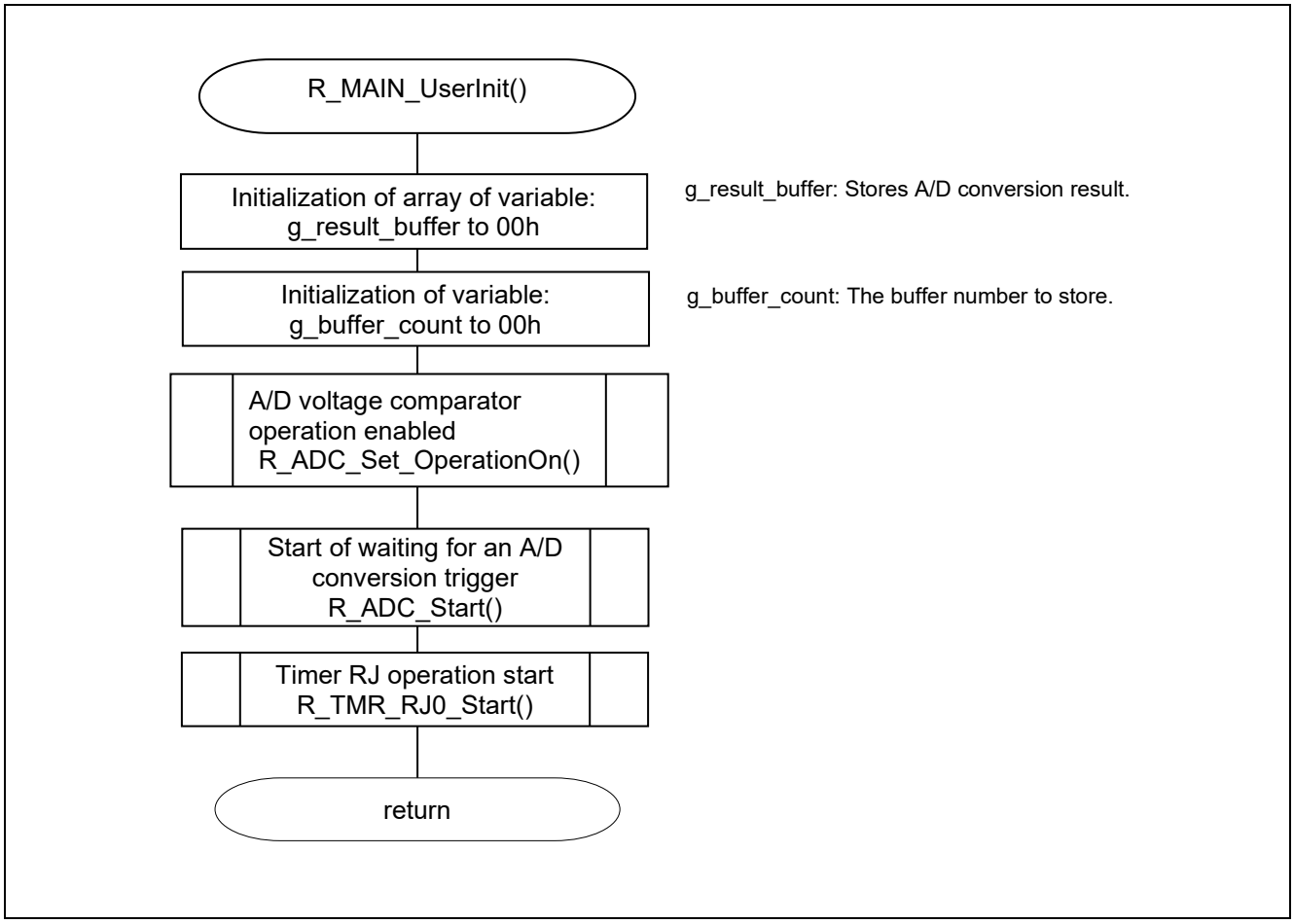

Figure 5.10 Operation Start Processing of A/D Converter and Timer RJ

5.7.10 Enabling the A/D Voltage Comparator

Figure 5.11 shows the flowchart for enabling the A/D voltage comparator.

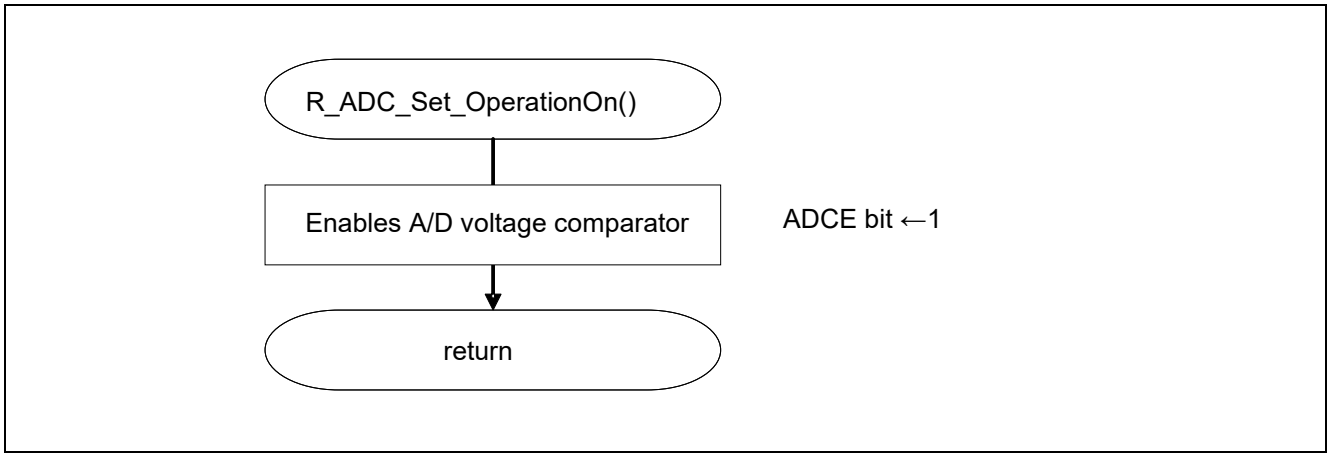

Figure 5.11 Enabling the A/D Voltage Comparator

Start of A/D voltage comparator

- A/D converter mode register 0 (ADM0)
  Controls the operation of the A/D voltage comparator.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
x	x	x	x	x	x	x	**1**

Bit 0

ADCE	A/D voltage comparator operation control
0	Stops A/D voltage comparator operation.
1	**Enables A/D voltage comparator operation.**

Note: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

5.7.11 Start of Waiting for An A/D Conversion Trigger

Figure 5.12 shows the waiting for an A/D conversion trigger.

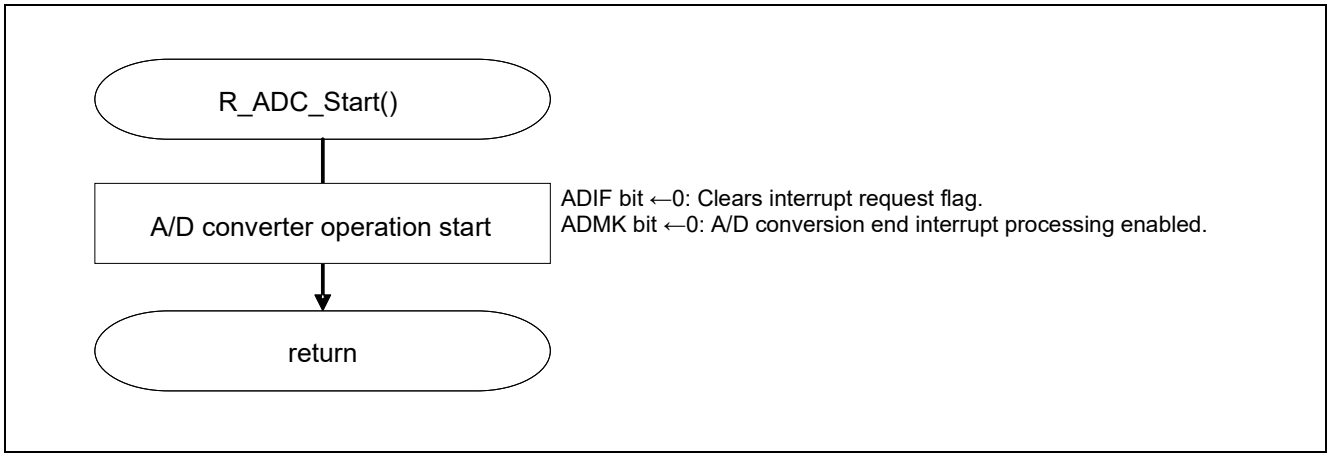

Figure 5.12 Start of Waiting for An A/D Conversion Trigger

Setting up end of A/D conversion interrupts

- Interrupt request flag register (IF1H)
  Clears the interrupt request flag.
- Interrupt mask flag register (MK1H)
  Disables interrupts.

Symbol: IF1H

7	6	5	4	3	2	1	0
TMIF10	TRJIF0	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
x	x	x	x	x	x	x	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated.**
1	Interrupt request is generated, and enters into interrupt request status.

Symbol: MK1H

7	6	5	4	3	2	1	0
TMMK10	TRJMK0	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
x	x	x	x	x	x	x	**0**

Bit 0

ADMK	Interrupt processing control
0	**Interrupt servicing enabled**
1	Interrupt servicing disabled

Note: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

5.7.12 Timer RJ Operation Start

Figure 5.13 shows the Timer RJ operation start.

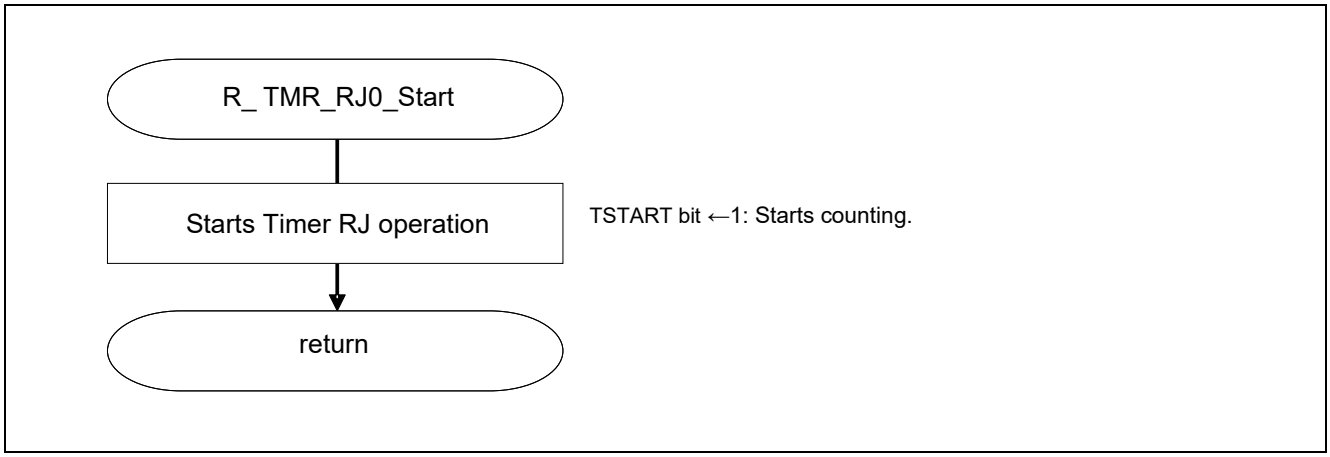

Figure 5.13 Timer RJ Operation Start

Setup of Timer RJ operation

- Timer RJ control register 0 (TRJCR0)
  Starts Timer RJ counter operation.

Symbol: TRJCR0

7	6	5	4	3	2	1	0
0	0	TUNDF	TEDGF	0	TSTOP	TCSTF	TSTART
x	x	x	x	x	x	x	**1**

Bit 0

TSTART	Timer RJ count start
0	Count stops
1	**Count starts**

Note: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

5.7.13 Start of Snooze Function of A/D Conversion

Figure 5.14 shows the start of snooze function of A/D conversion.

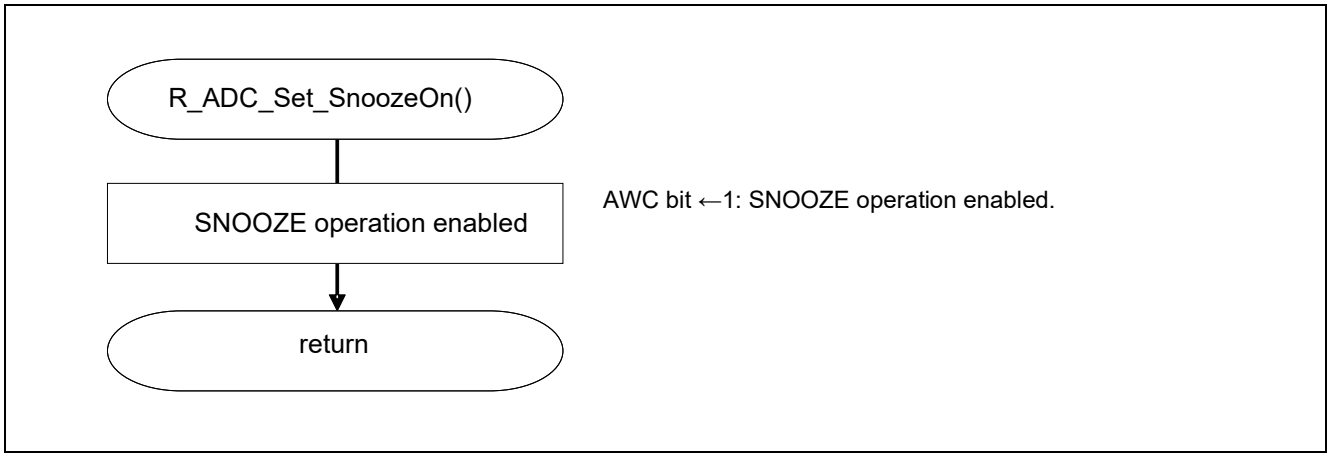

Figure 5.14 Start of Snooze Function of A/D Conversion

Setup of SNOOZE mode

- A/D converter mode register 2 (ADM2)
  Sets up SNOOZE mode.

Symbol: ADM2

7	6	5	4	3	2	1	0
ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADYTP
x	x	x	x	x	**1**	x	x

Bit 2

AWC	SNOOZE mode setup
0	Do not use the SNOOZE mode function.
1	**Use the SNOOZE mode function.**

Note: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

5.7.14 Stop Snooze Function of A/D Conversion

Figure 5.15 shows the stop snooze function of A/D conversion.

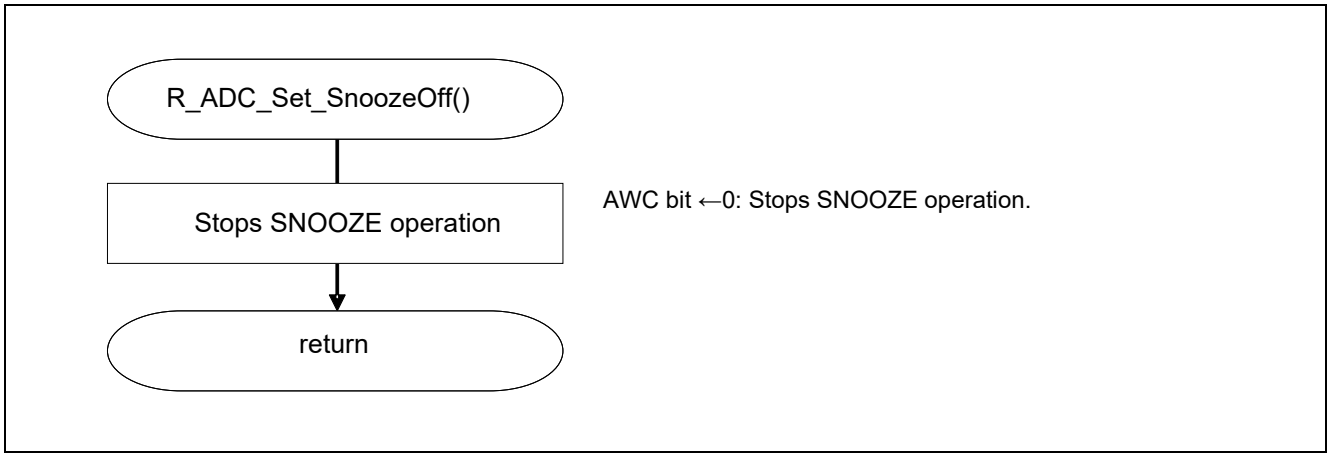

Figure 5.15 Stops Snooze Function of A/D Conversion

Setup of SNOOZE mode

- A/D converter mode register 2 (ADM2)
  Sets up SNOOZE mode.

Symbol: ADM2

7	6	5	4	3	2	1	0
ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADYTP
x	x	x	x	x	**0**	x	x

Bit 2

AWC	Setup of SNOOZE mode
0	**Do not use the SNOOZE mode function.**
1	Use the SNOOZE mode function.

Note: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

5.7.15 Acquisition of A/D Conversion Result

Figure 5.16 shows the acquisition of A/D conversion result.

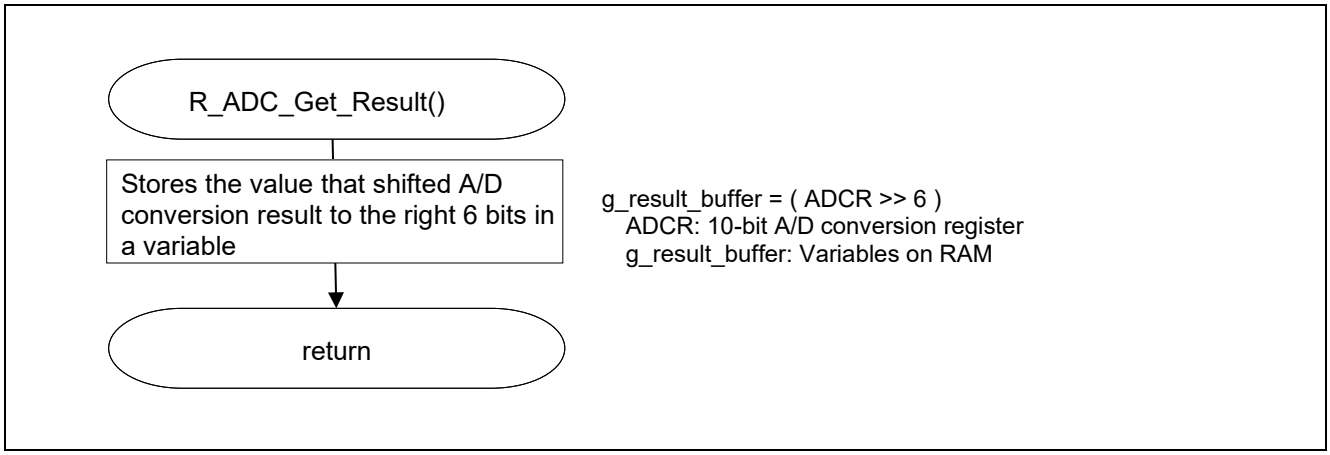

Figure 5.16 Acquisition of A/D Conversion Result

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G14 User's Manual: Hardware (R01UH0186E)
RL78 Family User's Manual: Software (R01US0015E)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Updates/Technical News
(The latest information can be downloaded from the Renesas Electronics website.)

Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Dec. 15, 2015	—	First edition issued
1.10	May, 11, 2022	5	Updated operation check conditions

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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