RL78/G23

Achieving a Watchdog Timer by Using the SNOOZE Mode Sequencer

Introduction

This application note describes how to achieve a watchdog timer function by using the SNOOZE mode sequencer (SMS) of an RL78/G23.

The SNOOZE mode sequencer can perform processing independently of the CPU. The SNOOZE mode sequencer runs a counter as a watchdog timer function. If the counter overflows before the CPU clears the counter, the SNOOZE mode sequencer generates an interrupt request. The interrupt request allows the CPU to detect that the counter was not cleared.

Target Device

RL78/G23

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specification

1.1 Overview of Specification

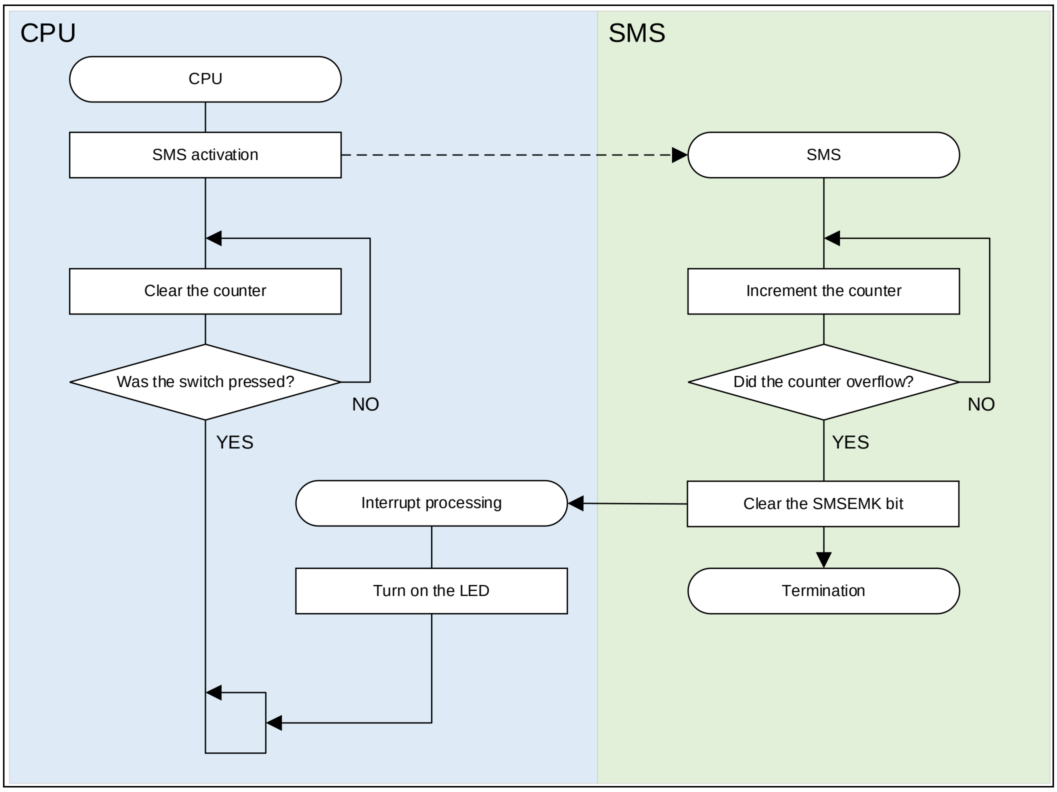
This application note describes how to achieve a watchdog timer function by using the SNOOZE mode sequencer of an RL78/G23.
The SNOOZE mode sequencer runs a counter as a watchdog timer function. The CPU periodically clears the counter so that the counter does not overflow.
The CPU stops clearing the counter when a switch is pressed. When one second elapses after counter clearance is stopped, the counter overflows and the SNOOZE mode sequencer generates an interrupt request. When the CPU detects the interrupt request, it turns on an LED.

Table 1-1 shows the peripheral functions to be used and Figure 1-1 shows an overview of operation.

Table 1-1 Peripheral Function and Use

Peripheral Function	Use
External interrupt (INTP3)	Triggers starting the SNOOZE mode sequencer.
SNOOZE mode sequencer	Runs a counter as a watchdog timer function and generates an interrupt request.

Figure 1-1 Operation overview



1.2 Outline of Operation

In this sample code, a low-level pulse is output from the P30 pin to generate an external interrupt request (INTP3). This external interrupt request triggers start of the SNOOZE mode sequencer. The SNOOZE mode sequencer increments the counter and judges whether an overflow has occurred. The CPU repeats clearance of the counter so that the counter does not overflow.

The CPU stops clearing the counter when a switch is pressed. The SNOOZE mode sequencer continues to increment the counter, and then a counter overflow occurs when one second elapses. If an overflow occurs, the SNOOZE mode sequencer generates an interrupt request (INTSMSE). When the CPU detects this interrupt, it turns on an LED.

The following describes the major settings of the peripheral functions.

(1) Initial settings of the external interrupt

- Set the INTP3 pin so that the falling edge is the effective edge.
- Set the P30 pin for output (as a trigger to start the SNOOZE mode sequencer).

(2) Initial settings of the SNOOZE mode sequencer

For details about the values to be set, see "4.7 Setting Up the SNOOZE Mode Sequencer".

2. Operation Confirmation Conditions

The operation of the sample code provided with this application note has been tested under the following conditions.

Table 2-1 Operation Confirmation Conditions

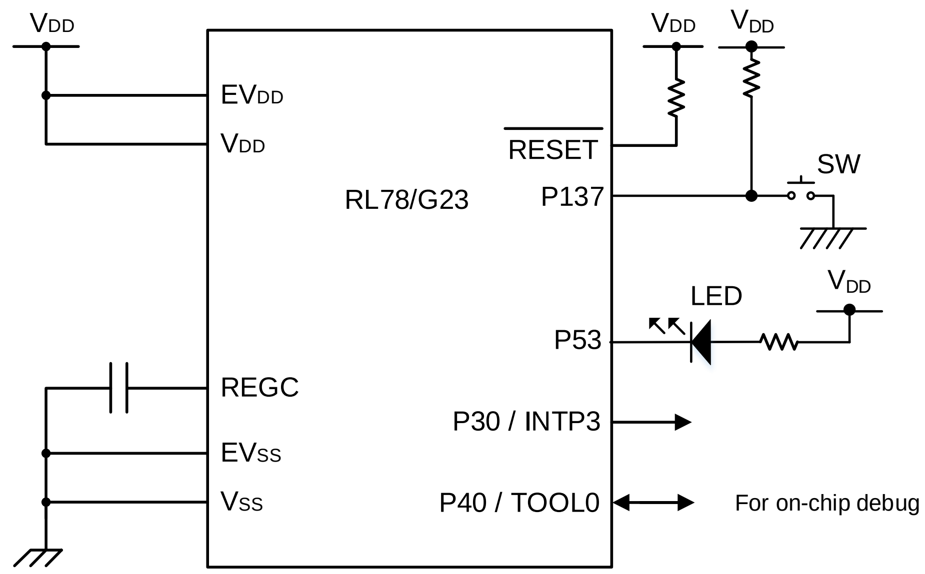
Item	Description
MCU used	RL78/G23 (R7F100GLG)
Board used	RL78/G23 Fast Prototyping Board (RTK7RLG230CLG000BJ)
Operating frequency	● High-speed on-chip oscillator clock (f_{IH}): 32 MHz ● Low-speed on-chip oscillator clock (f_{IL}): 32.768 kHz ● CPU/peripheral hardware clock: 32 MHz
Operating voltage	During V_{DD} operation: 3.3 V LVD0 detection voltage: Reset mode At rising edge TYP. 1.90 V (1.84 V to 1.95 V) At falling edge TYP. 1.86 V (1.80 V to 1.91 V)
Integrated development environment (CS+)	CS+ V8.09.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.12.00 from Renesas Electronics Corp.
Integrated development environment (e2studio)	e2 studio V2023-04 (23.4.0) from Renesas Electronics Corp.
C compiler (e2studio)	CC-RL V1.12.00 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V4.21.2 from IAR Systems Corp.
C compiler (IAR)	IAR C/C++ Compiler for Renesas RL78 V4.21.2.2420 from IAR Systems Corp.

3. Hardware Descriptions

3.1 Example of Hardware Configuration

Figure 3-1 shows an example of the hardware configuration used in the application note.

Figure 3-1 Hardware Configuration



Note 1. This schematic circuit diagram is simplified to show the outline of connections. When creating circuits, design them so that they meet electrical characteristics by properly performing pin processing. (Connect input-only ports to V_{DD} or V_{SS} individually through a resistor.)

Note 2. Connect pins (with a name beginning with EV_{SS}), if any, to V_{SS}, and connect pins (with a name beginning with EV_{DD}), if any, to V_{DD}.

3.2 List of Pins to be Used

Table 3-1 lists the pins to be used and their functions.

Table 3-1 Pins to be Used and Their Functions

Pin name	I/O	Function
P30 / INTP3	Output	SNOOZE mode sequencer activation trigger
P53	Output	LED lights
P137	Input	Switch Inputs

In this application note, the P30 and INTP3 pins, which are used as external interrupts, are set for output. This is because the high/low level of the output from the P30 pin is controlled by using a CPU instruction to generate an external interrupt request (from the INTP3 pin) that triggers the SNOOZE mode sequencer.

Caution In this application note, only thMe used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

4. Software Explanation

4.1 Setting of Option Byte

Table 4-1 shows the option byte settings.

Table 4-1 Option Byte Settings

Address	Setting Value	Contents
000C0H / 040C0H	11101111B	Disables the watchdog timer. (Counting stopped after reset)
000C1H / 040C1H	11111110B	LVD0 detection voltage: Reset mode At rising edge TYP. 1.90 V (1.84 V ～ 1.95 V) At falling edge TYP. 1.86 V (1.80 V ～ 1.91 V)
000C2H / 040C2H	11101000B	HS mode, High-speed on-chip oscillator clock (f_{IH}): 32 MHz
000C3H / 040C3H	10000100B	Enables on-chip debugging

4.2 List of Constants

Table 4-2 Constants lists the constants that are used in the sample code.

Table 4-2 Constants

Constant Name	Setting Value	Description
COUNTER_CLEAR	0x0000	Counter clear value
COUNTER_VALUE	0x00FA	Counter compare value (1 second setting value)

4.3 List of Variables

Table 4-3 lists global variables.

Table 4-3 Global Variables

Type	Variable Name	Description	Function Used
*(volatile __near unsigned short *) 0x3C2	p_sms_counter	Sequencer general-purpose register1 (SMSG1)	main r_main_user_init
*(volatile __near unsigned short *) 0x3C4	p_sms_count_value	Sequencer general-purpose register2 (SMSG2)	main r_main_user_init

4.4 List of Functions

Table 4-4 shows a list of functions.

Table 4-4 Functions

Function Name	Outline
main()	Main processing
r_main_user_init()	Main initial settings
r_main_sms_trigger()	SNOOZE mode sequencer activation
r_Config_SMS_interrupt()	INTSMSE interrupt processing

4.5 Specification of Functions

The function specifications of the sample code are shown below.

main()

Outline	Main processing
Header	r_cg_macrodriver.h、Config_INTC.h、Config_SMS.h、r_cg_userdefine.h
Declaration	void main(void);
Description	This function periodically clears the counter until a switch is pressed.
Argument	None
Return Value	None

r_main_user_init()

Outline	Main initial settings
Header	r_cg_macrodriver.h、Config_INTC.h、Config_SMS.h、r_cg_userdefine.h
Declaration	static void r_main_user_init(void);
Description	This function specifies the initial settings for the peripheral functions that are used for the application.
Argument	None
Return Value	None

r_main_sms_trigger ()

Outline	SNOOZE mode sequencer activation
Header	r_cg_macrodriver.h、Config_INTC.h、Config_SMS.h、r_cg_userdefine.h
Declaration	static void r_main_sms_trigger(void);
Description	This function generates a trigger to start the SNOOZE mode sequencer.
Argument	None
Return Value	None

r_Config_SMS_interrupt ()

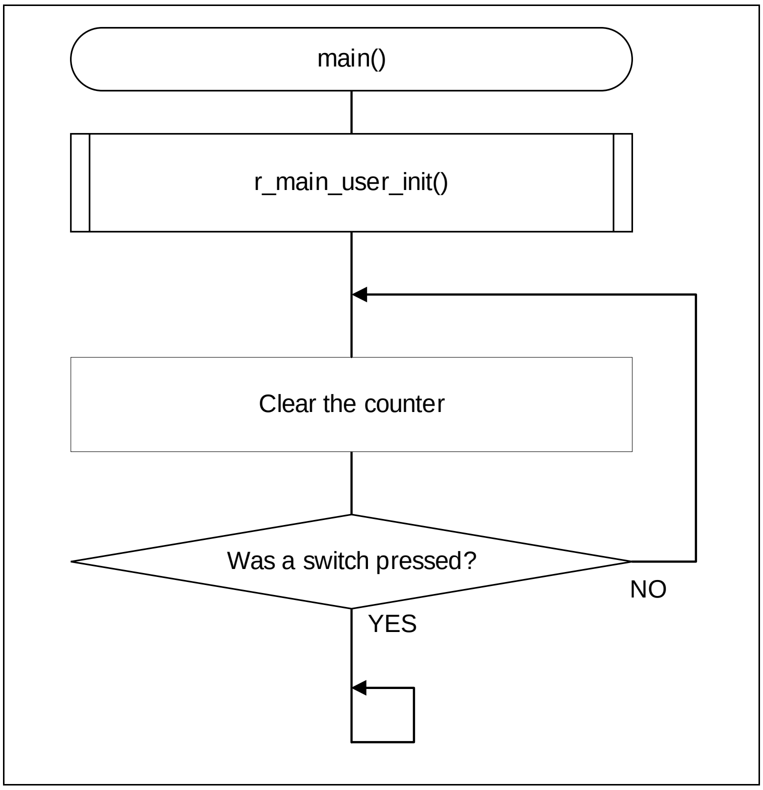
Outline	INTSMSE interrupt processing
Header	Config_SMS.h
Declaration	#pragma interrupt r_Config_SMS_interrupt(vect=INTSMSE)
Description	This function turns on an LED.
Argument	None
Return Value	None

4.6 Flowcharts

4.6.1 Main Processing

Figure 4-1 show flowcharts of the main processing.

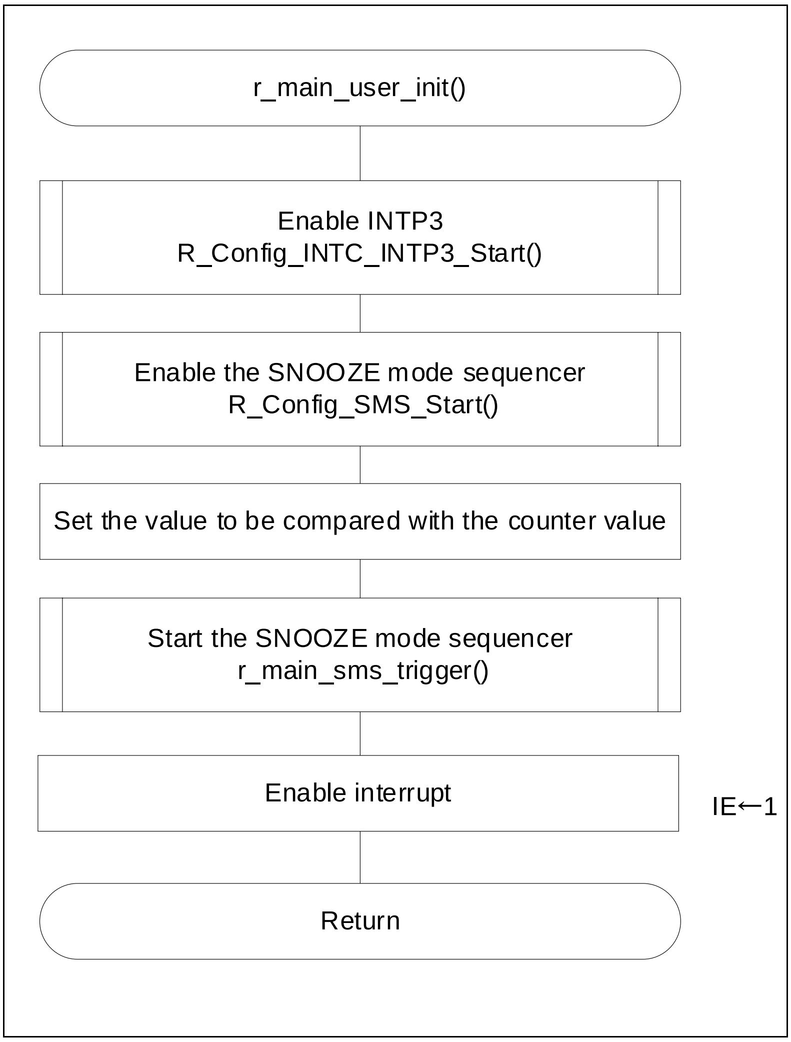
Figure 4-1 Main Processing



4.6.2 Main Initial Settings

Figure 4-2 shows the flowchart of the initial settings for main functions.

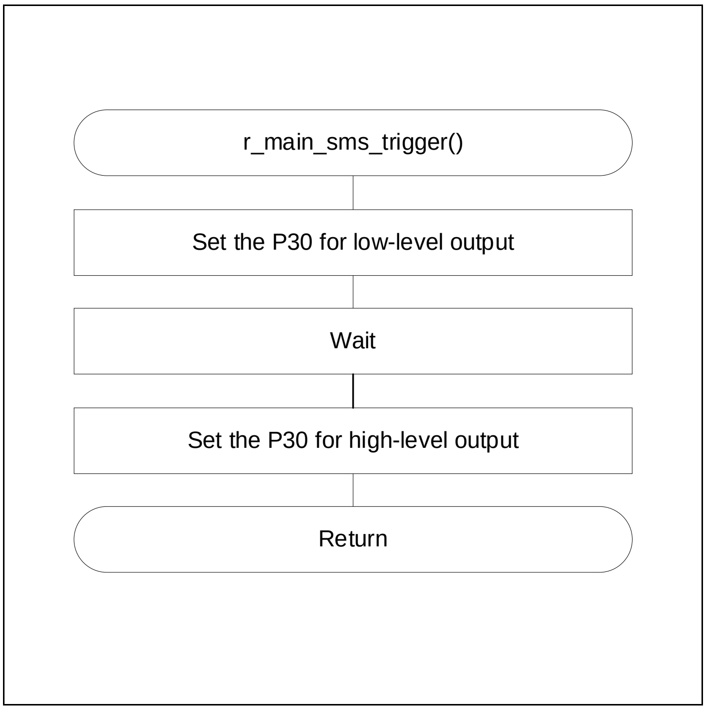
Figure 4-2 Main Initial Settings



4.6.3 SNOOZE Mode Sequencer Activation

Figure 4-3 shows the flowchart of the SNOOZE mode sequencer activation.

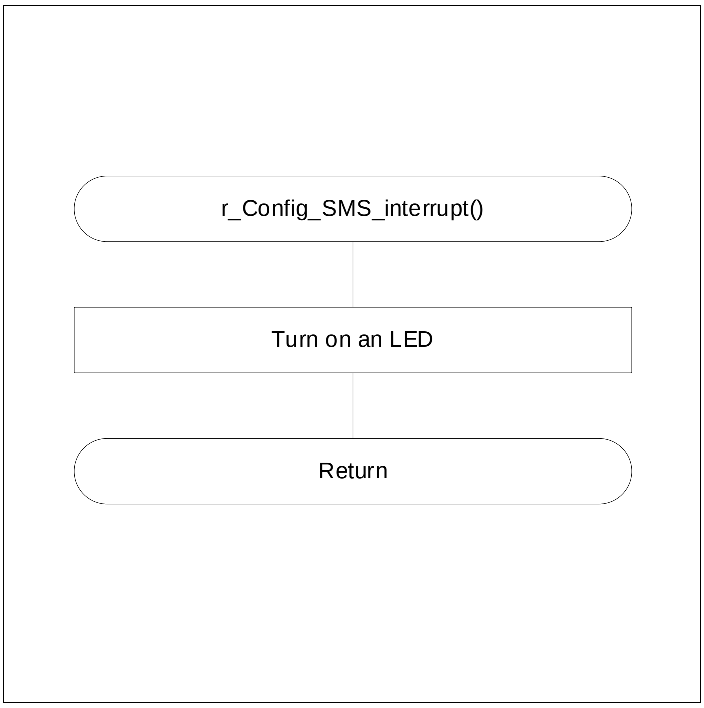
Figure 4-3 SNOOZE Mode Sequencer Activation



4.6.4 INTSMSE Interrupt Processing

Figure 4-4 shows the flowchart of the INTSMSE interrupt processing.

Figure 4-4 INTSMSE Interrupt Processing



4.7 Setting Up the SNOOZE Mode Sequencer

When the SNOOZE mode sequencer (SMS) is started by occurrence of a triggering event, it sequentially executes the processing commands that are stored in the sequencer instruction register (SMSI0-31). During execution of these commands, the sequencer general-purpose register (SMSG0-15) is used to store the source address, destination address, arithmetic data, and other data.

The SMSI0-31 and SMSG0-15 registers are set by coding an SMS program (.SMSASM file) in assembly language. You can also use the SNOOZE Mode Sequencer component of Smart Configurator to create an SMS program by combining processing blocks. The created SMS program is converted into C language by the assembler for SMS and then incorporated into the application program.

Figure 4-5 shows a flowchart of the processing of the SNOOZE mode sequencer.

Figure 4-5 Processing of the SNOOZE Mode Sequencer

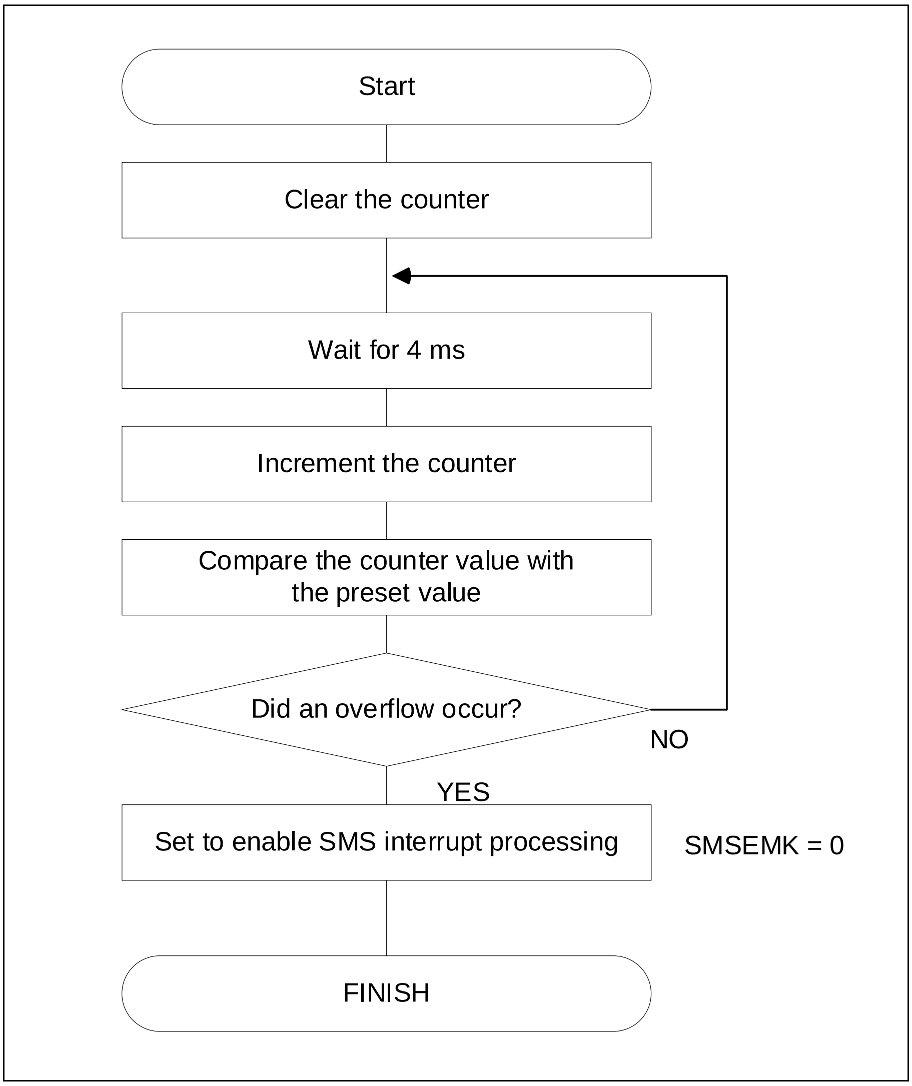


Table 4-1 Sequencer general-purpose registers 0-15

Register Symbol	Setting	Remark
SMSG0	0000H	fixed value: 0000H
SMSG1	0000H	Counter
SMSG2	0000H	Compare value
SMSG3	FFE5H	MK0H address
SMSG4	0001H	Increment value
SMSG5	03C0H	SMSG0 address
SMSG6	0000H	unused
SMSG7	0000H	unused
SMSG8	0000H	unused
SMSG9	0000H	unused
SMSG10	0000H	unused
SMSG11	0000H	unused
SMSG12	0000H	unused
SMSG13	0000H	unused
SMSG14	0000H	unused
SMSG15	FFFFH	fixed value: FFFFH

Table 4-2 Sequencer instruction registers 0-31

Register Symbol	Setting	Remark
SMSI0	3510H	MOVW SMSG1, [SMSG5+0]
SMSI1	9C21H	WAIT 194, 1
SMSI2	7140H	ADDW SMSG1, SMSG4
SMSI3	7122H	CMPW SMSG1, SMSG2
SMSI4	4FD1H	BC $1
SMSI5	5340H	CLR1 SMSG3.4
SMSI6	F000H	FINISH
SMSI7~31	0000H	unused

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RL78/G23 User's Manual: Hardware (R01UH0896)
RL78 family user's manual software (R01US0015)
The latest versions can be downloaded from the Renesas Electronics website.

Technical update
The latest versions can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2022.06.17	-	First Edition
1.10	2024.01.09	3	Corrected Figure 1-1 Operation overview
		5	Corrected Table 2-1 Operation Confirmation Conditions
		13	Corrected Figure 4-5 Processing of the SNOOZE Mode Sequencer
		14	Corrected Table 4-1 Sequencer general-purpose registers 0-15
		14	Corrected Table 4-2 Sequencer instruction registers 0-31
1.11	2024.07.24	6	Corrected hardware descriptions

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2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

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