RL78/G23

ELCL Chattering Prevention Function

Introduction

This application note describes how to implement a chattering prevention circuit in hardware using the logic and event link controller (ELCL). By using ELCL, the functions realized by external parts and software can be realized by hardware, therefore resources (external parts, ROM, RAM, etc.) can be reduced.

Target Device

RL78/G23

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

In this application note, ELCL is used to implement a chattering prevention circuit.

In the case of a switch with mechanical settings such as a button switch, the phenomenon (chattering) in which the contacts repeatedly turn on/off occurs when the switch is turned on/off. Therefore, in the embedded system, chattering prevention control is performed for the signal of the button switch to prevent malfunction so that the operation of pressing the button once and the operation of pressing it multiple times are not mistaken. The time that chattering occurs depends on the type of switch, and the range is from hundreds of microseconds to tens of milliseconds.

Figure 1-1 shows the switch waveform.

Figure 1-1 Switch waveform

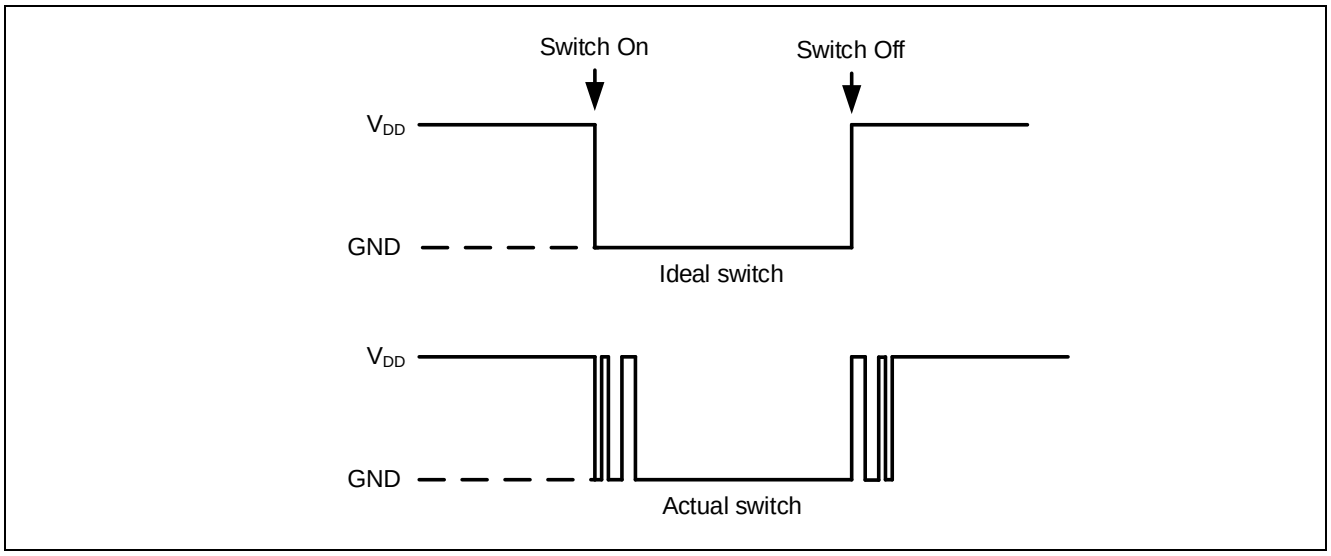


Figure 1-2 shows the system configuration for chattering prevention control using ELCL. The input signal from the external switch is INPUT A, and the output signal from the chattering prevention circuit is OUTPUT B. Use the delay count function of TAU0 to control the chattering prevention period.

Figure 1-2 System Configuration

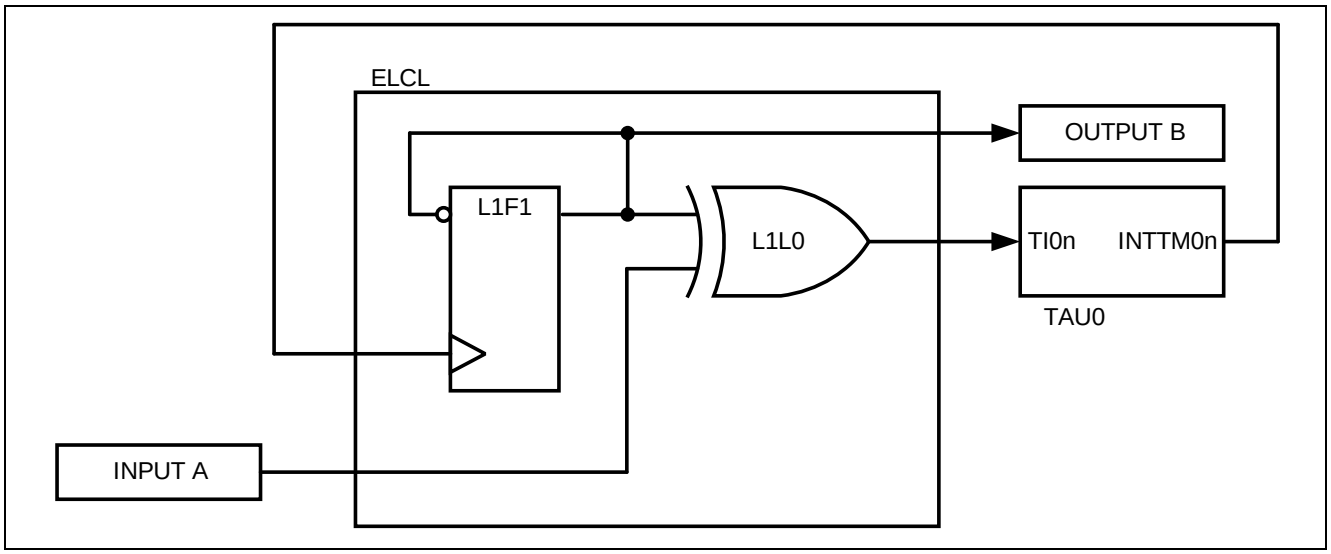


Figure 1-3 shows the timing chart of the system configuration in Figure 1-2. Table 1-1 gives an overview of Figure 1-3.

Figure 1-3 Timing chart of chattering prevention control

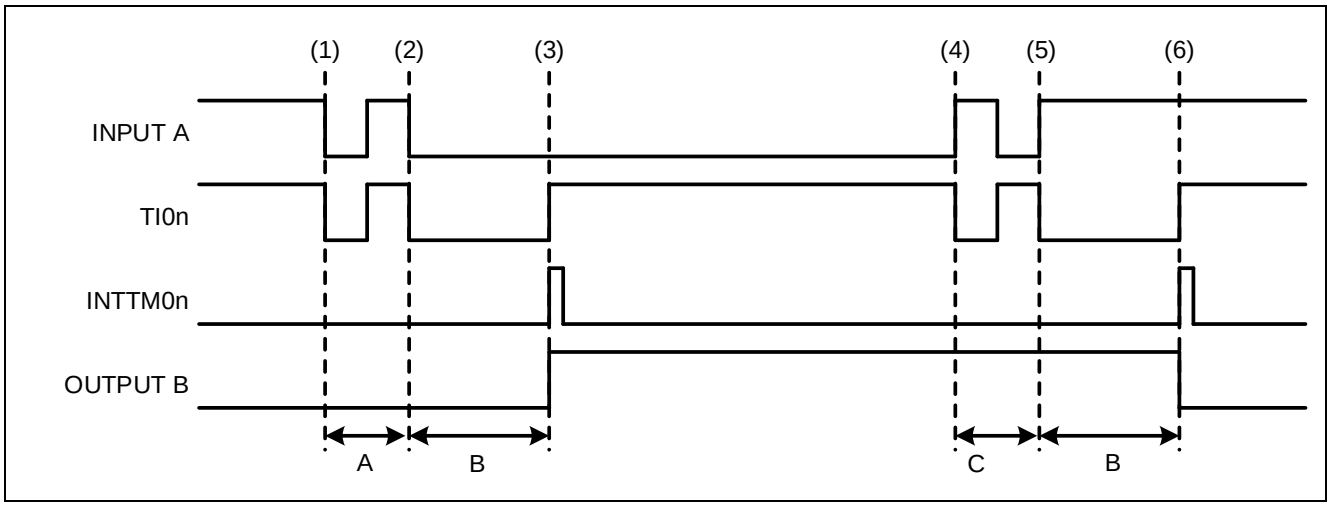


Table 1-1 Overview of chattering prevention control

No.	INPUT A	TAU0	INTTM0n	OUTPUT B
(1)	Press the switch High -> Low	Count start	Does not occur	Low
(2)	Chattering occurs High -> Low	Count restart	Does not occur because the period A is smaller than the setting interval B.	Low
(3)	Low	Completes counting of setting interval B, counting stop	Occur	Low -> High
(4)	Release the switch Low -> High	Count restart	Does not occur	High
(5)	Chattering occurs Low -> High	Count restart	Does not occur because the period C is smaller than the setting interval B.	High
(6)	High	Completes counting of setting interval B, counting stop	Occur	High -> Low

2. Conditions for Operation Confirmation Test

The sample code with this application note runs properly under the condition below.

Table 2-1 Operation Confirmation Conditions

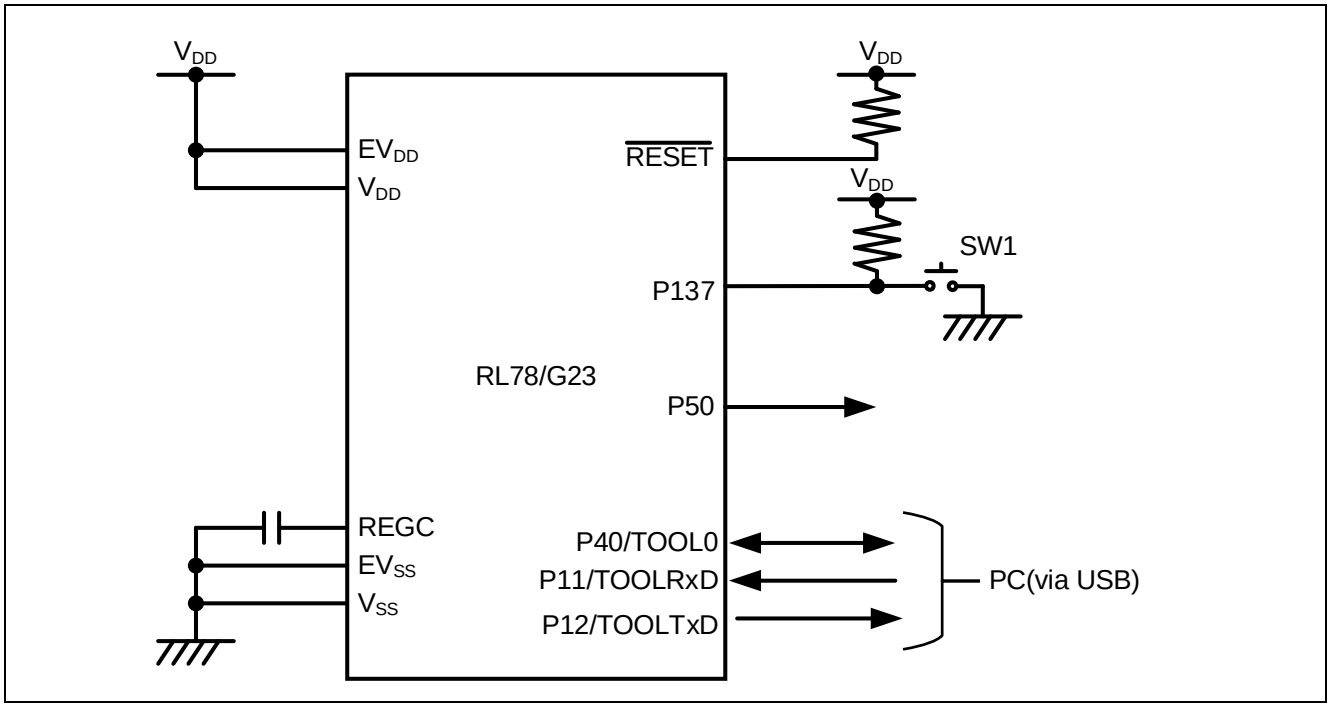
Items	Contents
MCU	RL78/G23 (R7F100GLG)
Operating frequencies	• High-speed on-chip oscillator clock: 32 MHz • CPU/peripheral hardware clock: 32 MHz
Operating voltage	• 3.3V • LVD0 operations (V_{LVD0}) : Reset mode Rising edge TYP.1.90V Falling edge TYP.1.86V
Integrated development environment (CS+)	CS+ for CC V8.11.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.13 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio 2024-07 (24.07.0) from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.13 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V5.10.3 from IAR Systems
C compiler (IAR)	
Smart Configurator	V.1.10.0
Board support package (r_bsp)	V.1.13
Emulator	CS＋, e^2 studio: COM port IAR: E2 Emulator Lite
Board	RL78/G23 Fast Prototyping Board (RTK7RLG230CLG000BJ)

3. Hardware

3.1 Example of Hardware Configuration

Figure 3-1 shows an example of the hardware configuration in this application.

Figure 3-1 Hardware Configuration



Caution 1. This simplified circuit diagram was created to show an overview of connections only. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements. (Connect each input-only port to V_{DD} or V_{SS} through a resistor.)

Caution 2. Connect the EV_{SS} pin to V_{SS} and the EV_{DD} pin to V_{DD}.

Caution 3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD0}) that is specified as LVD.

3.2 Used Pins

Table 3-1 shows list of used pins and assigned functions.

Table 3-1 List of Pins and Functions

Pin name	Input/Output	Function
P137	Input	SW1 (Low Active)
P50	Output	ELCL output signal (for monitor)

Caution. In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

4. Software

4.1 Overview of the sample program

In this sample code, chattering prevention control is performed for the input signal of SW1 (P137), and the signal generated by the chattering prevention circuit is output to P50.

Figure 4-1 shows the system configuration of the sample code, and Figure 4-2 shows the timing chart.

It is possible to check the chattering prevention control signal by selecting P50 as the link destination of the ELCL output signal.

Figure 4-1 System configuration of the sample code

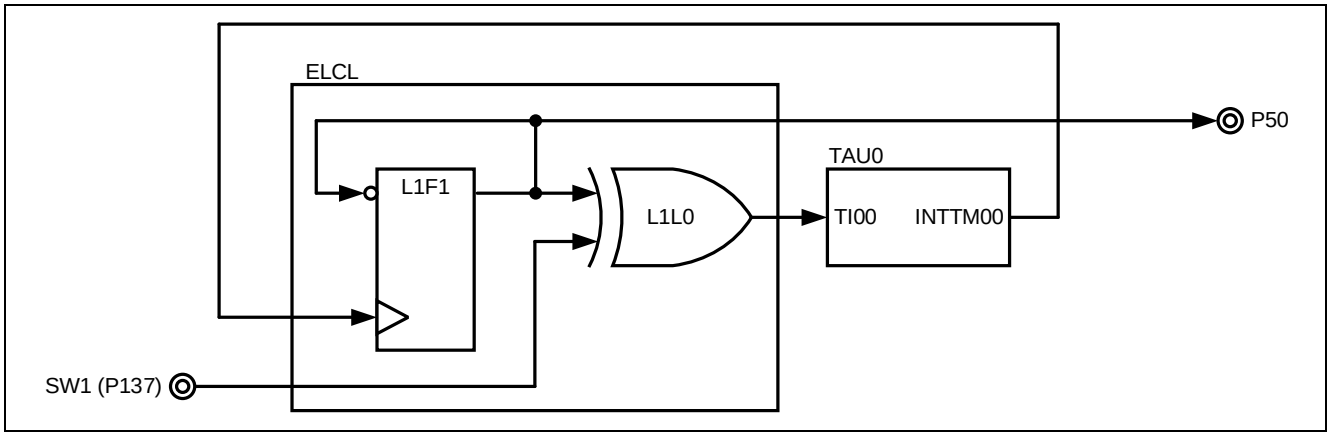
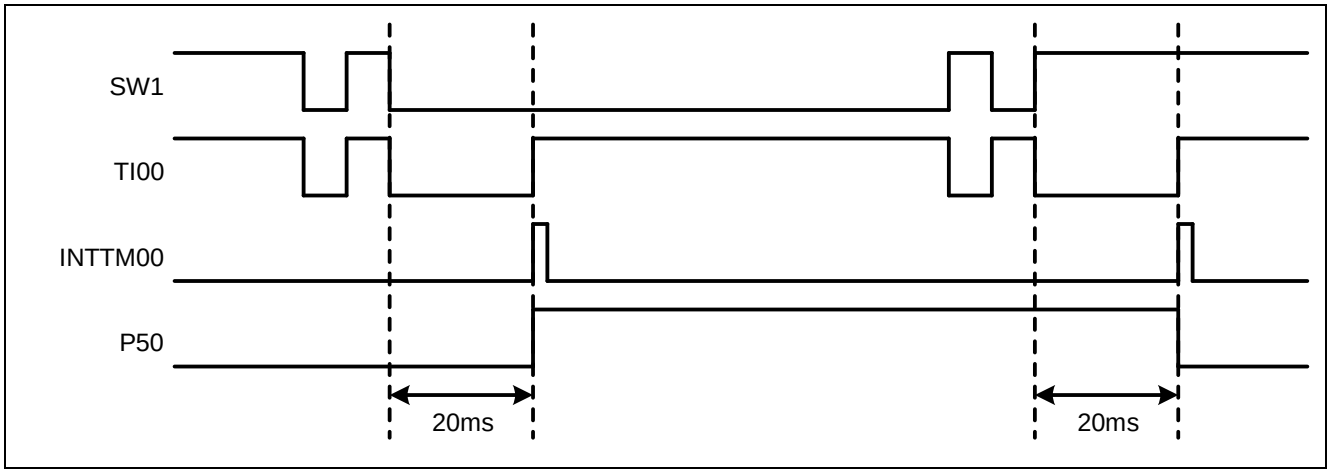


Figure 4-2 Timing chart of the sample code



4.2 Folder Configuration

Table 4-1 shows folder configuration of source file and header files using by sample code except the files generated by integrated development environment and the files in the bsp environment.

Table 4-1 Folder configuration

Folder/File configuration	Outline	Created by Smart configurator
¥r01an5612_elcl_chattering<DIR>Note 3	Root folder of this sample code	
¥src<DIR>	Folder for program source	
main.c	Sample code source file	
¥smc_gen<DIR>	Folder created by Smart Configurator	√
¥Config_ChatteringPrevention <DIR>	Folder for ELCL program	√
Config_ChatteringPrevention.c	Source file for ELCL	√
Config_ChatteringPrevention.h	Header file for ELCL	√
Config_ChatteringPrevention_ user.c	Interrupt source file for ELCL	√Note 1
¥Config_PORT<DIR>	Folder for PORT program	√
Config_PORT.c	Source file for PORT	√
Config_PORT.h	Header file for PORT	√
Config_PORT_user.c	Interrupt source file for PORT	√Note 1
¥Config_TAU0_0<DIR>	Folder for TAU0 channel 0 program	√
Config_TAU0_0.c	Source file for TAU0 channel 0	√Note 2
Config_TAU0_0.h	Header file for TAU0 channel 0	√
Config_TAU0_0_user.c	Interrupt source file for TAU0 channel 0	√Note 1
¥general<DIR>	Folder for initialize or common program	√
¥r_bsp<DIR>	Folder for BSP program	√
¥r_config<DIR>	Folder for program	√

Note. <DIR> means directory.

Note 1. Not used in this sample code.

Note 2. The IAR version of the sample code contains r01an5612_elcl_chattering.ipcf. For the ipcf file, refer to "RL78 Smart Configurator User Guide: IAR (R20AN0581)".

4.3 Option Byte Settings

Table 4-2 shows the option byte settings.

Table 4-2 Option Byte Settings

Address	Setting Value	Contents
000C0H/040C0H	1110 1111B (EFH)	Operation of Watchdog timer is stopped (counting is stopped after reset)
000C1H/040C1H	1111 1110B (FEH)	LVD0 operating mode: reset mode Detection voltage: Rising edge 1.90V Falling edge 1.86V
000C2H/040C2H	1110 1000B (E8H)	Flash operating mode: HS mode High-speed on-chip oscillator clock: 32MHz
000C3H/040C3H	1000 0101B (85H)	On-chip debugging is enabled

4.4 Constants

Constants are not used in this sample code.

4.5 Variables

Global variables are not used in this sample code.

4.6 Functions

Table 4-3 shows the functions used in the sample code. However, the unchanged functions generated by the Smart Configurator are excluded.

Table 4-3 Functions

Function name	Outline	Source file
Main	Main process	main.c

4.7 Function Specifications

This part describes function specifications of the sample code.

[Function name] main

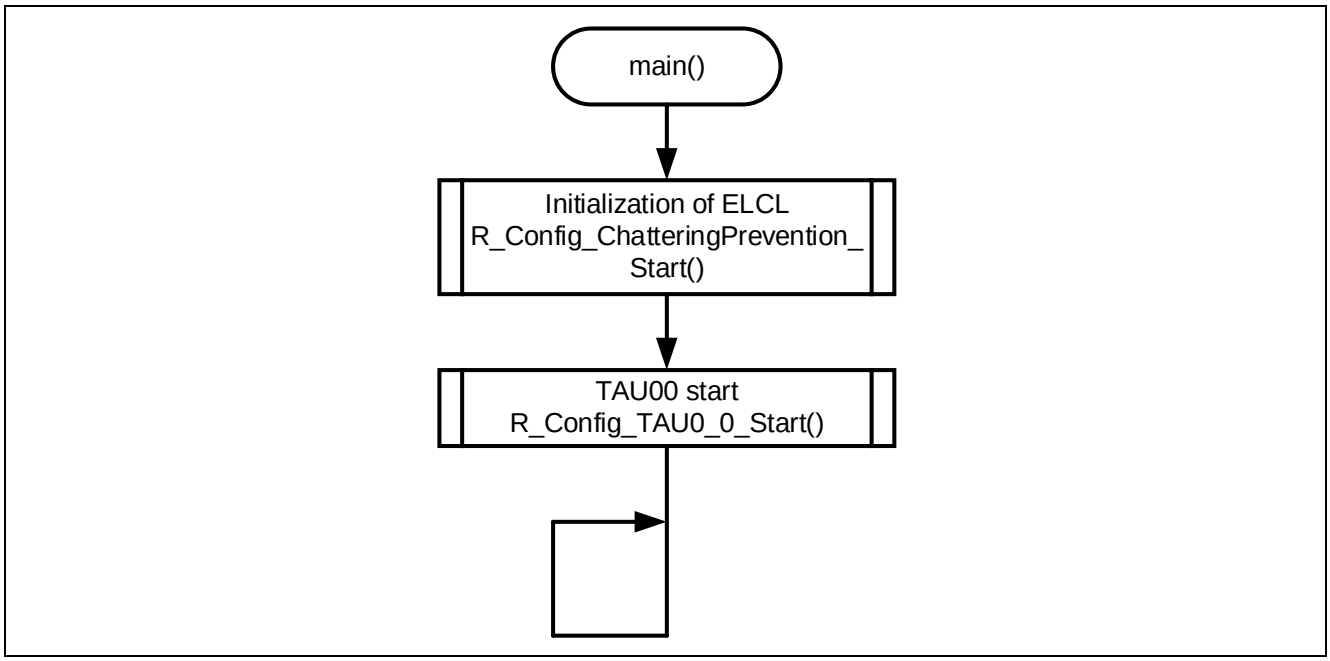
Outline	Main process
Header	r_smc_entry.h
Declaration	void main (void);
Description	This function initializes ELCL, and sets ELCL output. It starts the operation of TAU0 channel 0.
Arguments	None
Return value	None
Remarks	None

4.8 Flow Charts

4.8.1 Main Process

Figure 4-3 shows flowchart of main process.

Figure 4-3 Main process



5. Application example

In addition to the sample code, this application note contains the following Smart Configurator configuration files.

r01an5612_elcl_chattering.scfg

The following is a description of the file and examples of settings and notes for use.

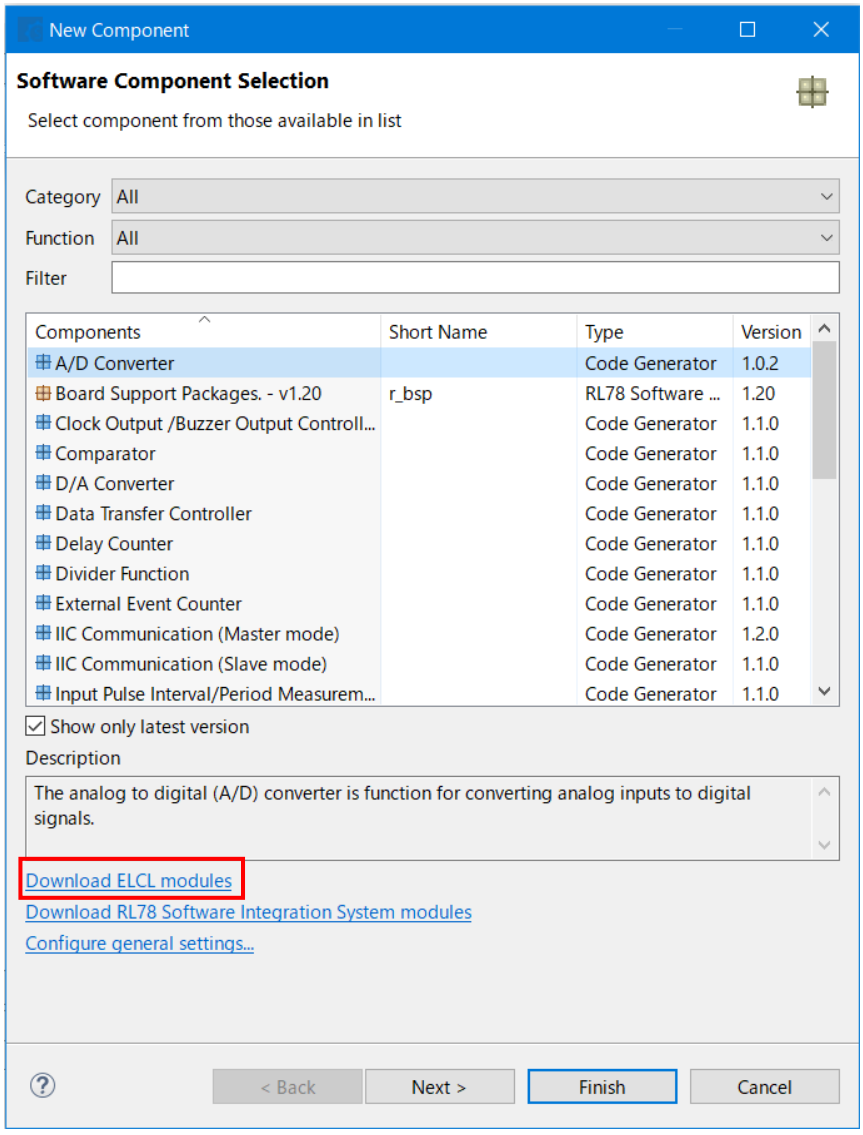
5.1 Setting up the ELCL components

To use the ELCL component, you need to install the ELCL content file.

The procedure is shown below.

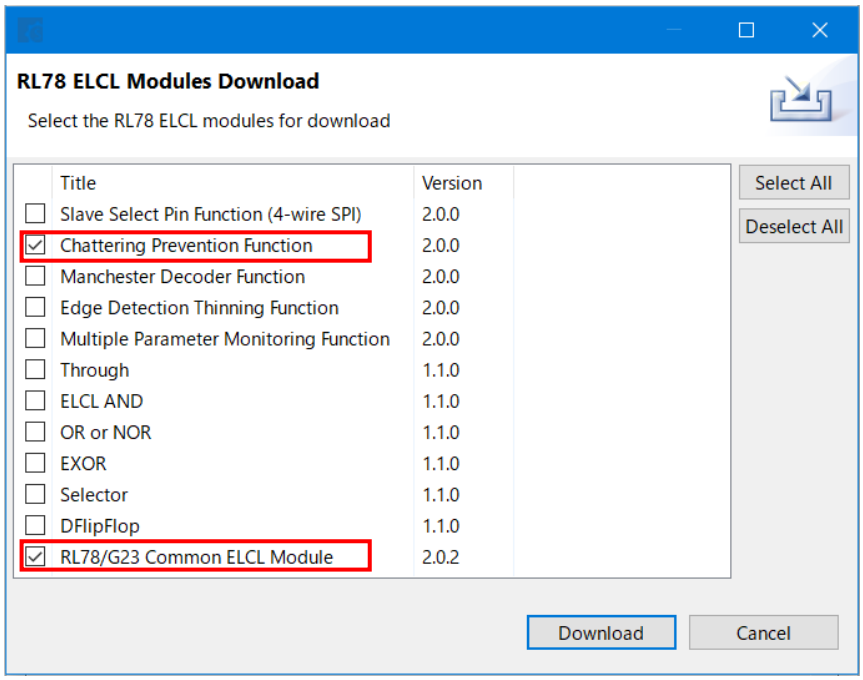
1. Start the Smart Configurator.
2. Click on the "Components" tag, and then click "Add component".
3. When the "New Component" window shown in Figure 5-1 opens, click on "Download ELCL modules".

Figure 5-1 Add component



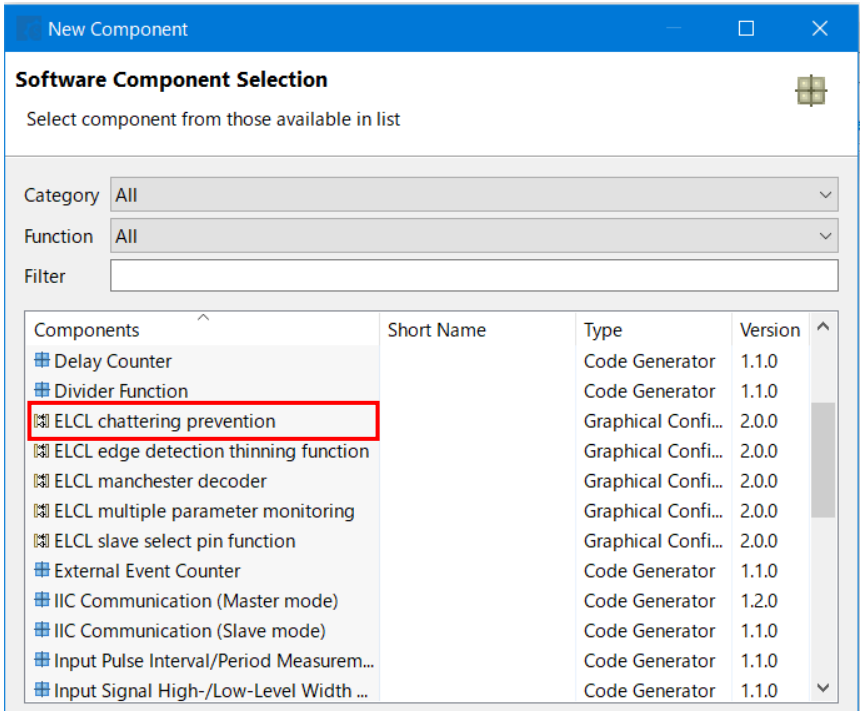
4. Select "Chattering Prevention Function" and download it. Please download the common setting file "RL78/G23 Common ELCL Module" as well.

Figure 5-2 Download the module



5. After the download is complete, make sure that "ELCL chattering prevention" is available for selection.

Figure 5-3 Select the module



5.2 r01an5612_elcl_chattering.scfg

This is the Smart Configurator configuration file used in the sample code. It contains all the features configured in the Smart Configurator. The sample code settings are as follows.

Table 5-1 Parameters of Smart Configurator (1/2)

Tag name	Component	Contents
Clocks	-	Operation mod: High-speed main mode 2.4 (V)~5.5 (V) EV_{DD} setting: 1.8V≦EV_{DD0}＜5.5V High-speed on-chip oscillator: 32MHz f_{IHP}: 32MHz f_{CLK}: 32MHz (High-speed on-chip oscillator) f_{SXP}: 32.768kHz (Low-speed on-chip oscillator)
System	-	On-chip debug operation setting: COM port Note 1 Pseudo-RRM/DMM function setting: Used Start/Stop function setting: Unused Trace function setting: Used Security ID setting: Use security ID Security ID：0x00000000000000000000 Security ID authentication failure setting: Do not erase flash memory data
Components	r_bsp	Start up select : Enable (use BSP startup) Control of invalid memory access detection : Disable RAM guard space (GRAM0-1) : Disabled Guard of control registers of port function (GPORT) : Disabled Guard of registers of interrupt function (GINT) : Disabled Guard of control registers of clock control function, voltage detector, and RAM parity error detection function (GCSC) : Disabled Data flash access control (DFLEN) : Disables Initialization of peripheral functions by Code Generator/Smart Configurator : Enable API functions disable : Enable Parameter check enable : Enable Setting for starting the high-speed on-chip oscillator at the times of release from STOP mode and of transitions to SNOOZE mode : High-speed Enable user warm start callback (PRE) : Unused Enable user warm start callback (POST) : Unused Watchdog Timer refresh enable : Unused
	Config_LVD0	Operation mode setting: Reset mode Voltage detection setting: Reset generation level (V_{LVD0}): 1.86 (V)

Table 5-2 Parameters of Smart Configurator (2/2)

Tag name	Component	Contents
Components	Config_TAU0_0	Components: Delay Counter Resource: TAU0_0 Operation clock: CK00 Clock source: $f_{CLK}/2^5$ Input source setting: ELCL Noise filter: unused External event edge select: Falling edge Delay time: 20 ms Note 2 The start trigger under the count: effect Interrupt setting: unused
	Config_ ChatteringPreventio n	Components: ELCL chattering prevention Input signal selector: P137 Logic block selection: L1 Output signal selector: TAU0 Channel0 Input (L1) Output signal selector: P50

Note 1. When using IAR, use by the following settings.
On-chip debug operation setting: Use emulator
Emulator setting: E2 Emulator Lite
Note 2. Delay is the chattering prevention period.

5.2.1 Clocks

Set the clock used in the sample code.

5.2.2 System

Set the on-chip debug of the sample code.

"Control of on-chip debug operation" and "Security ID authentication failure setting" affect "On-chip debugging is enabled" in "Table 4-2 Option Byte Settings". Note that changing the settings.

5.2.3 r_bsp

Set the startup of the sample code.

5.2.4 Config_LVD0

Set the power management of the sample code.

Affects "Setting of LVD0" in "Table 4-2 Option Byte Settings". Note that changing the settings.

5.2.5 Config_TAU0_0

Initialize the TAU0 of the sample code. In the sample code, it is used in Delay Counter mode. The set value of "Delay time" in the Smart Configurator becomes the chattering prevention period.

5.2.6 Config_ChatteringPrevention

Initialize and output the ELCL of the sample code.

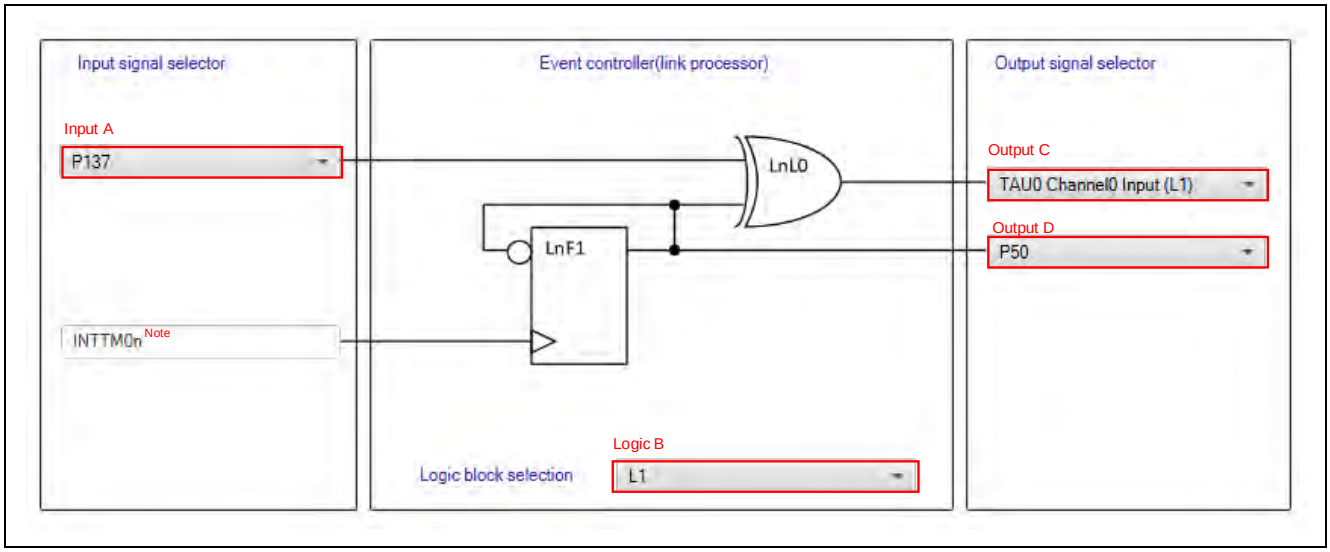
In the sample code, P137 is used as the pin to perform chattering, TAU00 is used to count the chattering prevention period, and P50 is used as the output destination.

See section 5.3 Component "ELCL chattering prevention" for details.

5.3 Component "ELCL chattering prevention"

Figure 5-4 shows the component "ELCL chattering prevention" and Table 5-3 shows the options for this component.

Figure 5-4 Component "ELCL chattering prevention"



Note. The flip-flop input clock is set as follows according to the channel selected in Output C.
For TAU0 Channel0 Input, INTTM00
For TAU0 Channel1 Input, INTTM01
For TAU0 Channel5 Input, INTTM05

Table 5-3 Choices of component "ELCL chattering prevention"

Item	Choices	Description
Input A Note 1	P10	Select pin for chattering
	P11	
	P12	
	P20	
	P50	
	P51	
	P120	
	P137	
Logic B	L1	Select the logical cell block
	L2	
	L3	
Output C	TAU0 Channel0 Input (L1 or L2 or L3) Note2	Select TAU
	TAU0 Channel1 Input (L1 or L2 or L3) Note2	
	TAU0 Channel5 Input (L1 or L2 or L3) Note2	
Output D Note1	P01	Select the output destination
	P10	
	P11	
	P12	
	P13	
	P14	
	P15	
	P16	
	P17	
	P50	
	P51	
	P60	
	P61	
	INTELCL	
	DTC startup trigger	
	SMS startup trigger	
	A/D converter hardware trigger	
	D/A converter0 hardware trigger	
	D/A converter1 hardware trigger	
	CTSU hardware trigger	
	ITL capture trigger	

Note 1. Prohibit to select the same signal for Input A and Output D.

Note 2. Select the signal of Output C according to the logic block set in Logic B.
The flip-flop input signal is selected according to the Output C signal. See the note in Figure 5-4.

5.3.1 Setting the ELCL Register

Table 5-4 to Table 5-6 show the initial settings of the ELCL register in the sample code, and Figure 5-5 to Figure 5-7 show the ELCL configuration at that time. Refer to Figure 4-1 for the overall ELCL configuration.

Table 5-4 ELCL register settings (Inputs)

Register Symbol	Register Name	Setting	Description
ELISEL0	Input signal select register 0	1BH	Input pin P137 is selected
ELISEL1	Input signal select register 1	1DH	Output from flip-flop 1 of logic cell block L1 in the ELCL is selected
ELISEL6	Input signal select register 6	16H	INTTM00 is selected

Figure 5-5 Setting of ELCL input

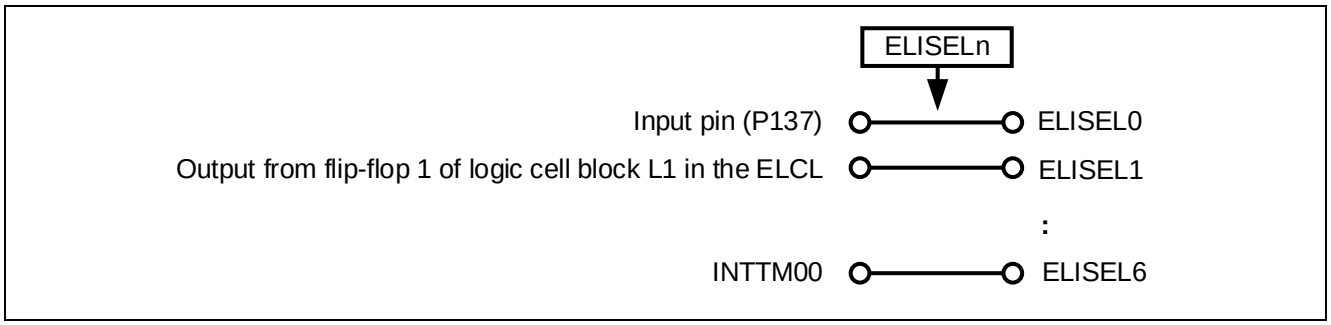


Table 5-5 ELCL register settings (Logic cell block L1)

Register Symbol	Register Name	Setting	Description
ELL1SEL0	Event link L1 signal select register 0	01H	Select the signal selected by ELISEL0 as the link target of L1
ELL1SEL1	Event link L1 signal select register 1	02H	Select the signal selected by ELISEL1 as the link target of L1
ELL1SEL2	Event link L1 signal select register 2	82H	Select the signal selected by ELISEL1 as the link target of L1 (Negative logic)
ELL1SEL6	Event link L1 signal select register 6	01H	Select the signal selected by ELISEL6 as the link target of L1
ELL1LNK0	Event link L1 output select register 0	01H	Link target selected by ELL1SEL0 to input 0 of logic cell 0 in logic cell block L1
ELL1LNK1	Event link L1 output select register 1	02H	Link target selected by ELL1SEL1 to input 1 of logic cell 0 in logic cell block L1
ELL1LNK2	Event link L1 output select register 2	09H	Link target selected by ELL1SEL2 to input of flip-flop 1 in logic cell block L1
ELL1LNK6	Event link L1 output select register 6	02H	Link target selected by ELL1SEL6 to clock of flip-flop 1 in logic cell block L1
ELL1CTL	Logic cell block L1 control register	83H	Enable use of logic cell block L1 flip-flops 1, logic cell 0 selects EX-OR circuit

Figure 5-6 Setting of logic cells L1

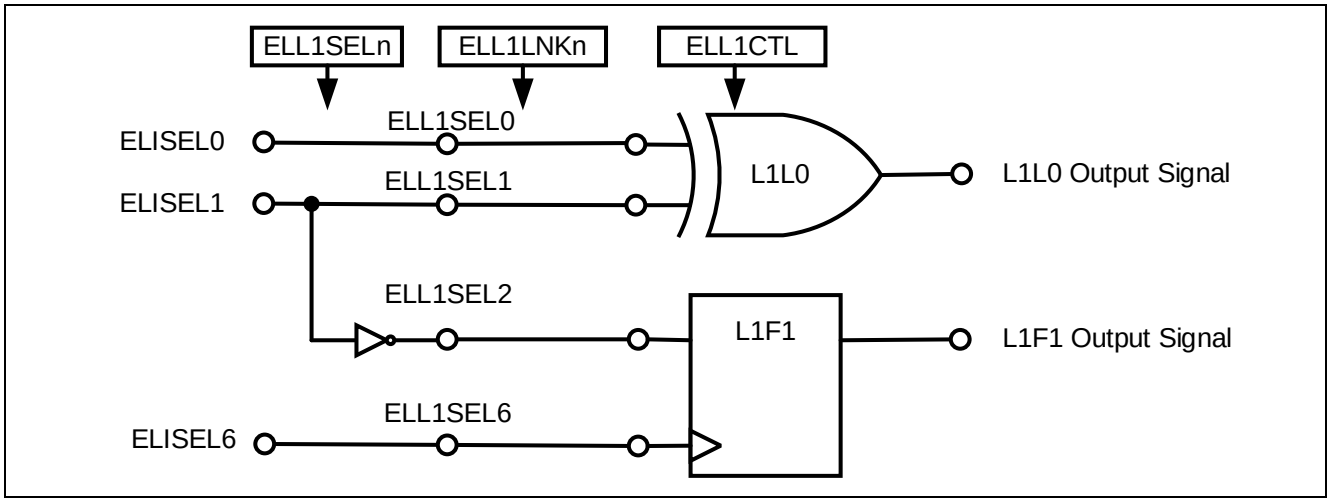
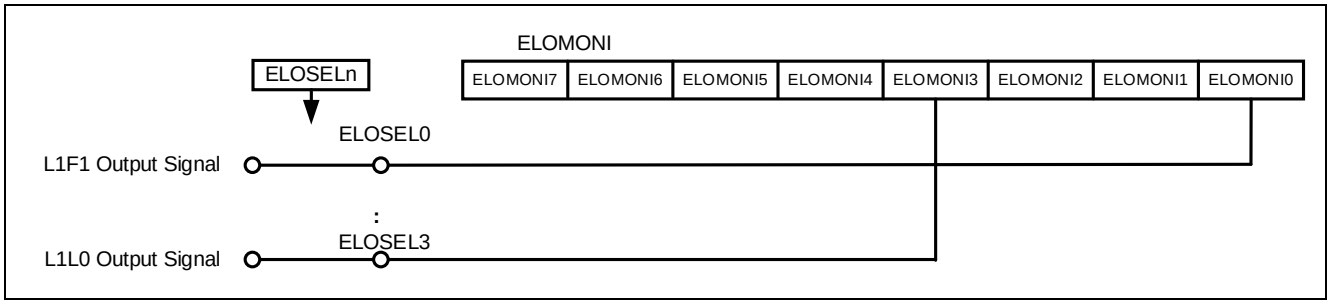


Table 5-6 ELCL register settings (Outputs)

Register Symbol	Register Name	Setting	Description
ELOSEL0	Output signal select register 0	05H	Select the output signal [4] from logic cell block L1.
ELOSEL3	Output signal select register 3	01H	Select the output signal [0] from logic cell block L1.

Figure 5-7 Settings of ELCL output



6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference

RL78/G23 User's Manual: Hardware (R01UH0896E)

RL78 Family User's Manual: Software (R01US0015E)

RL78 Smart Configurator User's Guide: CS+ (R20AN0580E)

RL78 Smart Configurator User's Guide: e^2 studio (R20AN0579E)

RL78 Smart Configurator User's Guide: IAREW (R20AN0581E)

(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update / Technical News

(The latest version can be downloaded from the Renesas Electronics website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Apr.13.21	-	First edition
2.00	Mar.24.22	5	Table 2-1 Operation Confirmation Conditions Operating voltage Rising edge TYP.1.875V -> 1.90V Falling edge TYP.1.835V -> 1.86V
		5	Updated tool version Table 2-1 Operation Confirmation Conditions Integrated development environment (CS+) : E8.05.00f -> V8.07.00 C compiler (CS+) : V1.09.00 -> V1.11 Integrated development environment (e^2 studio) : 2021-01 (21.01.0) -> 2022-01 (22.1.0) C compiler (e^2 studio) : V1.09.00 -> V1.11 Integrated development environment (IAR) : V4.20.1 -> V4.21.1 Smart Configurator : V.1.0.0 -> V.1.2.0 Board support package (r_bsp) : V.1.0.0 -> V.1.13
		5, 6 14, 15	Changed due to COM port support Table 2-1 Operation Confirmation Conditions Emulator: E2 Emulator Lite -> CS＋, e^2 studio: COM port IAR: E2 Emulator Lite Figure 3-1 Hardware Configuration Added P11/TOOLRxD and P12/TOOLTxD Table 5-1 Parameters of Smart Configurator (1/2) Note 1 added
		8	Updated the folder structure in Table 4-1 due to the sample program update Added Note 3 due to the update of the IAR version sample code.
		9	Table 4-2 Option byte setting Detection voltage Rise 1.875V / Fall 1.835V -> Rise 1.90V / Fall 1.86V
		10	Changed the header file due to the IAR version sample code update 4.7 Function Specifications [function name] main, header e^2 studio, CS +: r_smc_entry.h IAR: ior7f100g.h, ior7f100g_ext.h, r_cg_macrodriver.h, Config_SMS.h, Config_ITL000_ITL001.h -> r_smc_entry.h

Rev.	Date	Description	
		Page	Summary
2.00	Mar.24.22	11, 12-13,17	Updated some figures as follows due to the component "ELCL chattering prevention" update. Figure 4-3 Main process Function name: R_Config_ButtonDebounce_Create () -> R_Config_ChatteringPrevention_Start () Figure 5-1 Add components Figure 5-2 Download the module Figure 5-3 Select the module Figure 5-4 Component "ELCL chattering prevention" Figure update
		13, 15-18	Updated the spelling of the component names to the latest. ELCL Chattering Prevention -> ELCL chattering prevention
		14	Table 5-1 Parameters of Smart Configurator(1/2) Clock: f_{SXL} -> f_{SXP} Component Config_LVD0 Reset generation voltage (V_{LVD0}): 1.835 (V) -> 1.86 (V)
		15	Table 5-2 Parameters of Smart Configurator(2/2) Component Config_ChatteringPrevention Input signal selector: P137 / INTP0 -> P137 Logic block selection: Logic block 1 -> L1 Output signal selector: TAU0 Channel0 Input -> TAU0 Channel0 Input (L1)
		15-16	Deleted unused components with the update of the component "ELCL chattering prevention" Delete Table 5-2 Parameters of Smart Configurator(2/2) Component Config_PORT 5.2.7 Config_PORT
		17	Added the note of Figure 5-4 with the update of the component "ELCL chattering prevention"
		18	Updated/Added the contents and note in Table5-3 with the component "ELCL chattering prevention" update. Table 5-3 Choices for component "ELCL chattering prevention" Added Input A, Logic B, Output C, Output D choices Note1,Note2
		22	Added of RL78 Smart Configurator User's Guide 7. Reference RL78 Smart Configurator User's Guide: CS+ (R20AN0580E) RL78 Smart Configurator User's Guide: e² studio (R20AN0579E) RL78 Smart Configurator User's Guide: IAREW (R20AN0581E)
2.10	Sep.18.24	4	Changed chattering prevention control outline and timing chart
		5	Update Table 2-1 Operation Confirmation Conditions
		7	Change the delay time in “Figure 4 2 Timing chart of the sample code
		8	Remove the comments from Config_TAU0_0.c
		15	Change the setting of Config_TAU0_0

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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