R9A02G011

RTK-251-DRPEVB Instruction Manual

Introduction

The RTK-251-DRPEVB is an evaluation board for USB Power Delivery (USB PD). The RTK-251-DRPEVB has a USB PD 3.0 controller R9A02G011, Authentication microprocessor (MCU), and Bi-directional Buck-Boost Voltage Regulator (BB-VR) ISL95338. This document is the instruction manual for RTK-251-DRPEVB.

The RTK-251-DRPEVB supports USB PD 3.0 ver.2.0 functions, PDFU and USB Type-C™ authentication (RTK0EUG011D08010BJ only). The USB Type-C™ receptacle is connected to the adapter side of the BB-VR, and a 19V DC adapter is connected to the system side of the BB-VR. As a USB Type-C™ power source, the RTK-251-DRPEVB outputs up to 20V and 3A for USB Type-C™ VBUS. As a USB Type-C™ power sink, the RTK-251-DRPEVB receives power from VBUS and generates 17V on a system side test point.

The RTK-251-DRPEVB has various I/O test points, one switch and one LED. The user can develop the software to access these I/O by using a Software Development Kit (SDK).

The RTK-251-DRPEVB has a USB micro controller RL78/G1C which is connected to SMBus of the PDC.

The PDC on this board can be controlled from PC via the micro controller, so a device connected to Type-C™ interface can be communicated from PC.

Target Device

USB PD with USB Type-C™ Authentication evaluation board: RTK-251-DRPEVB

USB Power Delivery Controller: R9A02G011

Bi-directional Buck-Boost Voltage Regulator (BB-VR): ISL95338 or RAA489800 Note

Authentication microprocessor: R5H30313XB08

Ordering Information

RTK0EUG011D08000BJ (R5H30313XB08 is not mounted)

RTK0EUG011D08010BJ (R5H30313XB08 is mounted: for PDFU, USB Type-C™ Authentication)

[Note] RAA489800 is a successor product to ISL95338, and user can update the RTK-251-DRPEVB board to the RAA489800 version by some minor changes. Please refer to Section 3.2 for the update method.

Related Document

Use this document in combination with the following documents.

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

- R9A02G011 Data Sheet: R19DS0088EJ
- R9A02G011 User's Manual: R19UH0102EJ
- R9A02G011/R9J02G012 Application Note Flash Memory Programming Guide: R19AN0060EJ
- E1 Emulator E20 Emulator User's Manual: R20UT0398EJ
- E2 Emulator Lite User's Manual: R20UT3240EJ
- E1/E20 Emulator, E2 Emulator Lite Additional Document for User's Manual (Notes on Connection of RL78): R20UT1994EJ
- Renesas Flash Programmer V3.05 Flash memory programming software User's Manual: R20UT4307EJ
- USB Power Delivery Controller Application Note SDK (Software Design Kit): BCD-ISG-21-5004
- USB Power Delivery Controller Application Note SDK (Software Design Kit) for Evaluation Board: BCD-ISG-21-5001
- USB Power Delivery Controller Flash memory image data generator software (PDC-IMGGEN)
- Application Note: BCD-ISG-19-5015
- R5H30313XB08 Data sheet: R01DS0314EJ
- Renesas USB PD Exerciser User's Manual: BCD-IMB-19-5017
- R9A02G011/R9J02G012 Firmware development guide for USB Type-C™ Authentication: R19AN0061EJ
- ISL9241 DATASHEET: FN8945
- ISL9241EVAL1Z USER'S MANUAL: UG184
- ISL95338 DATASHEET: FN8896
- RAA489800 DATASHEET: FN9319

Contents

1. Features

RTK-251-DRPEVB supports the following features.

- USB Power Delivery and USB Type-C™
  - Supports USB Power Delivery 3.0 ver.2.0
  - Having one USB Type-C™ port
  - Power Role: Dual Role Power (DRP)
    - Power Source voltage: 5, 9, 15, 20V and other voltages up to 20V
    - Power Sink voltage: 5 to 20V
  - Supports Programmable Power Supply (PPS) function
    - Up to 5VProg supported (3.3V to 5.9V VBUS power supply, additional voltage options are under evaluation)
  - Supports USB Type-C™ Authentication (C-Auth) feature
  - Supports USB Power Delivery Firmware Update feature (PDFU)

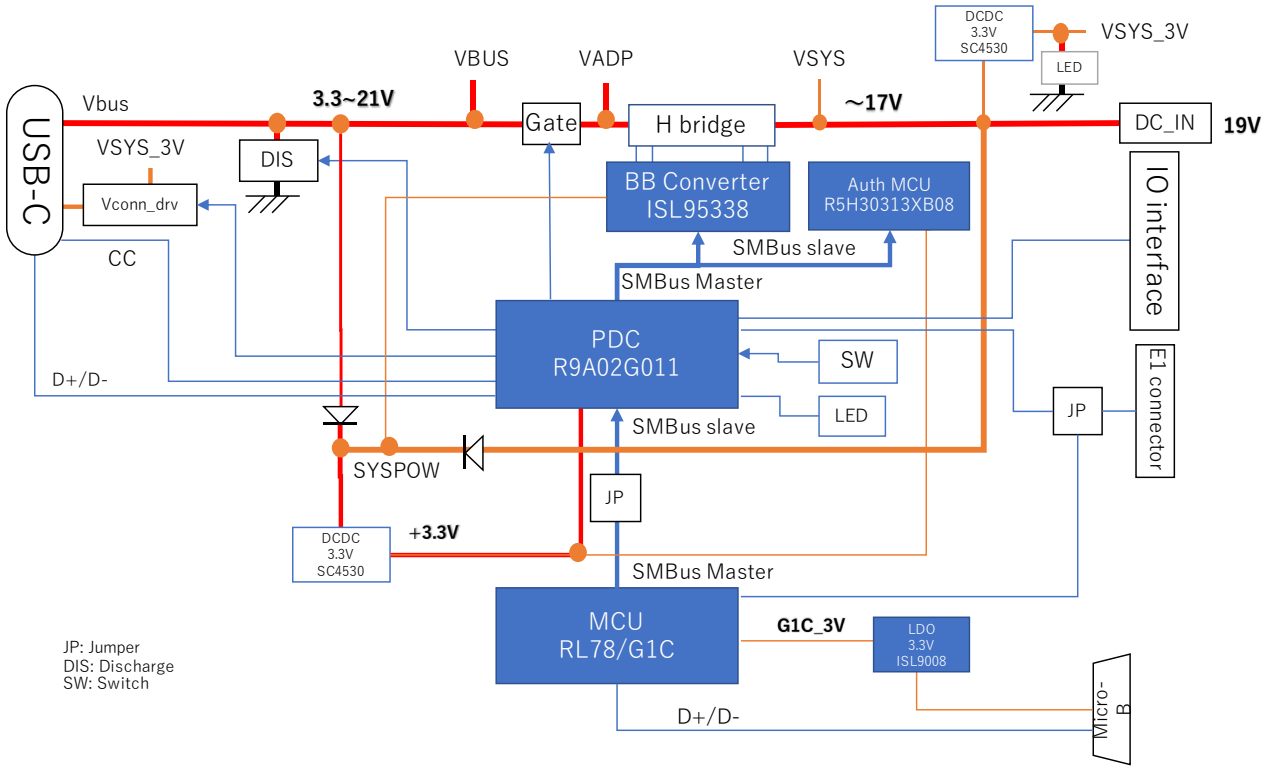
- Interface
  - LED indicators
    - System power indicator (1 LED, orange)
    - Indicator for R9A02G011 (1 LED, blue)
  - Switch
    - An external interrupt input to R9A02G011
  - On-chip debugging emulator interface
    - Renesas on-chip debugging emulator interface to write and debug firmware for R9A02G011 and RL78/G1C
  - USB Micro-B port
    - Exerciser interface for PC
    - USB Micro-B is connected to RL78/G1C
    - USB Micro-B provides power to RL78/G1C
  - GPIO
    - SMBus master/slave interface of R9A02G011
    - R9A02G011 GPIOs

- Protections
  - Over Temperature Protection on the USB Type-C™ Receptacle
  - R9A02G011 monitors VBUS voltage level for Over Voltage and Over Current Protection

- Mode Options
  - USB PD Exerciser mode
  - FW Update mode

1.1 Block Diagram

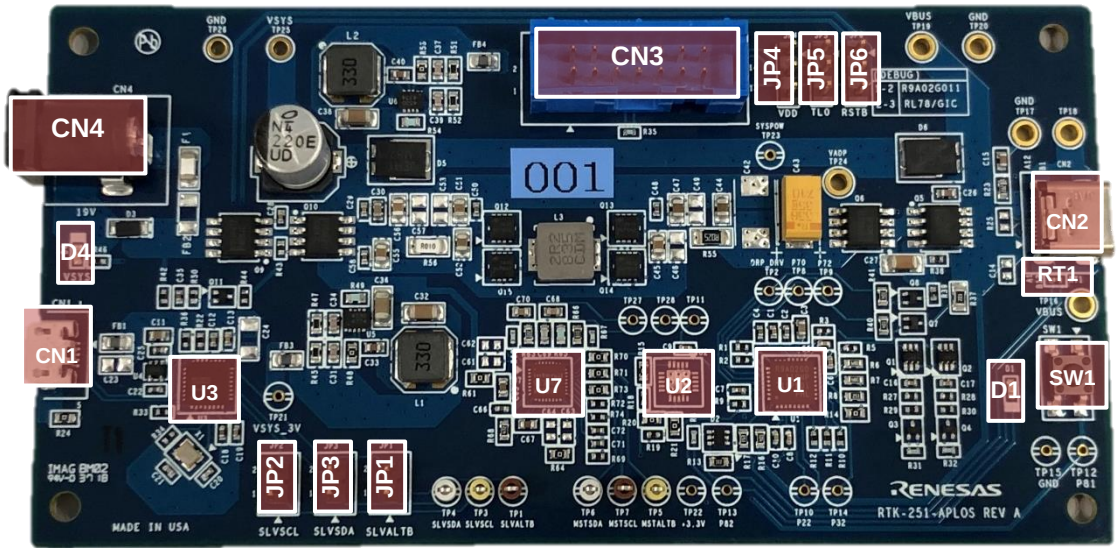
Figure 1-1 RTK-251-DRPEVB block diagram



1.2 Component

1.2.1 Component layout

Figure 1-2 Highlighted mainly parts on the board



1.2.2 Component information

(1) IC

No.	Description	Remark
U1	R9A02G011 (PDC)	-
U7	ISL95338 (BB-VR)	Can replace with RAA489800 Refer to section 3.2
U3	R5F10KBCANA (RL78/G1C)	-
U2	R5H30313XB08 (Authentication MCU)	RTK0EUG011D08010BJ only

(2) Connector

No.	Description	Remark
CN4	DC Jack for power input from AC adapter	-
CN2	USB Type-C™ receptacle	-
CN1	USB Micro-B receptacle	-
CN3	Renesas on-chip debugging emulator interface	-

(3) Switch

No.	Description	Port connection of the PDC
SW1	Tactile switch	P81: Pin30 (“L”: pushed)

(4) LED

No.	Description	Port connection of the PDC
D4	VSYS power indicator (Orange)	-
D1	General purpose indicator (Blue)	P82: Pin31 (“L”: light)

(5) Thermistor

No.	Description	Port connection of the PDC
RT1	Thermistor for the PORT1	P21: Pin3

(6) Jumper

No.	Description	Port connection of the PDC
JP1	SMBus Slave Alert signal connection jumper between PDC and RL78/G1C	P62: Pin10
JP2	SMBus Slave Clock signal connection jumper between PDC and RL78/G1C	P60: Pin9
JP3	SMBus Slave Data signal connection jumper between PDC and RL78/G1C	P61: Pin8
JP4	VDD selection jumper for CN3 1-2: R9A02G011, 2-3: RL78/G1C	-
JP5	TOOL0 signal selection jumper for CN3 1-2: R9A02G011, 2-3: RL78/G1C	P40: Pin7
JP6	RESETB signal selection jumper for CN3 1-2: R9A02G011, 2-3: RL78/G1C	-

(7) Test point

No.	Description	Port connection of the PDC
TP1	SMBus Slave alert on R9A02G011	P62: Pin10
TP2	GATE on VBUS control pin	P73: Pin29
TP3	SMBus Slave SCL on R9A02G011	P60: Pin9
TP4	SMBus Slave SDA on R9A02G011	P61: Pin8
TP5	SMBus Master alert on R9A02G011 (SMBus Slave alert on BB-VR)	P137: Pin24
TP6	SMBus Master SDA on R9A02G011 (SMBus Slave SDA on BB-VR)	P31: Pin5
TP7	SMBus Master SCL on R9A02G011 (SMBus Slave SCL on BB-VR)	P30: Pin6
TP8	P70 on R9A02G011	P70: Pin26
TP9	P72 on R9A02G011	P72: Pin28
TP10	P22 on R9A02G011	P22: Pin4
TP11	VCC on Auth MCU	-
TP12	P81 on R9A02G011	P81: Pin30
TP13	P82 on R9A02G011	P82: Pin31
TP14	P32 on R9A02G011	P32: Pin11
TP15	GND	-
TP16	cVBUS (Near USB Type-C™ receptacle)	-
TP17	GND (to measure VBUS return current)	-
TP18	GND (to measure VBUS return current)	-
TP19	cVBUS	-
TP20	GND	-
TP21	VSYS_3V	-
TP22	+3.3V	-
TP23	SYSPOW	-
TP24	VADP	-
TP25	VSYS	-
TP26	GND	-
TP27	COMPR on BB-VR	-
TP28	COMPF on BB-VR	-

2. Available Configurations

A fixed configuration data is programmed in the R9A02G011 on the RTK-251-DRPEVB when the board is shipped out. The configuration can be changed if the data is updated by using configuration changed options.

The detail explanation of the configuration changed options is described in Chapter 4, 5 and 6 **Note**.

[Note] Chapter 4,5 and 6 are described in the full version of this manual.

It is restricted access, and please contact Renesas sales person or distributer if necessary.

If you change the “Shipped out configuration”, it is necessary to generate a flash memory data of “Mode dedicated Configuration”, “SDK Configuration” or “Standard Configuration”, then program the data to the PDC on the board.

Fig 2-1 Configuration for the RTK-251-DRPEVB

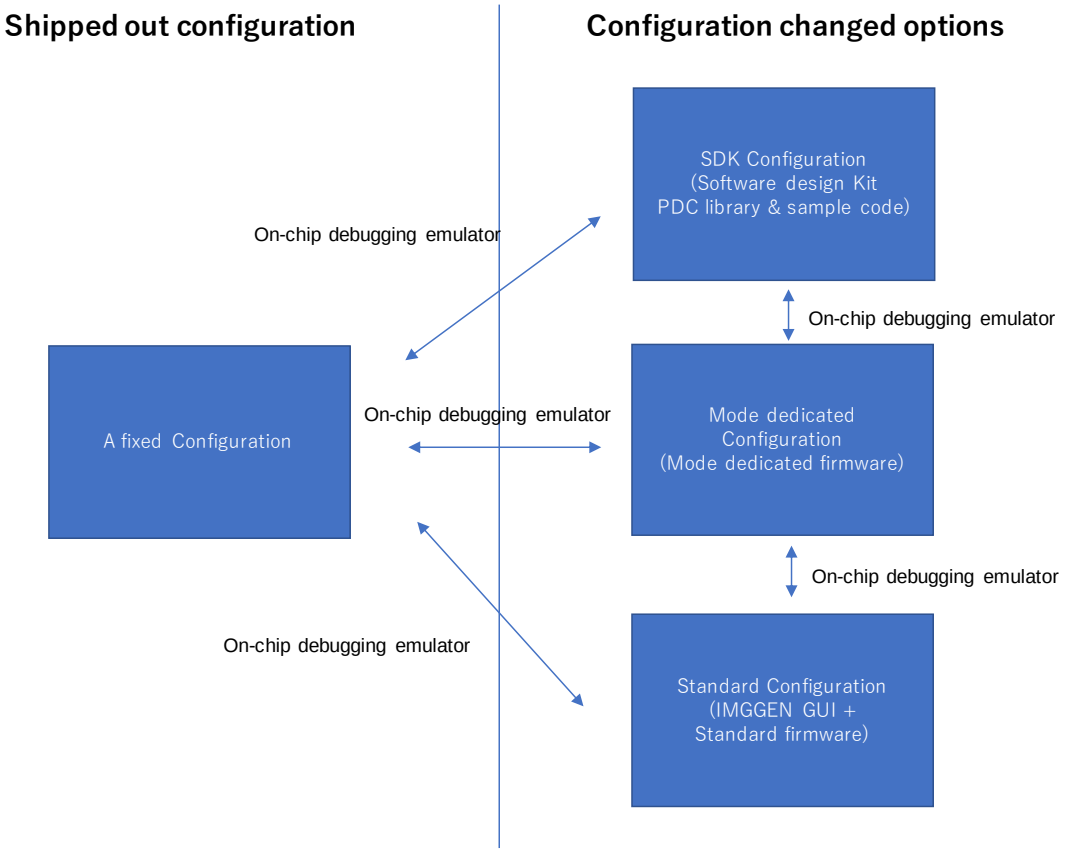


Table 2-1 Configuration list for the RTK-251-DRPEVB

Features	RTK0EUG011 D08000BJ	RTK0EUG011 D08010BJ	Availability of FW	Existing EVB Note2	Reference section #
Generic DRP	O	N/A	Shipped out configuration	RTK-252-Dual	2.1
	▽	▽	User customizing by SDK or IMGGEN		2.1, 6.1
Generic DRP with C-Auth	N/A	▽Note1	User customizing by SDK or IMGGEN	ET-D720251-1006	2.1
Source only with C-Auth	N/A	O	Shipped out configuration	ET-D720251-1004-B	2.1
USB PD Exerciser Mode	◇	◇	Exerciser's mode operation	-	4.1
FW Update Mode	◇	◇	FW Update mode operation	ET-D720251-0005	4.2
Sink only (Bus powered Sink)	▽	▽	User customizing by SDK or IMGGEN	ET-D720251-0006 ET-D720251-1006	5.1, 6.2
Billboard emulation	☐	☐	User customized by SDK	-	5.2

O: Fixed configuration

◇: Mode dedicated configuration

▽: Standard configuration or SDK configuration

☐: SDK configuration

Note1: C-Auth initiator feature, responder feature and cable authentication be available by SDK or PDC-IMGGEN customizing

Note2: User can replace these existing evaluation board with RTK-251-DRPEVB to realize the feature.

The Mode dedicated configuration data, SDK, PDC-IMGGEN and standard firmware can be download from Renesas-web. It is restricted access, and please contact Renesas sales person or distributer if necessary.

2.1 Shipped out configurations

The RTK0EUG011D08000BJ and RTK0EUG011D08010BJ are programmed as following configuration, when they are shipped out. The RTK-251-DRPEVB can be used as the software developing board instead of the RTK-252-DUAL.

RTK0EUG011D08000BJ	RTK0EUG011D08010BJ
Power Role: Dual Role 65W Power Source (5, 9, 15, 20V) 60W Power Sink (5, 9, 12, 15, 20V) Supports BC1.2 DCP Supports D1 LED (Light: Source operation, Blink: Sink operation)	Power Role: Source Only 60W Power Source (5, 9, 15, 20V) Supports BC1.2 DCP Supports D1 LED (Light: Source operation) PDFU support USB Type-C™ Authentication Responder

Table 1-2 Pin assignment of shipped out configuration of the R9A02G011

Pin No.	Pin	Name	Descriptions
1	P16	VCONN_DRV1	Load SW for Vconn
2	P20	VBUSM	VBUS voltage monitor input
3	P21	OTP	Thermistor next to USB Type-C™ Receptacle
4	P22	Open	－（Refer to BB-VR registers for OCP）
5	P31	MSTSDA	SMBus master data input/output (open-drain) Connected to Auth MCU / BB-VR
6	P30	MSTSCL	SMBus master clock input/output (open-drain) Connected to Auth MCU / BB-VR
7	P40	TOOL0	Connected to E1 connector
8	P61	SLVSDA	SMBus slave data input/output (open-drain) Connected to RL78G1C
9	P60	SLVSCL	SMBus slave clock input/output (open-drain) Connected to RL78G1C
10	P62	SLVSALTB	SMBus slave alert output (open-drain). Connected to RL78G1C
11	P32	AUTH_RESB	Reset signal to Auth MCU
12	P80	PUE	USB Type-C™ pull-up enable by 1.5kohm5%
13	P50	DM	USB Type-C™ D- pin connection, 68ohm damping resistor
14	P51	DP	USB Type-C™ D+ pin connection, 68ohm damping resistor
15	RD1	RD1	Rd resistor 1, Analog pin from CC-PHY.
16	CC1	CC1	Configuration Channel 1, Analog pin from CC-PHY
17	CC2	CC2	Configuration Channel 2, Analog pin from CC-PHY
18	RD2	RD2	Rd resistor 2, Analog pin from CC-PHY.
19	REG	REGCTX	Regulator capacitance for CC-PHY. Connecting regulator output stabilization capacitance for internal operation.
20	VDD	VDD	Power supply (from 3.0V to 5.5V)
21	REGC	REGC	Regulator capacitance. Connecting regulator output stabilization capacitance for internal operation.
22	P121	SLVADDR0	SMBus slave address bit [1] (Pulled-up)
23	P122	SLVADDR1	SMBus slave address bit [2] (Pulled-up)
24	P137	MSTALTB	PROCHOT# signal from BB-VR
25	RESETB	RESETB	Chip Reset Input (active low)
26	P70	Open	-
27	P71	DISCHG	Discharge control for USB Type-C™ VBUS
28	P72	Open	-
29	P73	AGATE	Gate for VBUS and BB-VR Vadp
30	P81	sw_in	Switch input (Active Low)
31	P82	LED_CTRL	LED control (Open Drain)
32	P17	VCONN_DRV2	Load SW for Vconn

2.2 Configuration option changes

Renesas provide following three kind data of the “Configuration option changes”.

- Mode dedicated configuration
- SDK configuration
- Standard configuration

The data can be download from Renesas-web. It is restricted access, and please contact Renesas sales person or distributer if necessary.

2.2.1 Mode dedicated configuration

Renesas provide two dedicated configuration data to realize the “USB PD Exerciser Mode” and the “FW Update Mode”.
The detail explanation of the configuration changed options is described in Chapter 4.

[Note] Chapter 4 is described in the full version of this manual.

It is restricted access, and please contact Renesas sales person or distributer if necessary.

2.2.2 SDK configuration

The “SDK Configuration” is a data which is generated by PDC Software Design Kit (SDK) with Integrated Design Environment (IDE: Renesas CS+, IAR Embedded Workbench for RL78, etc.).

The SDK has PDC library, several sample codes and setup files for IDE (Renesas CS+ and IAR Embedded Workbench), so user can realize several functions.
You can realize the “Billboard Emulation” by using SDK.
The detail explanation of the configuration changed options is described in Chapter 5.

[Note] Chapter 5 is described in the full version of this manual.

It is restricted access, and please contact Renesas sales person or distributer if necessary.

2.2.3 Standard configuration

The “Standard Configuration” is a data which is generated by Renesas “PDC-IMGGEN” and a standard firmware.
The “Generic DRP” and “Sink only” modes can be setup by above environment easily.
The detail explanation of the configuration changed options is described in Chapter 6.

[Note] Chapter 6 is described in the full version of this manual.

It is restricted access, and please contact Renesas sales person or distributer if necessary.

3. Board setup and how to use

3.1 Required materials to use this board.

- RTK-251-DRPEVB: 1 unit
- 19V AC Adapter (mating plug is Φ5.5 mm x 2.5 mm, center +. Depth is 8.85mm): 1 unit
- USB Type-C™ Cable: 1pcs

Notes:
Please use this board when you understand and agree that Renesas DOES NOT have any responsibility, indemnification, or liability for use of this board.
Renesas uses 19V/4.7A AC adapter for evaluation for this board.
VBUS output power should be limited within AC adapter power budget. For example, if AC adapter power budget is 90W, VBUS power for two ports and system power should be within 90W. System power is less than about 150mW (0.15W).

1. Connect AC Adapter to DC jack (CN4) and supply power to the board, confirm orange LED (D4) light.
2. Connect a device to USB Type-C™ receptacle (CN2) via USB cable. The board supplies power to device by a result of communication between the board and device.

The RTK-251-DRPEVB operates as sink device if it is connected to source capable device on CN2 without powered from CN4.

3.2 How to update from ISL95338 version to RAA489800 version

This section describes how to update from ISL95338 version to RAA489800 version for both hardware and software.

3.2.1 Hardware Setting

Following change is necessary on RTK0EUG011D08000BJ or RTK0EUG011D08010BJ.

(1) Replace ISL95338 with RAA489800.

Following capacitors and resistors changes are recommended.

(2) Change C69 from 1nF to 10nF (BB-VR REF pin capacitance).

* Mounting with Pb-free solder is recommended for all.

3.2.2 Software Setting

The R9A02G011 firmware needs to be updated for RAA489800. Please refer to Chapter 5 and 6 [Note] for details.

[Note] Chapter 4, 5 and 6 are described in the full version of this manual.

It is restricted access, and please contact Renesas sales person or distributer if necessary.

4. Configuration option changes for Mode Dedicated configuration

Renesas provide two dedicated configuration data to realize the “USB PD Exerciser Mode” and the “FW Update Mode”. These modes are available if dedicated flash memory data are programmed to flash memory in the R9A02G011 and RL78/G1C on the RTK-251-DRPEVB.

4.1 USB PD Exerciser Mode

The “USB PD Exerciser Mode” is used to evaluate a device connected to the CN2. The RTK-251-DRPEVB can be controlled from a PC via CN1 through the RL78/G1C on the board.

The detail information is described in Renesas USB PD Exerciser User’s Manual: BCD-IMB-19-5017. Refer to the document.

4.2 FW Update Mode

The “FW Update Mode” is used to update a flash memory data in the R9A02G011 on a device connected to the CN2. The RTK-251-DRPEVB can be controlled from a PC via CN1 through the RL78/G1C on the board.

The detail information is described in Renesas USB PD Exerciser User’s Manual: BCD-IMB-19-5017. Refer to the document.

5. Configuration option changes for SDK configuration

This board can be used for evaluating several Power Delivery devices (Sink-only, Source-only, DRP, etc) by programming original flash memory data generated by using SDK.

Four examples are described in this chapter.

5.1 Sink only (Bus-powered Sink) device

The RTK0EUG011D08000BJ can be used as the Sink-only (Bus-powered) evaluation board instead of the ET-D720251-0006.

The RTK0EUG011D08010BJ can be used as the Sink-only (Bus-powered) evaluation board instead of the ET-D720251-0006 and ET-D720251-1006.

It is necessary to modify the board to operate as Sink-only (Bus-powered) evaluation board, then flash memory data which is made as “Sink-only device” by SDK should be programmed in the PDC on this board.

5.1.1 Board modification

Following two modifications are needed to realize the BUS-powered Sink usage.

1) Remove FB3
2) Connect +3.3V and VSYS_3V together.

Refer to Figure 5-1.

Figure 5-1 Board fix points

5.1.2 Making flash memory data

The SDK includes a sample code for this board. Modify it for your configuration then program it to the board.

The detail information is described in following documents. Refer to the documents.

- USB Power Delivery Controller Application Note SDK (Software Design Kit): BCD-ISG-21-5004
- USB Power Delivery Controller Application Note SDK (Software Design Kit) for Evaluation board: BCD-ISG-21-5001

5.2 Billboard Class emulation device

The RTK-251-DRPEVB mounts some materials to realize the “Billboard Class” emulation.

User can evaluate the “Billboard Class” by using this board, if modify this board and develop firmware to simulate the “Billboard Class” function.

5.2.1 Board modification

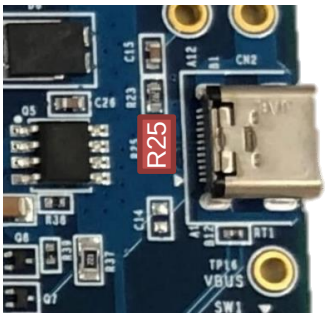
Following two modifications are needed. The modification realizes connecting D+ / D- of the CN2 to P51 / P50 of the R9A02G011 on this board.

1) Remove R25 resistor
2) Install resistors R6, R7, and R8

1) Remove R25

R25 is a resistor to short DP/DM for DCP.

Figure 5-2 R25



2) Install resistors R6, R7, and R8

User should install 68ohm (type 1608) resisters for R6 and R7, and 1.5kohm (type 1608) for R8 to connect DP/DM to the R9A02G011.

Figure 5-3 part of schematic around pins for DP/DM on R9A02G011

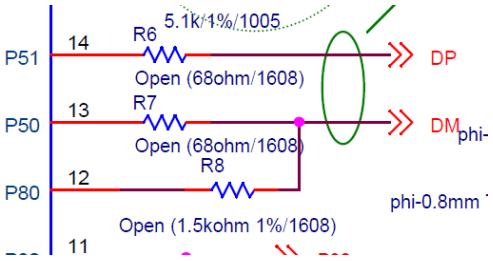
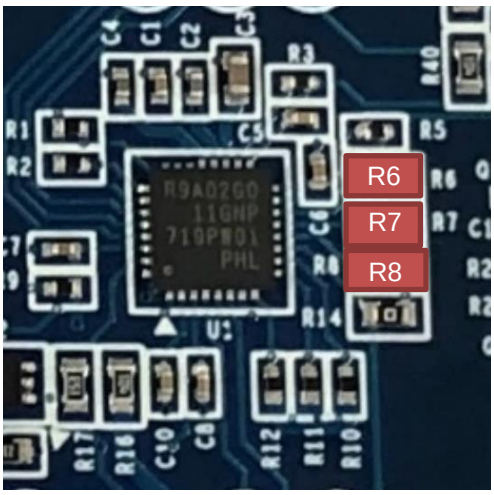


Figure 5-4 Board picture around R6, R7, and R8



5.2.2 Making flash memory data

The “Billboard Class” emulation device can be realized if you develop firmware which operate as USB Billboard Class device (Low-speed) by controlling D+/D- line by P51 / P50.

5.3 Evaluating another voltage regulator

The RTK-251-DRPEVB can be used for evaluating another voltage regulator controlled by SMBus.

Following examples is described for evaluating ISL9241 instead of the ISL95338 (BB-VR).

Remark)

The flash memory data should be updated to control the ISL9241 instead of the ISL95338 (BB-VR).

The specification and usage of the ISL9241 are described in related documents. Refer to the documents.

Figure 5-5 Connection example of RTK-251-DRPEVB and ISL9241

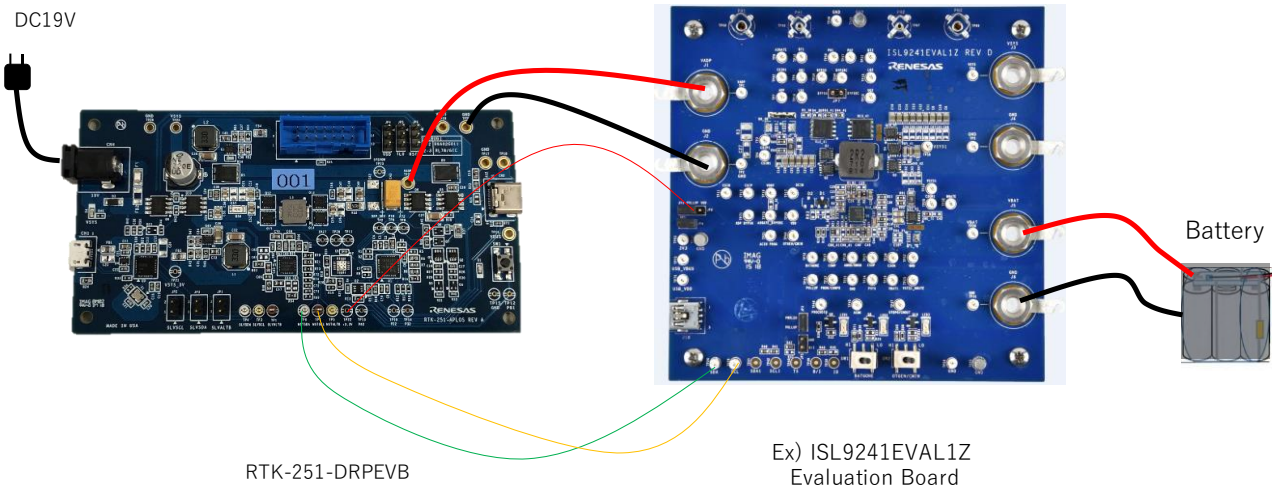


Table 5-1 Signal connection between RTK-251-DRPEVB and ISL9241EVAL1Z

RTK-251-DRPEVB	ISL9241EVAL1Z	Note
VADP (TP24)	VADP (TP1)	
GND (TP20)	GND (TP2)	
3.3V (TP22)	PULLUP (JP6-center pin)	The jumper plug of the JP6 on the ISL9241EVAL1Z should be removed
ISL_SCL (TP7)	SCL (TP26)	
ISL_SDA (TP6)	SDA (TP24)	

Table 5-2 RTK-251-DRPEVB setting

CN, JP, TP	Connection	Note
CN4: 19V	Connect to 19V AC Adapter	
JP1: SLVALTB	Open (no connection)	
JP2: SLVSCL	Open (no connection)	
JP3: SLVSDA	Open (no connection)	
JP4: VDD	1-2 short	
JP5: TL0	1-2 short	
JP6: RSTB	1-2 short	
TP24: VADP	Connect to TP1 of the ISL9241EVAL1Z	
TP20: GND	Connect to TP2 of the ISL9241EVAL1Z	
TP6: MSTSDA	Connect to TP24 of the ISL9241EVAL1Z	
TP7: MSTSCL	Connect to TP26 of the ISL9241EVAL1Z	
TP22: +3.3V	Connect to center of the JP6 of the ISL9241EVAL1Z	

Table 5-3 ISL9241EVAL1Z setting

J, SW, JP	Connection	Note
J1: ADP	Connect to TP24 of the RTK-251-DRPEVB	
J2: GND	Connect to TP20 of the RTK-251-DRPEVB	
J3: VSYS	Open (no connection)	
J4: GND	Open (no connection)	
J5: VBAT	Connect to Battery (+)	
J6: GND	Connect to Battery (-)	
SW1: BATGONE	Set to “LO”	
SW2: OTGEN	Set to “HI”	
JP3	Open (no connection)	
JP4	Open (no connection)	
JP5	Open (no connection)	
JP6	Open except for clip wire to DRPEVB (TP22 of the RTK-251-DRPEVB)	
JP7	Open (no connection)	

Table 5-4 Pin assignment of R9A02G011 for ISL9241EVAL1Z

Pin No.	Pin	Name	Descriptions
1	P16	VCONN_DRV1	Load SW for Vconn
2	P20	VBUSM	VBUS voltage monitor input
3	P21	OTP	Thermistor next to USB Type-C™ Receptacle
4	P22	Open	－（Refer to BB-VR registers for OCP）
5	P31	MSTSDA	SMBus master data input/output (open-drain) Connected to Auth MCU / ISL9241
6	P30	MSTSCL	SMBus master clock input/output (open-drain) Connected to Auth MCU / ISL9241
7	P40	TOOL0	Connected to E1 connector
8	P61	Open	No connection
9	P60	Open	No connection
10	P62	Open	No connection
11	P32	AUTH_RESB	Reset signal to Auth MCU. Optional
12	P80	Open	No connection
13	P50	Open	No connection
14	P51	Open	No connection
15	RD1	RD1	Rd resistor 1, Analog pin from CC-PHY.
16	CC1	CC1	Configuration Channel 1, Analog pin from CC-PHY
17	CC2	CC2	Configuration Channel 2, Analog pin from CC-PHY
18	RD2	RD2	Rd resistor 2, Analog pin from CC-PHY.
19	REG	REGCTX	Regulator capacitance for CC-PHY. Connecting regulator output stabilization capacitance for internal operation.
20	VDD	VDD	Power supply (from 3.0V to 5.5V)
21	REGC	REGC	Regulator capacitance. Connecting regulator output stabilization capacitance for internal operation.
22	P121	SLVADDR0	Pulled-up
23	P122	SLVADDR1	Pulled-up
24	P137	MSTALTB	PROCHOT# signal from BB-Charger. Optional
25	RESETB	RESETB	Chip Reset Input (active low)
26	P70	Open	No connection
27	P71	DISCHG	Discharge control for USB Type-C™ VBUS
28	P72	Open	No connection
29	P73	DR_GATE	Gate for VBUS and ISL9241 Vadp
30	P81	sw_in	Switch input (Active Low), Optional
31	P82	LED_CTRL	LED control (Open Drain), Optional
32	P17	VCONN_DRV2	Load SW for Vconn

5.4 Evaluating multi-source device

The RTK-251-DRPEVB can be used for evaluating multi-source device.

Following examples is described for evaluating multi-source device which has three ports.

The RL78/G1C of the RTK-251-DRPEVB for Port1 controls R9A02G011 on three boards.

Remark)

It is necessary to develop a flash memory data for the RL78/G1C on the Port-1 and three R9AG011.

Different slave address of the SMBus should be set to each device by flash memory data.

Figure 5-6 Evaluation environment for multi-source device

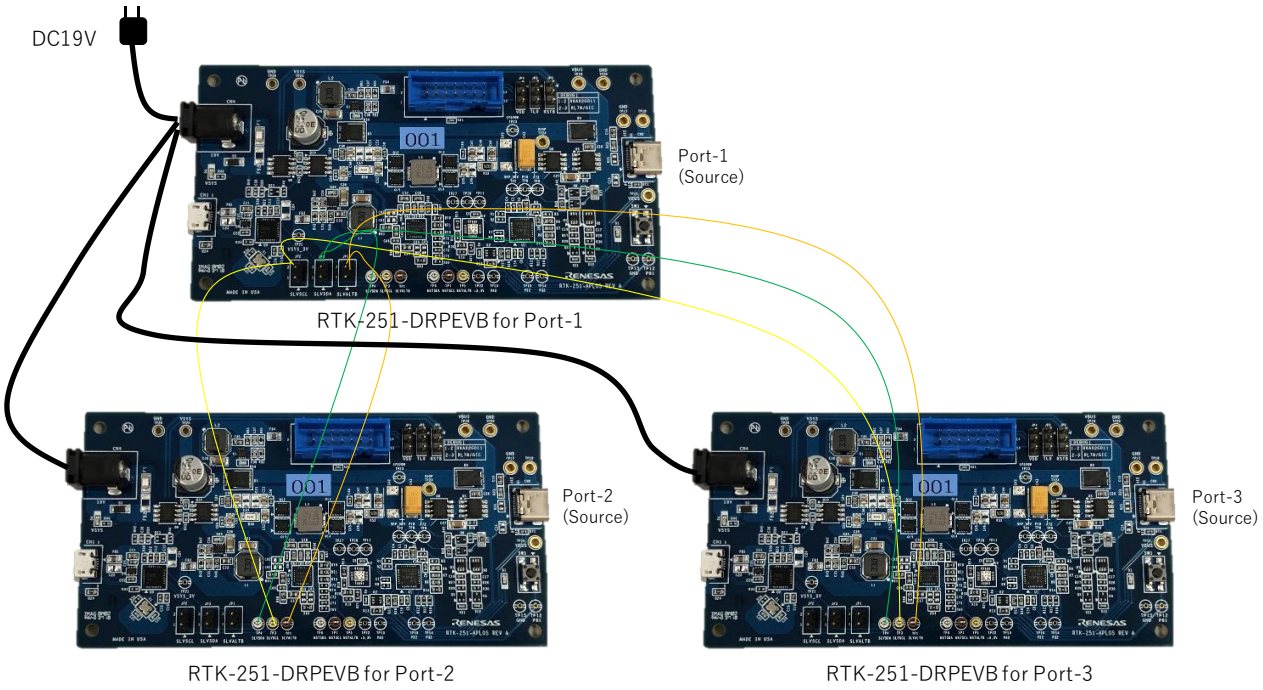


Table 5-5 Signal connection

RTK-251-DRPEVB for Port-1	RTK-251-DRPEVB for Port-2	RTK-251-DRPEVB for Port03
CN4:	CN4:	CN4:
JP1-2: G1C_ALTB	TP1	TP1
JP2-2: G1C_SCL	TP3	TP3
JP3-2: G1C_SDA	TP4	TP4

Table 5-6 RTK-251-DRPEVB for Port-1 setting

CN, JP, TP	Connection	Note
CN4: 19V	Connect to 19V AC Adapter	User needs to design 19V power supply circuit, and evaluate the designed board yourself.
JP1: SLVALTB	Short and connect to TP1 of another Port	
JP2: SLVSCL	Short and connect to TP3 of another Port	
JP3: SLVSDA	Short and connect to TP4 of another Port	
JP4: VDD	1-2 short or 2-3 short	
JP5: TL0	1-2 short or 2-3 short	
JP6: RSTB	1-2 short or 2-3 short	

Table 5-7 RTK-251-DRPEVB for Port-2 setting

CN, JP, TP	Connection	Note
CN4: 19V	Connect to CN4 of the Port-1	User needs to design 19V power supply circuit, and evaluate the designed board yourself.
JP1: SLVALTB	Open (no connection)	
JP2: SLVSCL	Open (no connection)	
JP3: SLVSDA	Open (no connection)	
JP4: VDD	1-2 short	
JP5: TL0	1-2 short	
JP6: RSTB	1-2 short	
TP1: P62/SLVSALTB	Connect to JP1-2 of the Port-1	
TP3: P60/SLVSCL	Connect to JP2-2 of the Port-1	
TP4: P61/SLVSDA	Connect to JP3-2 of the Port-1	

Table 5-8 RTK-251-DRPEVB for Port-3 setting

CN, JP, TP	Connection	Note
CN4: 19V	Connect to CN4 of the Port-1	User needs to design 19V power supply circuit, and evaluate the designed board yourself.
JP1: SLVALTB	Open (no connection)	
JP2: SLVSCL	Open (no connection)	
JP3: SLVSDA	Open (no connection)	
JP4: VDD	1-2 short	
JP5: TL0	1-2 short	
JP6: RSTB	1-2 short	
TP1: P62/SLVSALTB	Connect to JP1-2 of the Port-1	
TP3: P60/SLVSCL	Connect to JP2-2 of the Port-1	
TP4: P61/SLVSDA	Connect to JP3-2 of the Port-1	

6. Configuration option changes for Standard Configuration

This board can be configured as Generic DRP or Sink only (Bus-powered Sink) by using standard firmware and PDC-IMGGEN.

Some configuration changes are realized by following steps.

1. Prepare the required materials for using this board
2. Making flash memory data by the PDC-IMGGEN. -> Refer to 6.1 and 6.2
3. Program flash memory data to PDCs with Renesas on-chip debugging emulator or Renesas USB Power Delivery Flash Writer. -> Refer to Chapter 7

The procedure to generate flash memory data is described in following documents.

- R9A02G011/R9J02G012 Application Note Flash Memory Programming Guide
- USB Power Delivery Controller Flash memory image data generator software (PDC-IMGGEN) Application Note

A hex file should be generated if you use a Renesas on-chip debugging emulator.

A PDFU file should be generated if you use a Renesas USB Power Delivery Writer and a PDFU data is written to a target board.

The PDC-IMGGEN can program data to a target board which doesn't support PDFU without generating file by using Renesas USB Power Delivery Flash Writer.

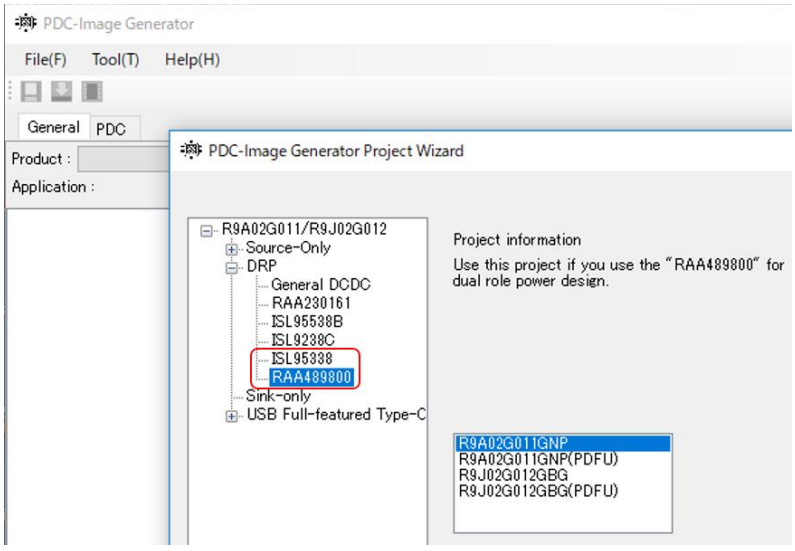
6.1 Generic DRP

The RTK0EUG011D08000BJ and RTK0EUG011D08010BJ can be used as Generic DRP evaluation board instead of the RTK-252-Dual.

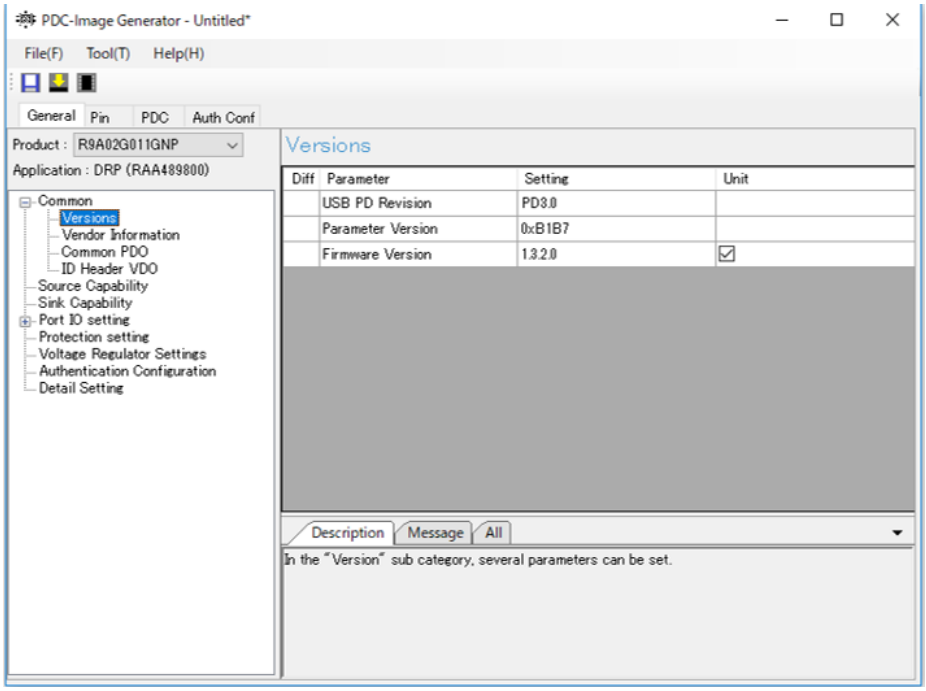
6.1.1 Making flash memory data

Several steps are needed to make flash memory data by PDC-IMGGEN and standard firmware.

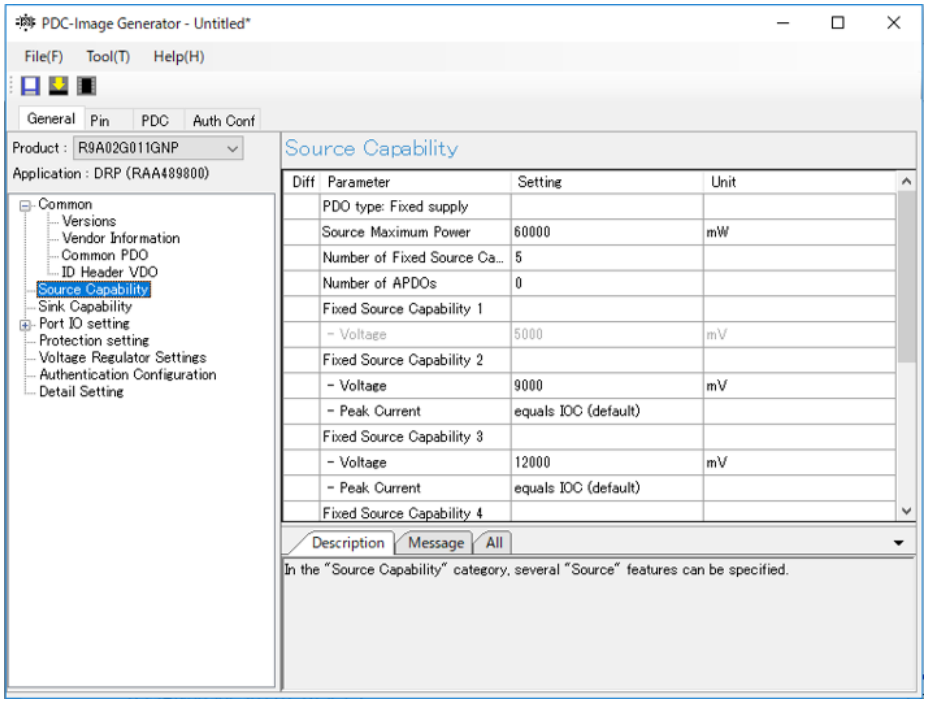
1) Create a new project then select the "DRP" project with "ISL95338" or "RAA489800" according to the actual power supply IC to be used.



2) Specify the appropriate Main FW (such as PDC_1320) in the “Firmware Version” parameter by the “General”-tab.



3) Customize parameters such as Source/Sink Capability, Role for your system’s specification.



4) Make HEX file, then program it by Renesas on-chip debugging emulator. -> Refer to Chapter 7

6.2 Sink only (Bus-powered Sink)

The RTK0EUG011D08000BJ can be used as the Sink-only evaluation board instead of the ET-D720251-0006.

The RTK0EUG011D08010BJ can be used as the Sink-only evaluation board instead of the ET-D720251-0006 and ET-D720251-1006.

It is necessary to modify the board and make flash memory data by standard firmware and PDC-IMGGEN.

In the Sink only feature, RTK-251-DRPEVB performs only as a power sink and requests to a device connected to the CN2 to have a VBUS voltage level but does not provide a VBUS power output.

Figure 6-1 Example of system image for the Sink only device

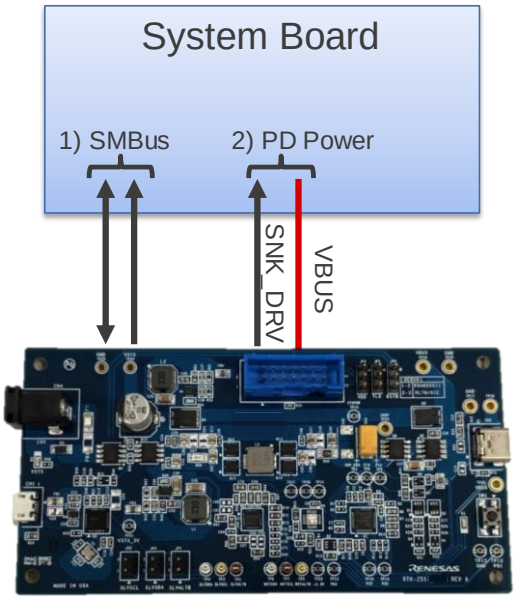


Table 6-1 Example of signal connection for the Sink only device

System Board	RTK-251-DRPEVB	Ref.) ET-D720251-0006 ET-D720251-1006
SDA	TP4: P61/SVLSDA	P61/SVLSDA
SCL	TP3: P60/SLVSCL	P60/SLVSCL
ALTB	TP1: P62/SLVALTB	P62/SLVALTB
SNK_DRV Note	TP13: P82 (SNK_DRV)	P73/SNK_DRV
Discharge	P71	P22/ANI10
Power	TP19: VBUS	VBUS
GND	TP20: GND	GND

[Note] There is a difference of the feature related SNK_DRV between a) RTK-251-DRPEVB (Sink only) and b) ET-D720251-0006/1006 based on each schematic as follows.

a) VBUS output to TP19 regardless of SNK_DRV
b) VBUS output to the pin only when SNK_DRV is asserted

For reference schematic as a simple Sink-only device, it can refer to the schematic of “PD Sink Device for Customer System” which included in this design kit.

6.2.1 Board Modification

Following two modifications are needed to realize the BUS-powered Sink usage.

1) Remove FB3
2) Connect +3.3V and VSYS_3V together.

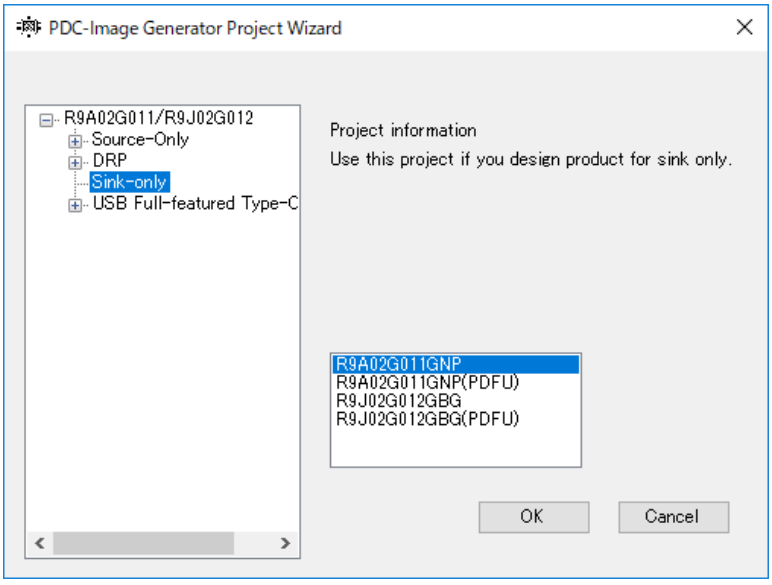
Refer to Figure 6-2.

Figure 6-2 Board fix points

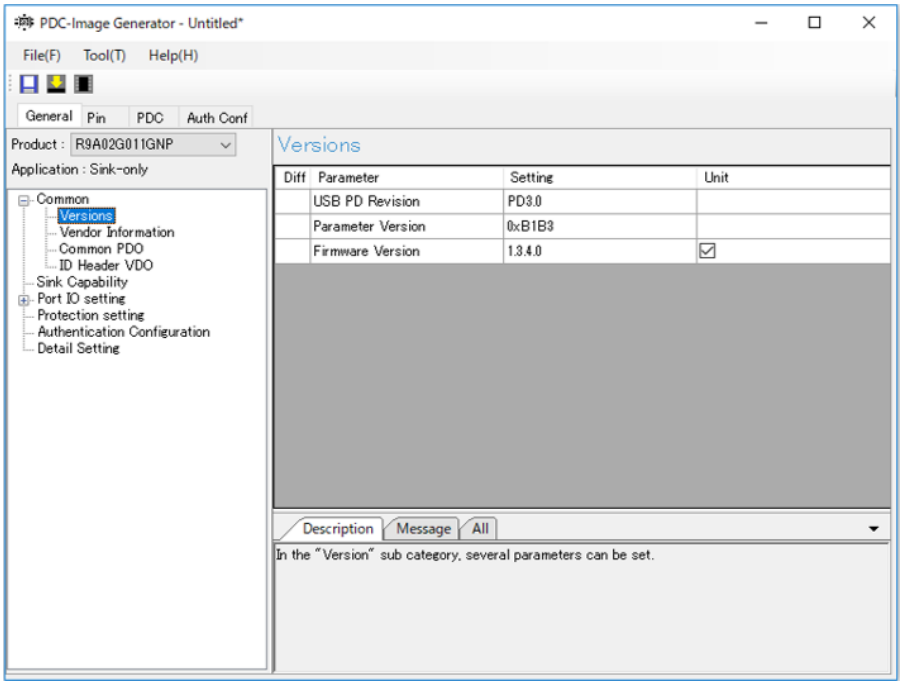
6.2.2 Making flash memory data

Several steps are needed to make flash memory data by PDC-IMGGEN and standard firmware. This section describes the procedure including the minimum required Vendor ID, Product ID, and Sink capability settings.

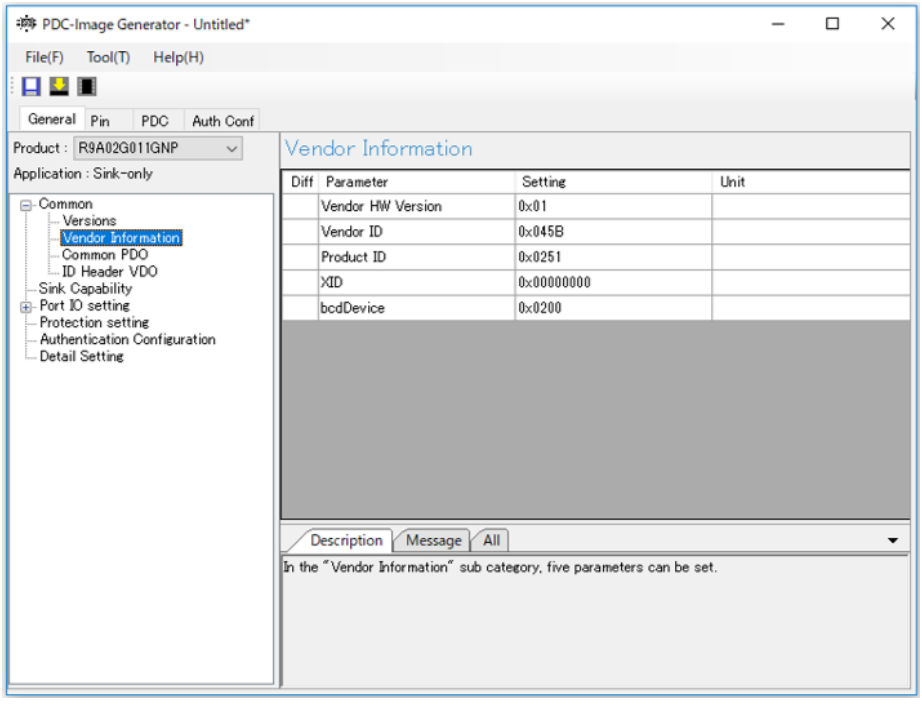
1) Create a new project then select “Sink-only” project



2) Specify the appropriate Main FW (such as PDC_1340) in the “Firmware Version” parameter by the “General”-tab.



3) Specify your "Vendor ID" assigned by USB-IF, and a "Product ID" which is managed by each vendor for a product individually.



Note) The default setting, i.e. 0x045B and 0x0251 are Renesas’s IDs.

4) Select “Number of Sink Capabilities” according to the required Sink Capability (default value is 5).

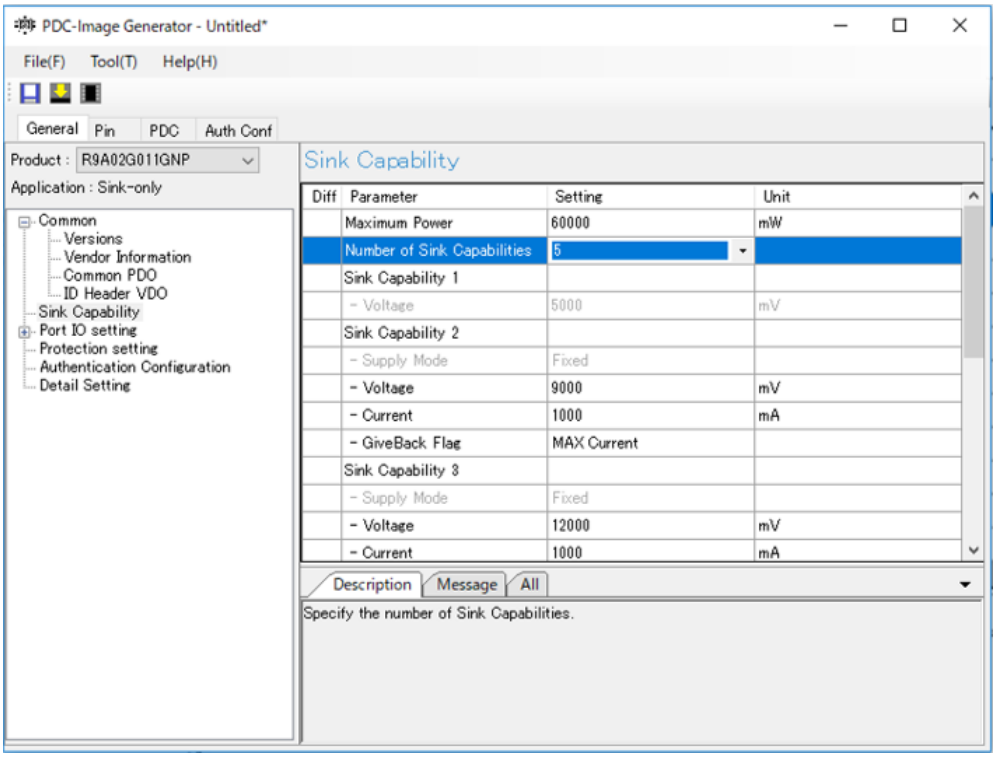


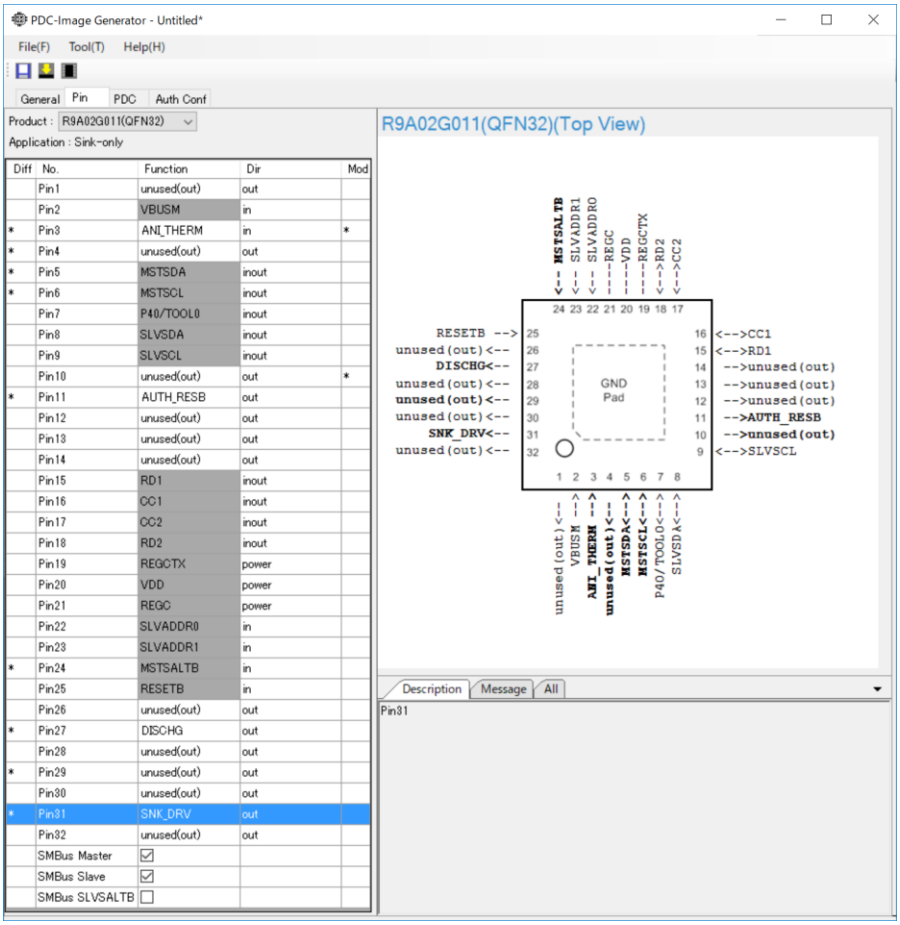
Table 6-2 shows Sink Capability settings according to "Number of Sink Capabilities".

RTK-251-DRPEVB (Sink only) requests the maximum voltage which matched own Sink Capabilities if it is connected to source capable device on CN2.

Table 6-2 Sink Capability settings according to "Number of Sink Capabilities"

Number of Sink Capabilities	Sink Capability 1	Sink Capability 2	Sink Capability 3	Sink Capability 4	Sink Capability 5
	Voltage/Operational current (default setting value)				
5 (default)	5V(fixed)/0.1A	9V/1A	12V/1A	15V/1A	20V/1A
4	5V(fixed)/0.1A	9V/1A	12V/1A	15V/1A	-
3	5V(fixed)/0.1A	9V/1A	12V/1A	-	-
2	5V(fixed)/0.1A	9V/1A	-	-	-
1	5V(fixed)/0.1A	-	-	-	-

5) Select following functions for each pin by the “Pin”-tab **Note**.

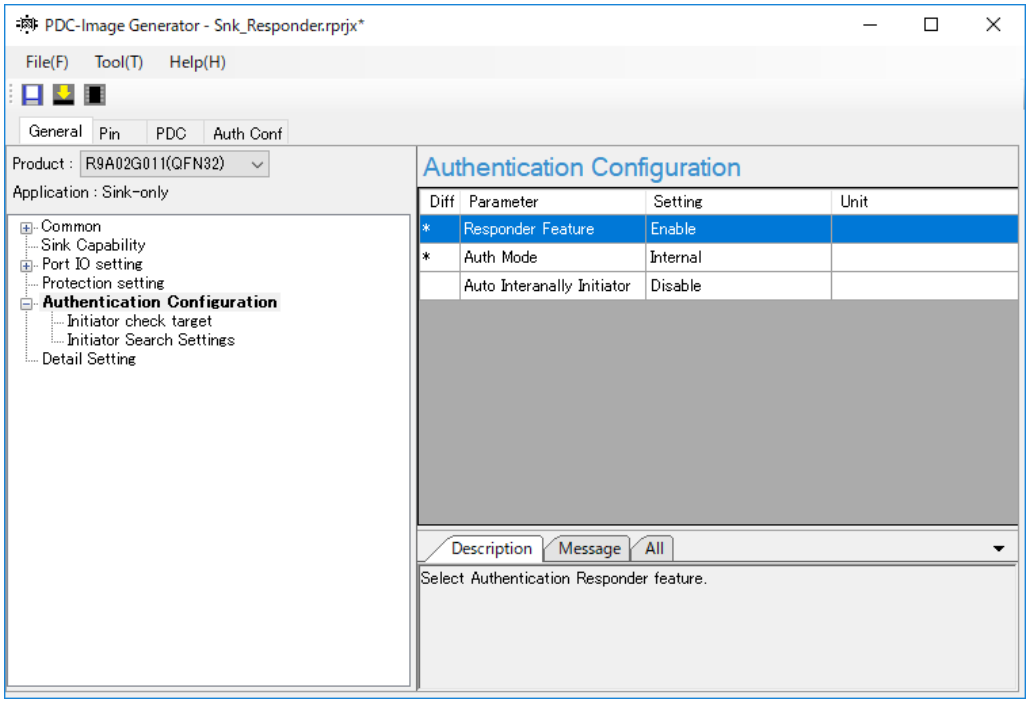


Diff	No.	Function	Dir	Mod
	Pin1	unused(out)	out	
	Pin2	VBUSM	in	
*	Pin3	ANI_THERM	in	*
*	Pin4	unused(out)	out	
*	Pin5	MSTSDA	inout	
*	Pin6	MSTSCL	inout	
	Pin7	P40/TOOL0	inout	
	Pin8	SLVSDA	inout	
	Pin9	SLVSCL	inout	
	Pin10	unused(out)	out	*
*	Pin11	AUTH_RESB	out	
	Pin12	unused(out)	out	
	Pin13	unused(out)	out	
	Pin14	unused(out)	out	
	Pin15	RD1	inout	
	Pin16	CC1	inout	
	Pin17	CC2	inout	
	Pin18	RD2	inout	
	Pin19	REGCTX	power	
	Pin20	VDD	power	
	Pin21	REGC	power	
	Pin22	SLVADDR0	in	
	Pin23	SLVADDR1	in	
*	Pin24	MSTSALTB	in	
	Pin25	RESETB	in	
	Pin26	unused(out)	out	
*	Pin27	DISCHG	out	
	Pin28	unused(out)	out	
*	Pin29	unused(out)	out	
	Pin30	unused(out)	out	
*	Pin31	SNK_DRV	out	
	Pin32	unused(out)	out	
	SMBus Master	☑		
	SMBus Slave	☑		
	SMBus SLVSALTB	☐		

Note SMBus Master and AUTH_RESB should be assigned if enable authentication feature.
“SNK_DRV” is connected to only LED on this board.
“unused (out)” should be selected for the pin’s function is not assigned.

6) Set following authentication feature if setup the board as “Authentication Responder”.

(This setting is only needed to use USB Type-C™ Authentication feature.)



7) Make HEX file, then program it by Renesas on-chip debugging emulator. -> Refer to Chapter 7

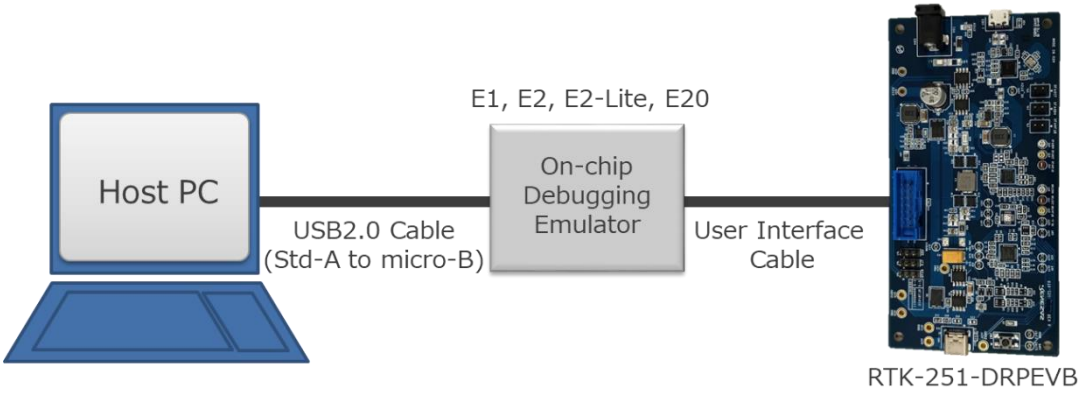
7. Program flash memory data

7.1 Renesas on-chip debugging emulator

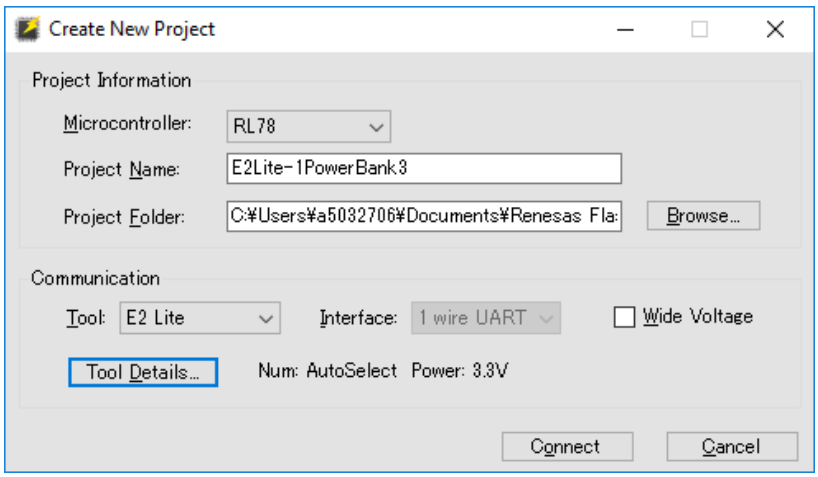
The Renesas on-chip debugging emulator can update the flash memory in the PDCs. The procedure is as follows.

1. Install Renesas Flash Programmer V3 (RFP) to your PC. The application can be download from Renesas Web site. The free-of charge Edition can be used.
2. Connect Renesas on-chip debugging emulator to CN3 on the board.
3. Connect the emulator to USB port of the PC.

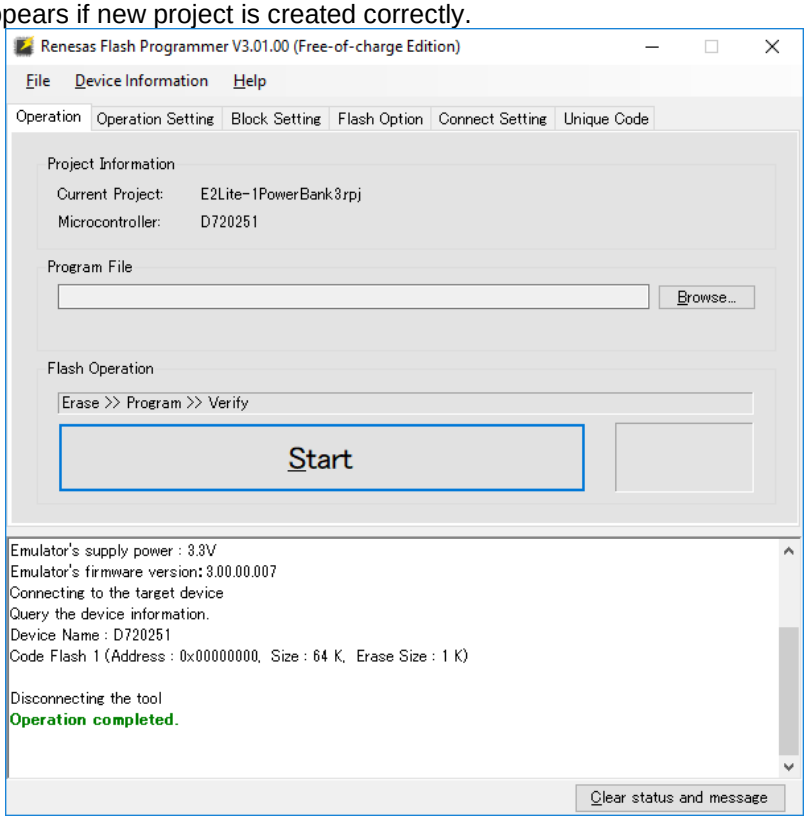
Figure 7-1 Board connection for programming by on-chip debugging emulator



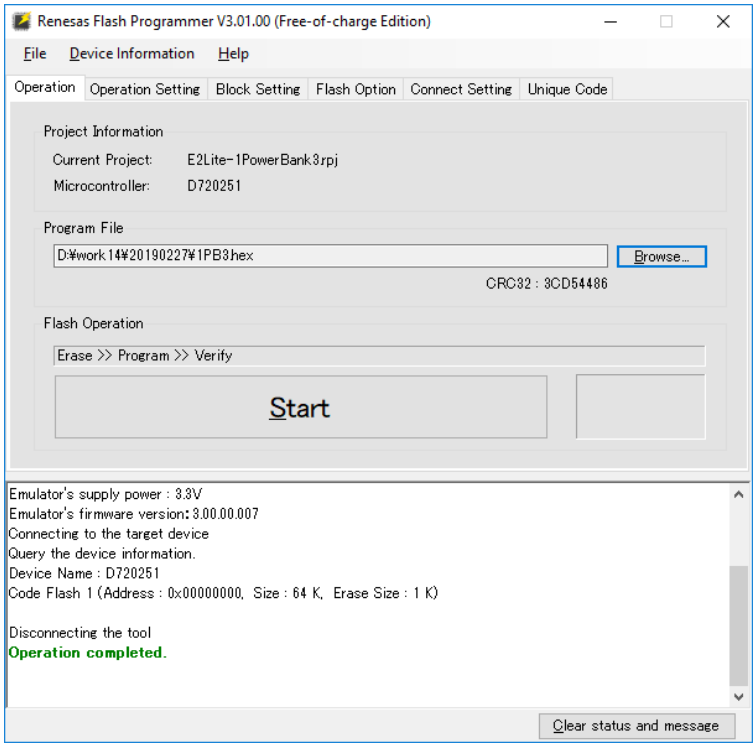
4. Execute the “Renesas Flash Programmer V3.xx.
5. Create a “New Project”.
6. Select the “RL78” in the “Microcontroller”-list box, input an arbitrary name in the “Project Name”
7. Select your on-chip debugging emulator product in the “Tool”-list box.
8. Click the “Tool detail” and select the 3.3V in the Power Supply if supply a power to the RTK-251-DRPEVB board from the on-chip debugging emulator, then click “connect”.



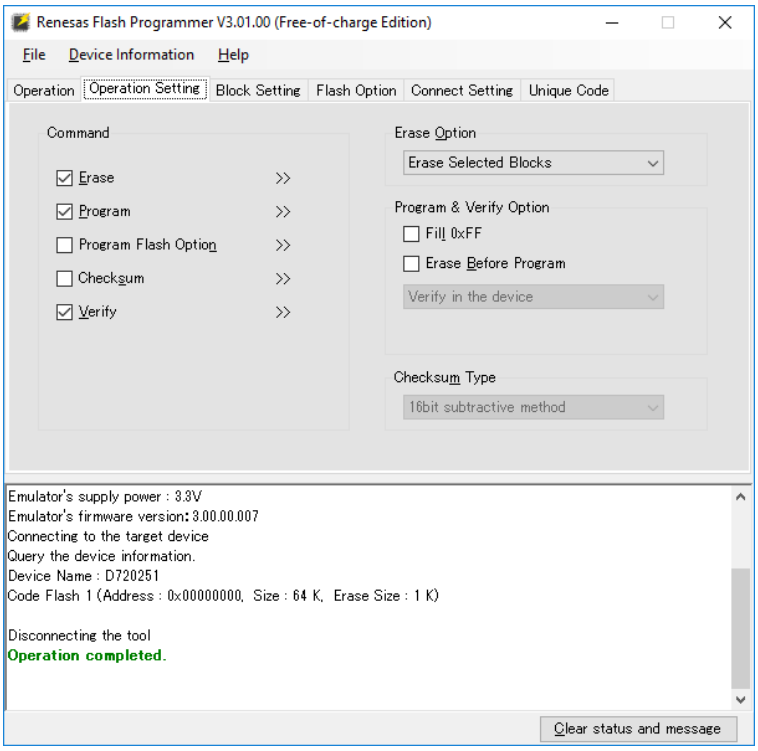
9. Below window appears if new project is created correctly.



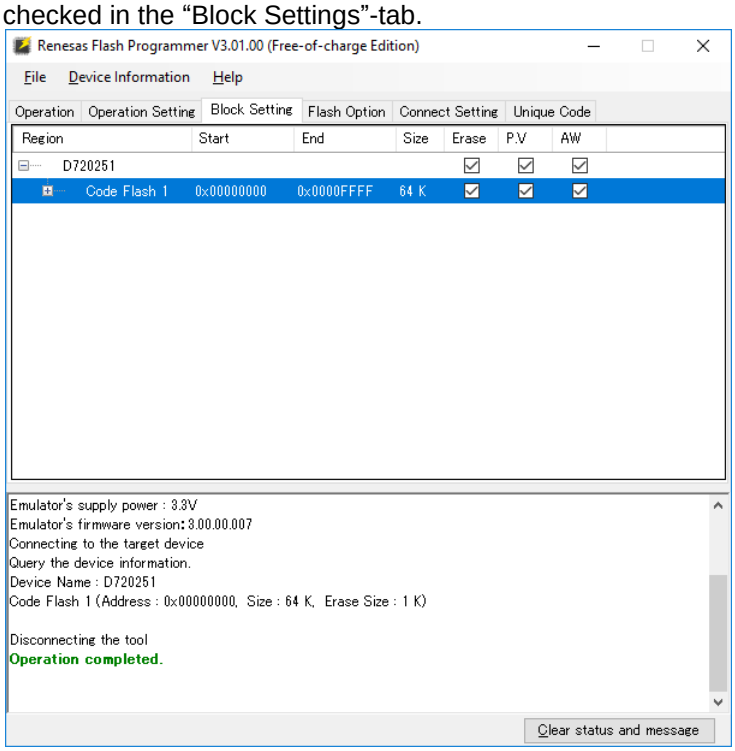
10. Specify a file to update in the “Program File” of the “Operation”-tab.



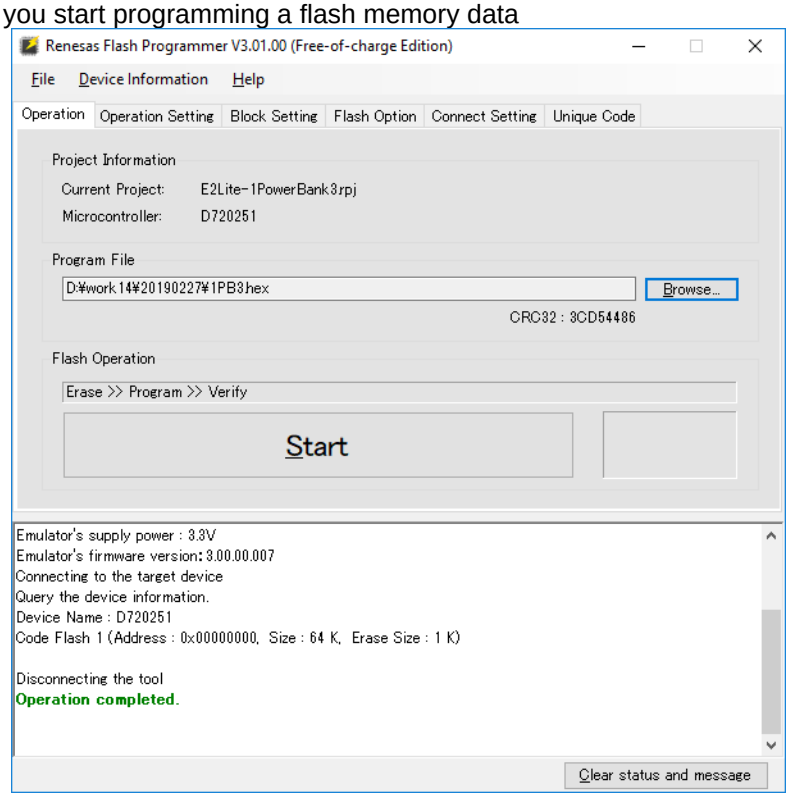
11. Check the “Erase”, “Program” and “Verify” in the “Operation Settings”-tab



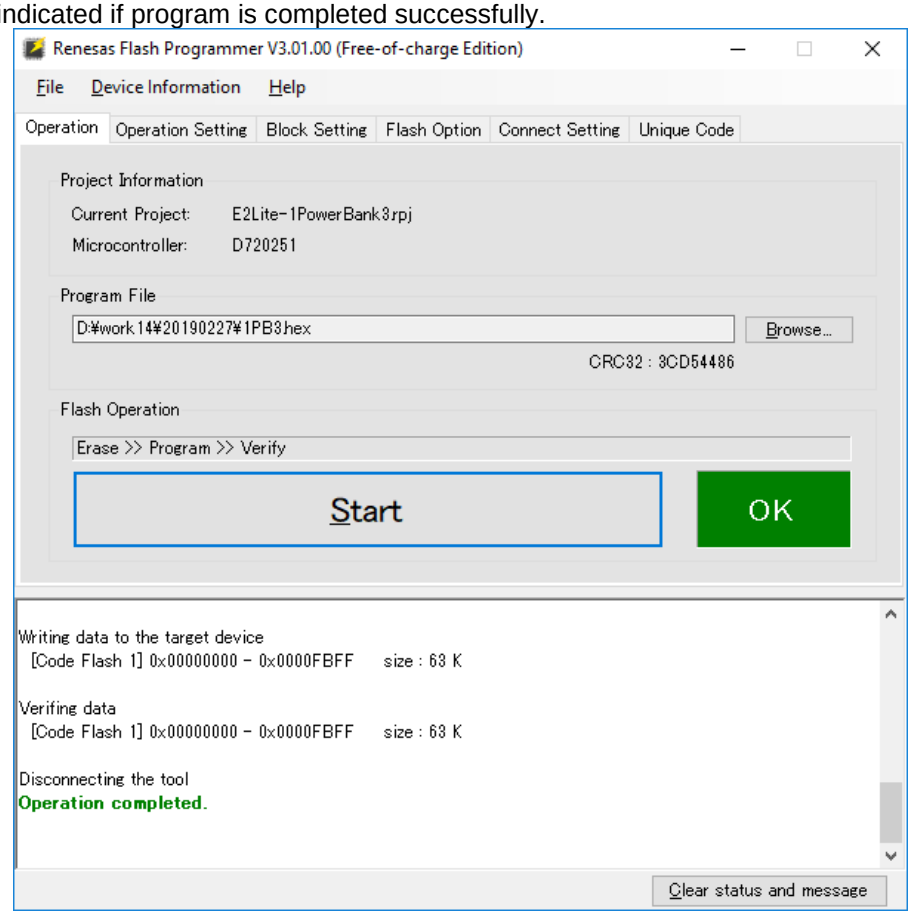
12. Confirm all area are checked in the “Block Settings”-tab.



13. Click the “Start” if you start programming a flash memory data



14. The “OK” is indicated if program is completed successfully.

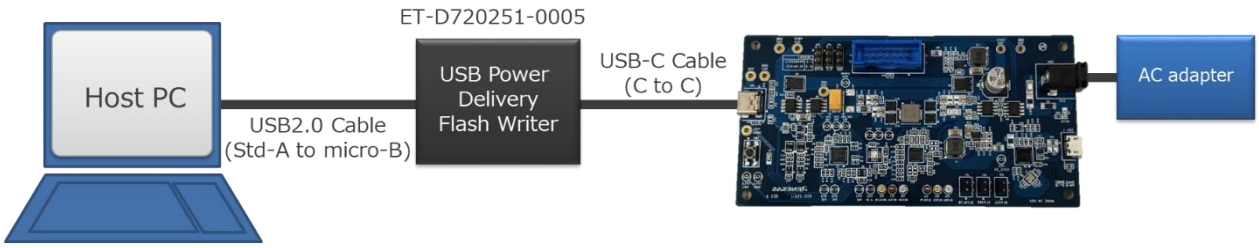


7.2 Renesas USB Power Delivery Flash Writer

The Renesas USB Power Delivery Flash Writer can update the flash memory in the PDCs. The procedure on the PDC-IMGGEN is as follows.

1. Connect RTK-251-DRPEVB to AC adapter.
2. Connect USB Power Delivery Flash Writer to Host PC and make sure that it is detected by Device Manager.
3. Connect USB Power Delivery Flash Writer to RTK-251-DRPEVB.

Figure 7-2 Board connection for programming by USB Power Delivery Flash writer



4. Open command prompt, then execute below command.

   Check the board is recognized from flash writing application below.

   wpdcfw /fwver

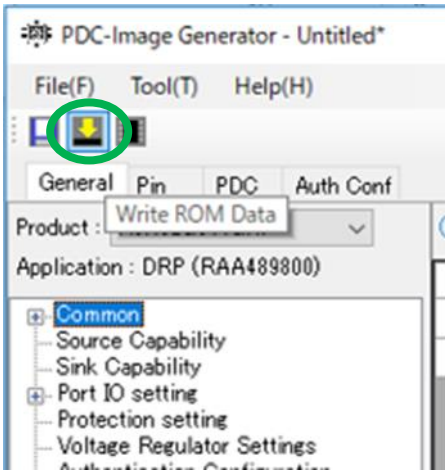
   Program data to the board by below command.

   wpdcfw /write standard.hex /target

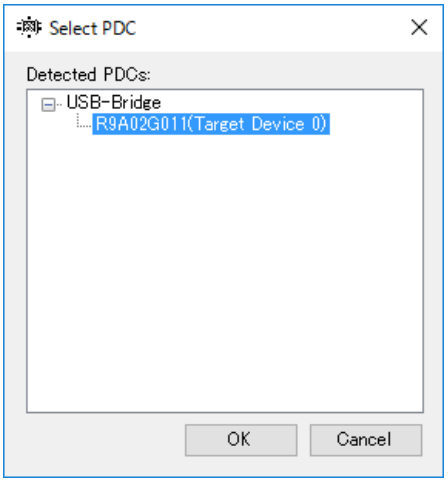
The PDC-IMGGEN can program flash data without making hex file by following procedure.

After setting all parameters,

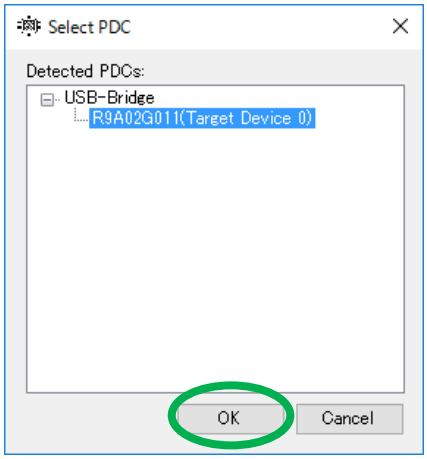
1. Click “ROM WRITE” icon in PDC-IMGGEN. then PDC detection sequence starts



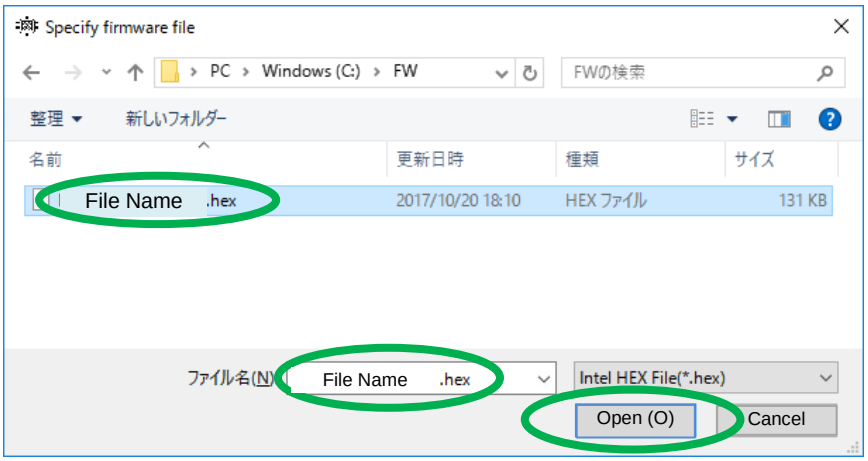
2. After detecting PDC, “Select PDC” window pops up. Select “R9A02G011(Target Device 0)”



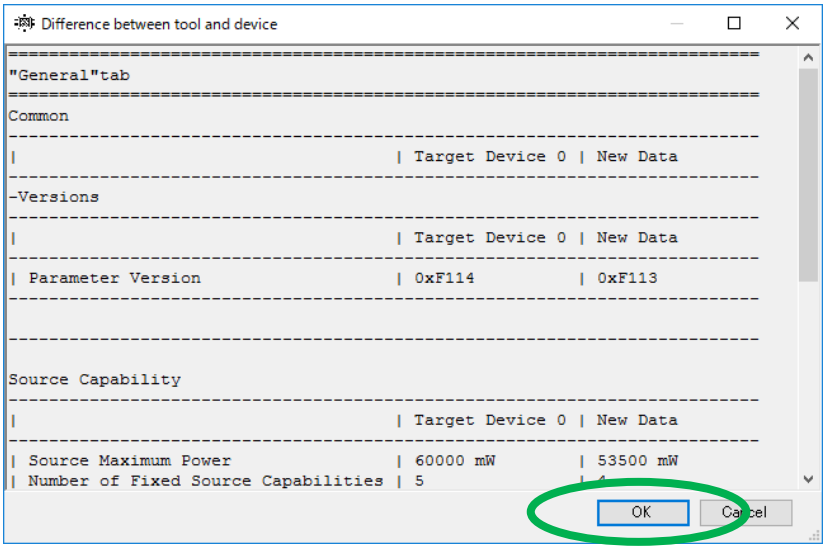
3. Click “OK”. Reading PDC sequence starts.



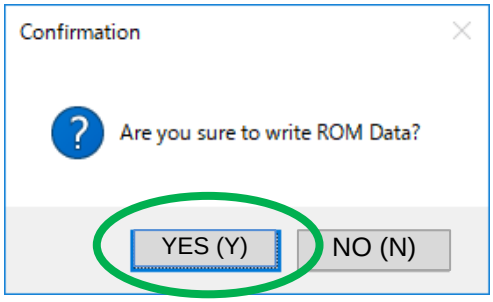
4. After reading PDC sequence, firmware file select window pops up. Then, select PDC firmware (PDC_12xx.hex).



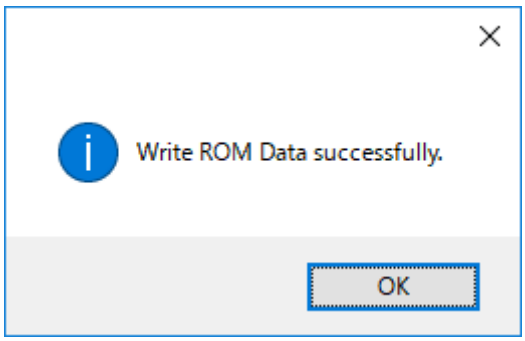
5. After file opens, FW comparative result pops up. Check whether new data is appropriate, then click OK.



6. After confirming the action to be performed, click “YES”. Start writing FW.



7. Finished



Revision History

Rev.	Date	Description	
		Page	**Summary**
1.0	Apr 04, 2019	-	Initial release
1.1	Oct 25, 2019	-	Added support target device of Buck-Boost Voltage Regulator (BB-VR): RAA489800
		11	2.1, Changed shipped out configuration RTK0EUG011D08010BJ
1.2	Dec 6, 2019	15	Corrected the descriptions of section 3.2.1
		25	Added 6.1. Generic DRP
		31	Added 7. Program flash memory data
1.3	Mar 31, 2021	1, 5	Revised descriptions of PD spec version
		10, 11, 14, 15	Revised description about content access
1.4	Sep 30, 2021	2	Updated Related Document
		27 - 32	Updated 6.2 Sink only (Bus-powered Sink)

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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