RX65N Group

Target Board for RX65N LED Blink Control Program

Introduction

The LED lighting control program runs on Target Board for RX65N. The function of this program performs either the user switch interrupt or the timer interrupt according to the mode selection at startup and controls the lighting of the LED by using the corresponding interrupt.

Target Device

RX65N Group

Target Device

IDE: e2studio v6.0.0

Compiler: CC-RX v2.07.00

Smart Configurator: v1.2.0

Hardware: Target Board for RX65N

Contents

1. Function list

The functions of the LED lighting control program are shown below.

  (1) Start-up mode selection
  (2) Timer interrupt function
  (3) User switch interrupt function

1.1 Mode selection of start-up

After resetting with the power-on reset or RES # pin, it detects whether the user switch is pressed and switches the start mode. If you reset while pressing down the user switch, it transits to manual mode, and if you reset without pressing the user switch it will transition to automatic mode.

1.2 Timer interrupt function (Auto-mode)

After switching to the automatic mode, set the timer interrupt and control the LED by timer interrupt. The setting list of the timer interrupt function and the processing contents are shown below

Timer: CMT0

Counter clock: PCLKB / 512

Interrupt interval: 500 ms

Interrupt level: Level 15

Interrupt class: CMI 0

Interrupt processing content: LED 0 (Port: D6), LED 1 (Port: D7) are alternately turned on and off

1.3 User switch interrupt function (Manual-mode)

After manual mode transition, this function is enabled. The setting list and processing contents of the user switch interrupt function are shown below.

Interrupt: IRQ 4 (Port: B1)

Detection type: Falling edge (corresponding to user switch press)

Interrupt level: Level 15

Digital filter: Enable (PCLKB / 64)

Interrupt processing content: LED 0 (Port: D6), LED 1 (Port: D7) are alternately turned on and off

2. LED lighting control program operation flow

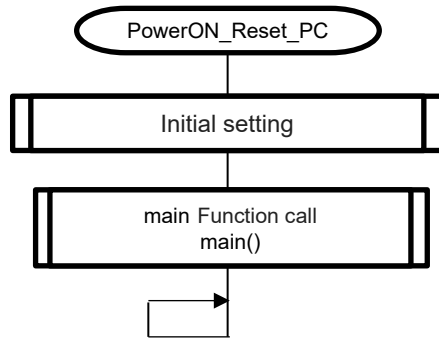**Figure 2-1** shows the power-on reset operation flow of the LED lighting control program.

Figure 2-1: Power-on reset operation flow

Figure 2-2 shows the operation flow of the main function of the LED lighting control program.
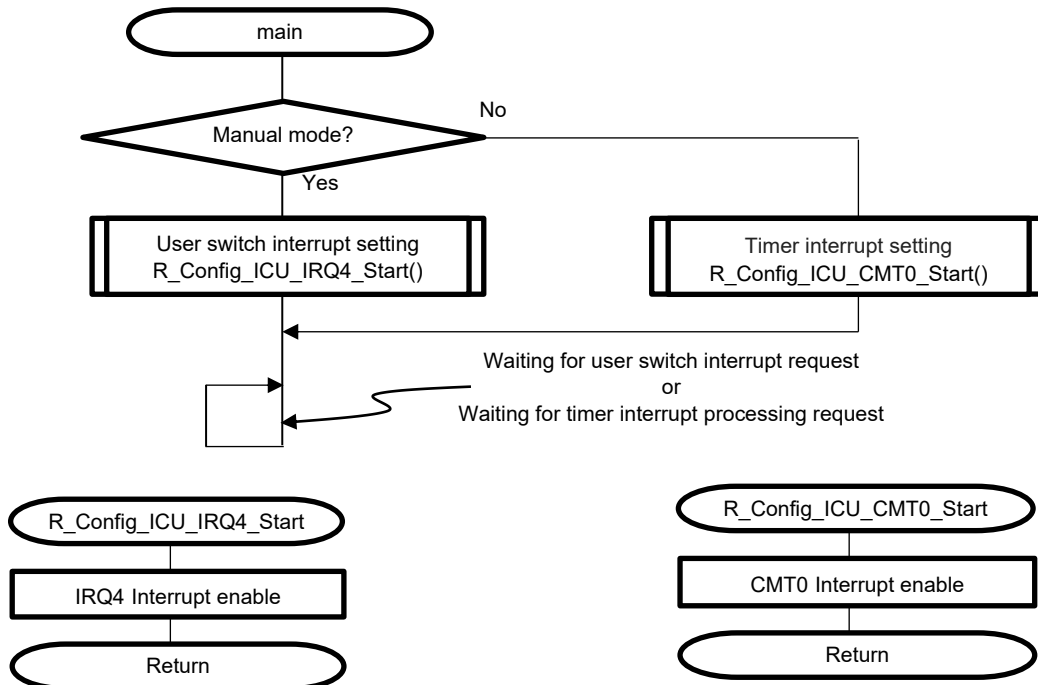

Figure 2-2: LED lighting control program operation flow

Figure 2-3 shows the user switch interrupt operation flow of the LED lighting control program, and **Figure 2-4** shows the timer interrupt operation flow.
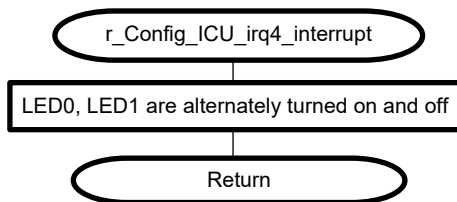
Figure 2-3: User switch interrupt operation flow   **Figure 2-4: Timer interrupt operation flow**
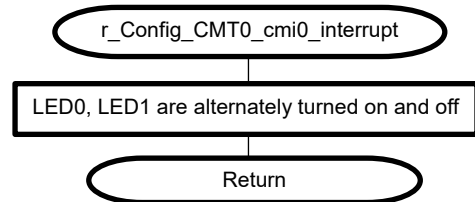
3. RX65N Internal block diagram

Figure 3-1 shows the internal block diagram of the RX65N and the used blocks of the LED lighting control program.
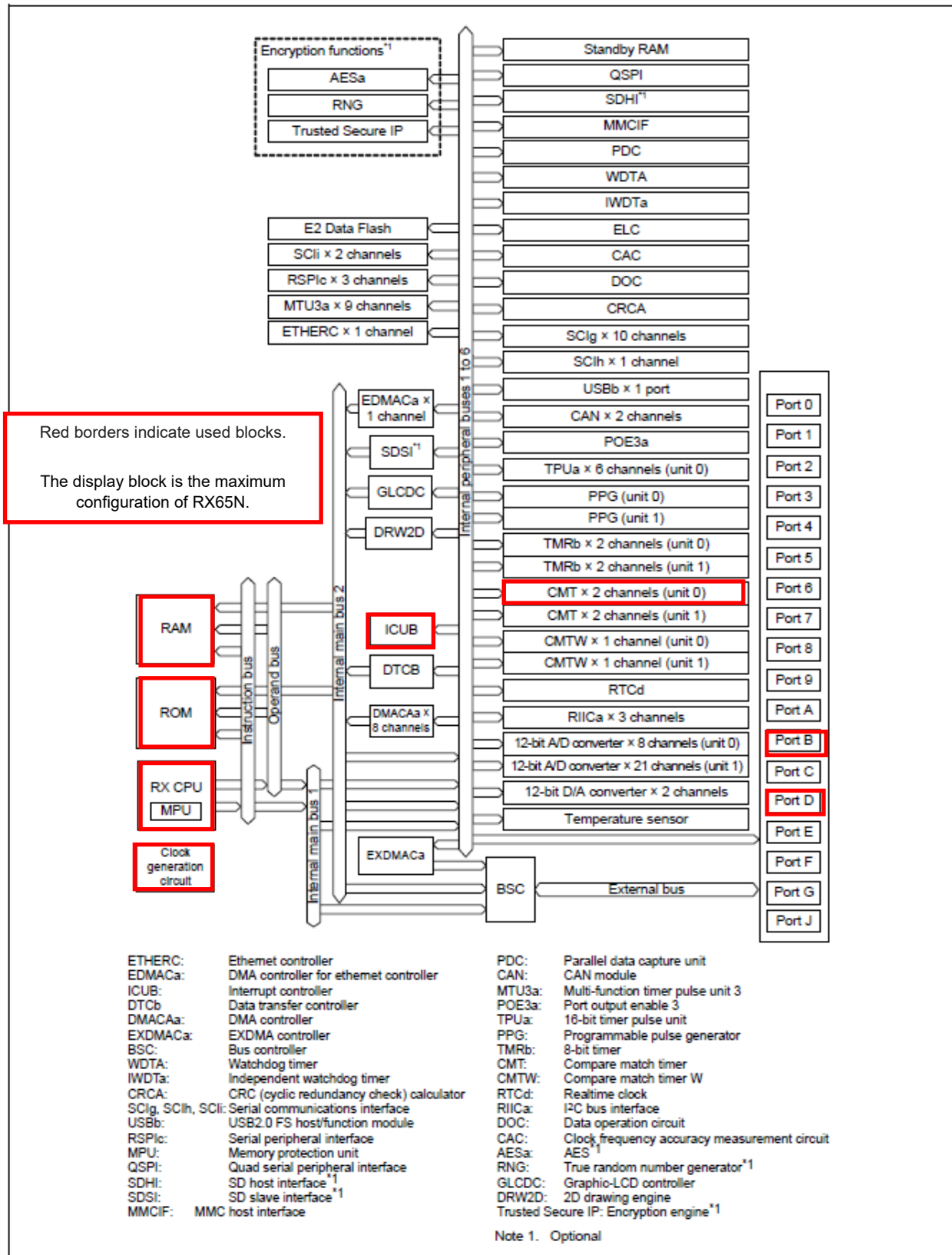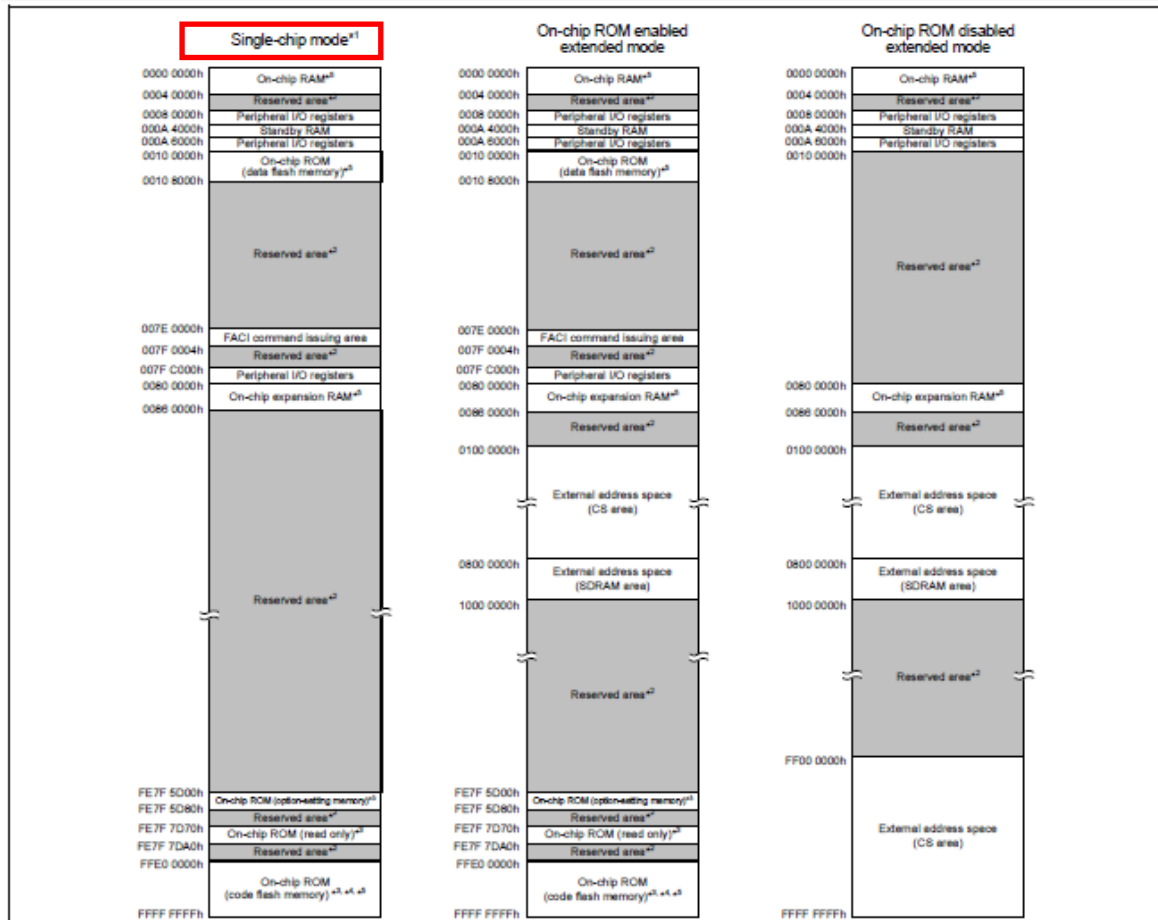

Figure 3-1: RX65N Internal block diagram

4. RX65N Memory map

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4-Gbytes is possible, and this contains both program and data areas. **Figure 4-1** shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

Single-chip mode[1]	On-chip ROM enabled extended mode	On-chip ROM disabled extended mode
0000 0000h On-chip RAM[5]	0000 0000h On-chip RAM[5]	0000 0000h On-chip RAM[5]
0004 0000h Reserved area[7]	0004 0000h Reserved area[7]	0004 0000h Reserved area[7]
0008 0000h Peripheral I/O registers	0008 0000h Peripheral I/O registers	0008 0000h Peripheral I/O registers
000A 4000h Standby RAM	000A 4000h Standby RAM	000A 4000h Standby RAM
000A 6000h Peripheral I/O registers	000A 6000h Peripheral I/O registers	000A 6000h Peripheral I/O registers
0010 0000h On-chip ROM (data flash memory)[5]	0010 0000h On-chip ROM (data flash memory)[5]	0010 0000h
0010 8000h	0010 8000h	
Reserved area[2]	Reserved area[2]	Reserved area[2]
007E 0000h FACI command issuing area	007E 0000h FACI command issuing area	
007F 0004h Reserved area[2]	007F 0004h Reserved area[2]	
007F C000h Peripheral I/O registers	007F C000h Peripheral I/O registers	
0080 0000h On-chip expansion RAM[5]	0080 0000h On-chip expansion RAM[5]	0080 0000h On-chip expansion RAM[5]
0086 0000h	0086 0000h	0086 0000h
	Reserved area[2]	Reserved area[2]
	0100 0000h External address space (CS area)	0100 0000h External address space (CS area)
Reserved area[2]	0800 0000h External address space (SDRAM area)	0800 0000h External address space (SDRAM area)
	1000 0000h	1000 0000h
	Reserved area[2]	Reserved area[2]
		FF00 0000h
FE7F 5D00h On-chip ROM (option-setting memory)[5]	FE7F 5D00h On-chip ROM (option-setting memory)[5]	External address space (CS area)
FE7F 5D80h Reserved area[7]	FE7F 5D80h Reserved area[7]	
FE7F 7D70h On-chip ROM (read only)[5]	FE7F 7D70h On-chip ROM (read only)[5]	
FE7F 7DA0h Reserved area[2]	FE7F 7DA0h Reserved area[2]	
FFE0 0000h On-chip ROM (code flash memory)[3],[4],[5]	FFE0 0000h On-chip ROM (code flash memory)[3],[4],[5]	
FFFF FFFFh	FFFF FFFFh	FFFF FFFFh

Note 1. The address space in boot mode is the same as the address space in single-chip mode.
Note 2. Reserved areas should not be accessed.
Note 3. The access cycle is 1 cycle, 2 cycles, and 3 cycles while the ROMWT[1:0] bits are 00b, 01b, and 10b respectively.
Note 4. The on-chip ROM (code flash memory) can be used in linear mode, where the user area forms a single area, or in dual mode, where the user area is divided into two banks. For details, refer to section 59.2, Structure of Memory in section 59, Flash Memory.
Note 5. The capacities of the code flash memory, data flash memory, and RAM differ depending on the products.

Code Flash Memory			Data Flash Memory		RAM	
Capacity	Address		Capacity	Address	Capacity	Address
	Linear mode	Dual mode (BANKSEL.BANKSWP[2:0] = 111b)				
2 Mbytes	FFE0 0000h to FFFF FFFFh	bank 1: FFE0 0000h to FFEF FFFFh	32 Kbytes	0010 0000h to 0010 7FFFh	640 Kbytes	0000 0000h to 0003 FFFFh
		bank 0: FFF0 0000h to FFFF FFFFh				0080 0000h to 0085 FFFFh
1.5 Mbytes	FFE8 0000h to FFFF FFFFh	bank 1: FFE4 0000h to FFEF FFFFh	32 Kbytes	0010 0000h to 0010 7FFFh	640 Kbytes	0000 0000h to 0003 FFFFh
		bank 0: FFF4 0000h to FFFF FFFFh				0080 0000h to 0085 FFFFh
1 Mbyte	FFF0 0000h to FFFF FFFFh	—	—	—	256 Kbytes	0000 0000h to 0003 FFFFh
768 Kbytes	FFF4 0000h to FFFF FFFFh	—	—	—	256 Kbytes	0000 0000h to 0003 FFFFh
512 Kbytes	FFF8 0000h to FFFF FFFFh	—	—	—	256 Kbytes	0000 0000h to

The red frame shows the operation mode and each flash / RAM capacity.

Figure 4-1: RX65N Memory map

5.   RX65N Clock generation block diagram

Figure 5-1 shows the clock generation route of the RX65N clock generation block diagram and the LED lighting control program.
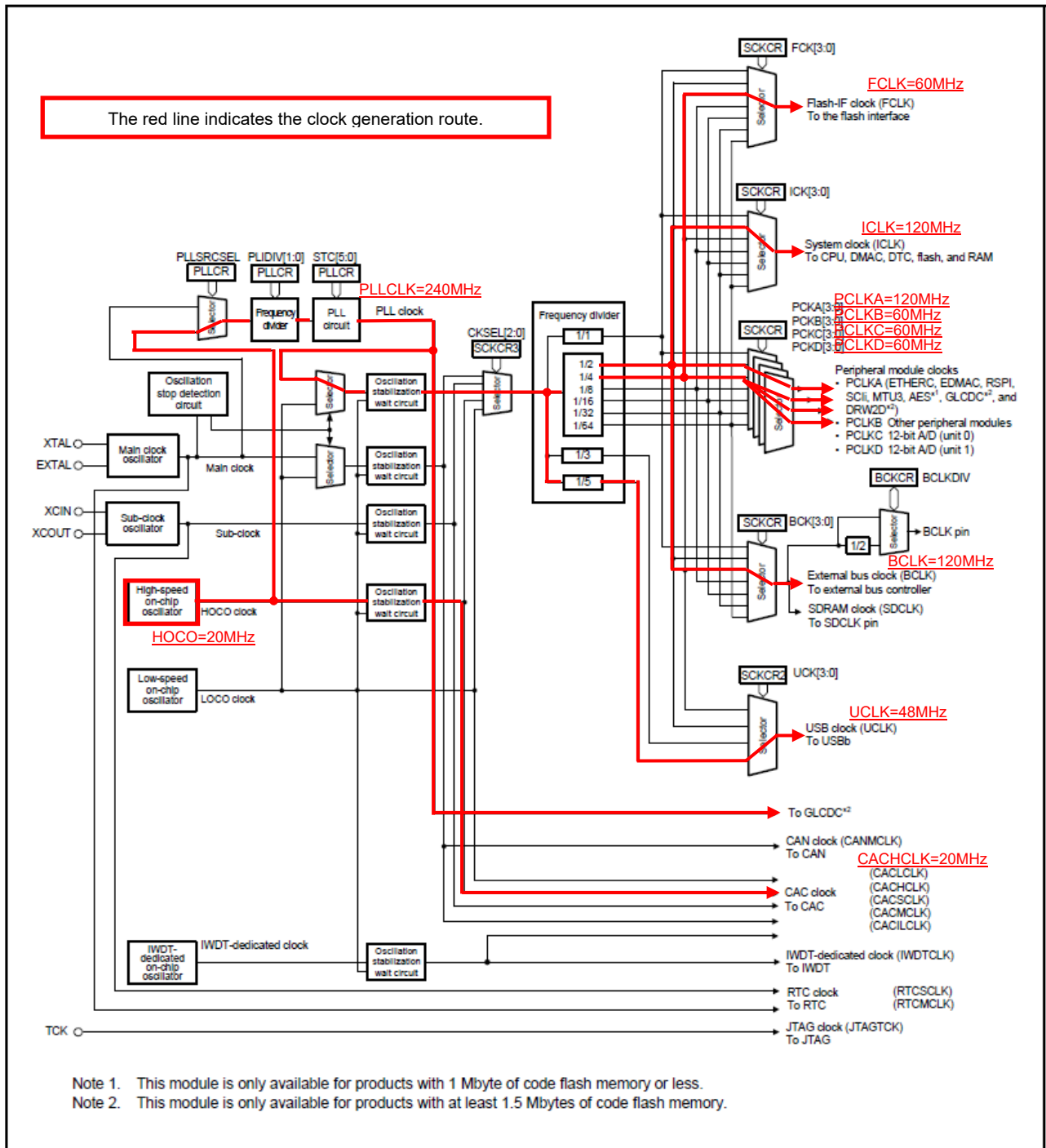

Figure 5-1: RX65N Clock generation block diagram

6. Precautions

Please do not incorporate this program into your product. This program does not guarantee the operation. When using it, please check the operation at your own risk.

Website and Support

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Oct 13, 2017	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

(Rev.3.0-1 November 2016)

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