RX66T-Group

Power Supply Control of a Three-Level Inverter by Using SiC Power Elements

Introduction

The aim of this application note is to explain how to implement two-level and three-level inverter control software for a three-phase, 50- or 60-Hz, 400-V, 10-kW inverter power supply, by using functions of the RX66T microcontroller, and how to use the library of the Renesas Motor Workbench tool, a support tool for motor control development. Note that the Smart Configurator tool is used for the target software of this application note.

The target software of this application note is only to be used for reference and Renesas Electronics Corporation does not guarantee the operation. Use the software after thorough evaluation in a suitable environment.

Target Device

Operations of the target software of this application note are checked by using the following device.

- RX66T (R5F566TEADFP)

Target Software

The following shows the target software of this application note:

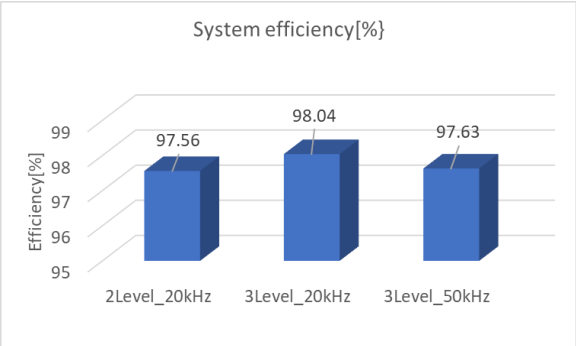
- RX66T_THREE_LEVEL_INVERTER_CTRL_CSP_Vxxx (IDE: CS+)
- RX66T_THREE_LEVEL_INVERTER_CTRL_E2S_Vxxx (IDE: e^2 studio)

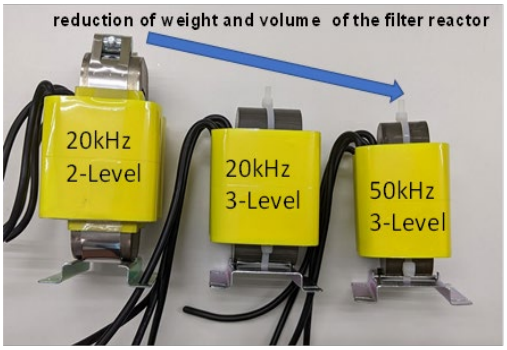
Reference Materials

- RX66T Group User's Manual -- Hardware (R01UH0749)
- Renesas Motor Workbench User's Manual (R21UZ0004)
- Smart Configurator User's Manual -- RX API Reference (R20UT4360)
- RX Smart Configurator User Guide -- CS+ (R20AN0470)
- RX Smart Configurator User Guide -- e^2 studio (R20AN0451)

Application effect of the 3-Level inverter topology

Compared with the 2-Level inverter, the 3-Level inverter can reduce the switching loss of the power devices. It improves the efficiency of inverter system and reduces size and weight of the filter reactors.





Contents

1. Overview

This application note describes how to implement two- or three-level inverter power supply control software by using functions of the RX66T microcontroller and how to use the library of the Renesas Motor Workbench tool, a support tool for motor control development.

1.1 Development Environments

Table 1-1 and Table 1-2 show the development environments for the software that this application note covers.

Table 1-1 Hardware Development Environment

Microcontroller	Evaluation Board
RX66T (R5F566TEADFP)	Three-phase, 50- or 60-Hz, 400-V, 10-kW inverter board*1 and RX66T CPU board*2

Table 1-2 Software Development Environment

IDE Version	Smart Configurator for RX Microcontrollers	Toolchain Version*3
CS+: V8.07.00	Version 2.11.0	CC-RX: V3.04.00
e^2 studio: 2022-01	Plug-in version of e^2 studio	

For the purchase or technical support of this system, contact a Renesas Electronics Corporation sales representative or an authorized Renesas Electronics Corporation product distributor.

Notes: 1. For details on the three-phase, 50- or 60-Hz, 400-V, 10-kW inverter power supply board (DAIV157-T4010-1), contact a Renesas Electronics sales office.
2. The CPU board used in this application note is from Renesas Electronics Corporation.
3. If the same version of the toolchain (C compiler) specified in the project is not in the import destination, the toolchain will not be selected, and an error will occur. Check the selected state of the toolchain on the project configuration dialog.
For the setting method, refer to FAQ 3000404.
(https://en-support.renesas.com/knowledgeBase/18398339)

2. Overview of the System

This section gives an overview of this system.

2.1 Specifications of the System

(1) Outline of Control over a Two- or Three-Level Inverter Power Supply

The output voltages in control over a two-level inverter power supply have PWM waveforms with two values, ±VDD/2 relative to the neutral point. On the other hand, the output voltages in control over a three-level inverter power supply also have PWM waveforms but with three values, ±VDD/2 relative to the neutral point and zero. An advantage of the latter is output waveforms that are closer to sine waves. Using SiC power elements in the main circuit to make the frequency higher enables the production of waveforms that are far closer to sine waves. This helps reduce the size of the LC filters.

In addition, the output voltage swing for a three-level inverter per switching action is half that for a two-level inverter, so the three-level inverter has less switching loss and the system generates less noise. Therefore, three-level inverters are suitable for reducing the size and improving the efficiency of a system. Figure 2-1 shows two- and three-level inverter circuits for comparison.

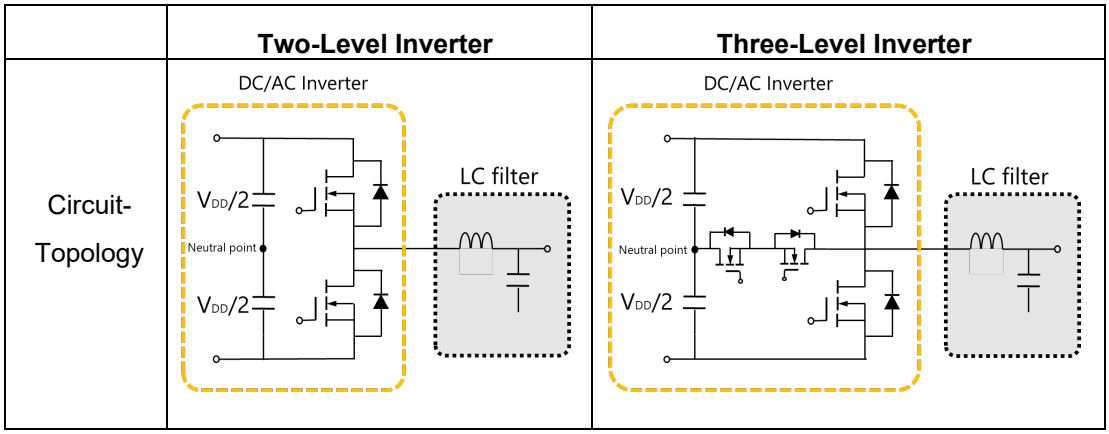


Figure 2-1 Comparison of Two- and Three-Level Inverter Circuits

(2) Basic Specifications of the System

Table 2-1 shows the basic specifications of this system.

Table 2-1 Basic Specifications of the System

Item	Specifications
Control method	Two- or three-level inverter power supply control
Output power	10 kW
Output voltage	3Φ, 400 Vac
Output frequency	50 or 60 Hz
Input voltage range	600 to 850 Vdc
Inverter switching frequency	20 to 50 kHz
Power factor	0.8

2.2 Hardware Configuration

Figure 2-2 shows the configuration of hardware.

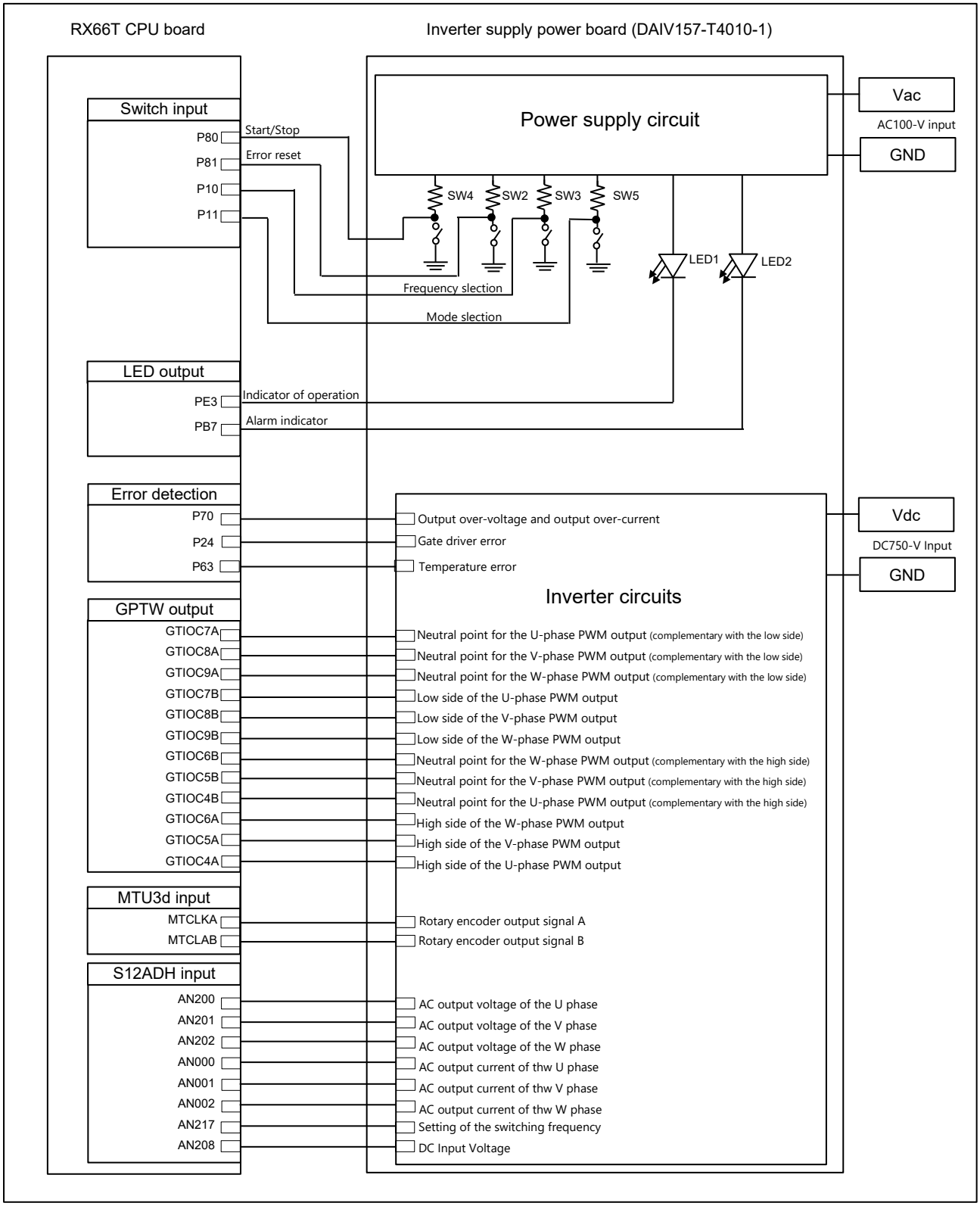


Figure 2-2 Hardware Configuration Diagram

2.3 Hardware Specifications

(1) User Interface

Table 2-2 lists the parts for the user interface of this system.

Table 2-2 User Interface

Item	Parts for the User Interface	Function
Main switch	Toggle switch (SW1)	Input of main power
Operation switch	Toggle switch (SW4)	Directive to start or stop operation
Frequency selection switch	Slide switch (SW3)	Selects 50 or 60 Hz as the inverter output frequency.
Mode selection switch	Slide switch (SW5)	Selects two- or three-level operation.
Reset button switch	Press switch (SW2)	Releases the system from the alarm state.
Initial carrier frequency volume controller	Trimming potentiometer (VR4)	Sets the switching frequency in transitions from the stopped state to the operating state.
Mid-operation carrier frequency encoder	Encoder (RE1)	Changes the switching frequency during operation.
Indicator of the power for control	Red LED (D1)	The power for control is being supplied: LED turned on No alarm: LED turned off
Alarm indicator	Red LED (D21)	The alarm is being generated: LED turned on No alarm: LED turned off
Indicator of operation	Red LED (D22)	Operating: LED turned on Stopped: LED turned off

(2) Pin Interfaces

Table 2-3 lists the pin interfaces for this system.

Table 2-3 Pin Interfaces (1/2)

R5F566TEADFP Pin Name	Function
PE3	Output for the operating or stopped state indicator (high: stopped, low: operating)
PB7	Output for the alarm or non-alarm state indicator (high: alarm, low: non-alarm)
P95/GTIOC7A	Neutral point for the U-phase PWM output (complementary with the low side)
P94/GTIOC8A	Neutral point for the V-phase PWM output (complementary with the low side)
P93/GTIOC9A	Neutral point for the W-phase PWM output (complementary with the low side)
P92/GTIOC7B	Low side of the U-phase PWM output
P91/GTIOC8B	Low side of the V-phase PWM output
P90/GTIOC9B	Low side of the W-phase PWM output
P76/GTIOC6B	Neutral point for the W-phase PWM output (complementary with the high side)
P75/GTIOC5B	Neutral point for the V-phase PWM output (complementary with the high side)
P74/GTIOC4B	Neutral point for the U-phase PWM output (complementary with the high side)
P73/GTIOC6A	High side of the W-phase PWM output

P72/GTIOC5A	High side of the V-phase PWM output
P71/GTIOC4A	High side of the U-phase PWM output
P70	Indicator for detection of an output overvoltage or output overcurrent (high: in the normal state, low: in an abnormal state)
P33/MTCLKA	Rotary encoder output signal A
P32/MTCLKB	Rotary encoder output signal B
P24	Indicator for detection of a gate driver error (high: in the normal state, low: in the abnormal state)

Table 2-3 Pin Interfaces (2/2)

P21/AN217	Setting of the switching frequency in transitions from the stopped state to the operating state
P63/MTIOC4D	Indicator for detection of a temperature error (high: in the normal state, low: in the abnormal state)
P62/AN208	Measurement of the positive voltage of the DC input relative to the negative voltage
P54/AN202	Measurement of the AC output voltage of the W phase relative to the neutral point
P53/AN201	Measurement of the AC output voltage of the V phase relative to the neutral point
P52/AN200	Measurement of the AC output voltage of the U phase relative to the neutral point
P42/AN002	Measurement of the AC output current of the W phase
P41/AN001	Measurement of the AC output current of the V phase
P40/AN000	Measurement of the AC output current of the U phase
P81	Setting of release from the alarm state (change of level on the pin for release from the alarm state: from high to low for at least 100 ms then back to high)
P80	Setting of a request for operation or release from the request (low: a request for operation, high: release of the request for operation)
P11	Selection of inverter operation (high: three-level, low: two-level)
P10	Selection of AC output frequency of the inverter (high: 50 Hz, low: 60 Hz)

(3) Peripheral Functions

Table 2-4 lists the peripheral functions used for this system.

Table 2-4 List of the Peripheral Functions

12-Bit A/D Converter	CMT	GPT	MTU3d
● Detection of the output currents of the U, V, and W phases ● Detection of the output voltages of the U, V, and W phases ● Detection of the DC voltage ● Initial switching frequency	● 1-ms interval timer ● 50-µs interval timer ● Output frequency phase timer	● Complementary PWM outputs	● Phase counter for the mid-operation carrier frequency encoder

(a) 12-Bit A/D Converter (S12ADH)

Unit 0 measures the U-phase output current (I_u), V-phase output current (I_v), and W-phase output current (I_w), in single scan mode (with the use of a hardware trigger).
Unit 2 measures the U-phase output voltage (V_u), V-phase output voltage (V_v), W-phase output voltage (V_w), DC input voltage (V_{in}), and initial switching frequency (F_{pwm_ini}) in single scan mode (with the use of a hardware trigger).

(b) Compare Match Timer (CMT)

The channel 0 compare match timer is used as a 1-ms interval timer.
The channel 1 compare match timer is used as a 50-µs interval timer.
The channel 2 compare match timer is used for counting phases of the output frequency.

(c) General PWM Timer (GPTW)

The channels 4 to 9 general PWM timers output waveforms that include dead time (active high) in complementary PWM mode.

(d) Multi-Function Timer Pulse Unit 3 (MTU3d)

The channel 1 multi-function timer pulse unit 3 in phase counting mode counts changes to the mid-operation carrier frequency encoder.

2.4 Software Configuration

2.4.1 Software File Configuration

Figure 2-3 shows the folder and file configuration of the software.

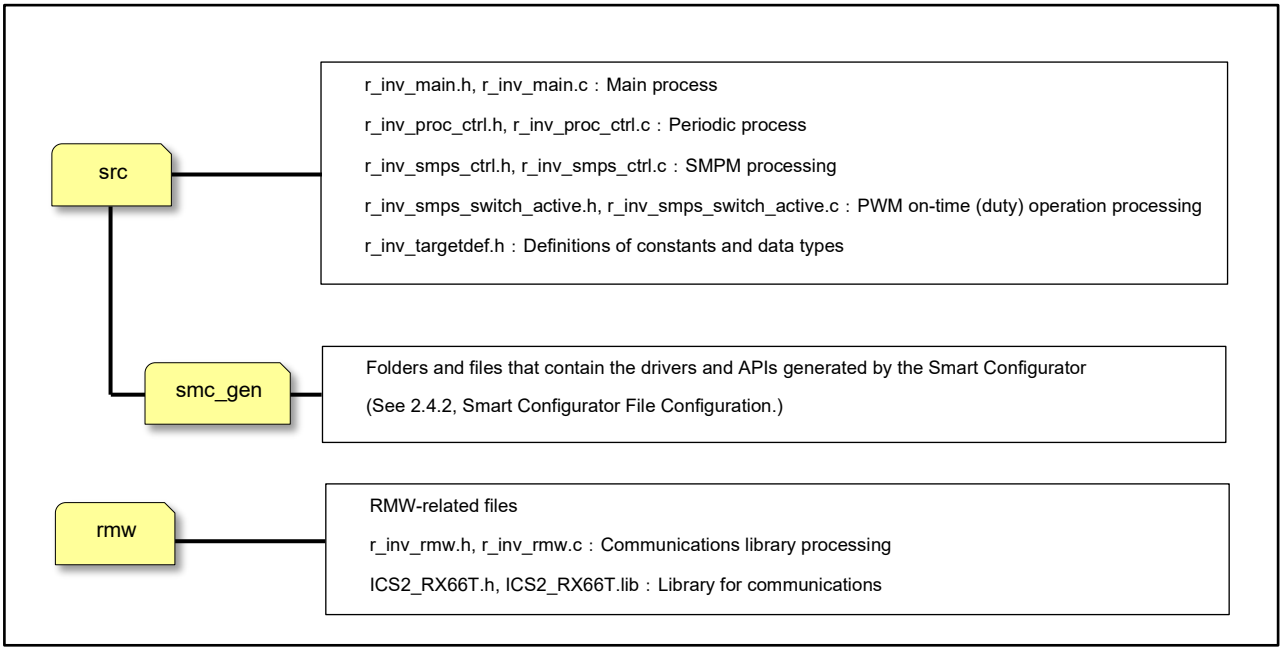


Figure 2-3 Folder and File Configuration

2.4.2 Smart Configurator File Configuration

Peripheral drivers were easily configured for this project by using the Smart Configurator tool (SC).

The SC saves the setting information on the MCU, peripheral functions, pin functions, and so on for use in the project in the project file (*.scfg) and refers to that information. Refer to the following file to confirm the peripheral function settings of this software.

"RX66T_THREE_LEVEL_INVERTER_CTRL_xxx_Vyyy.scfg"
(xxx: CSP indicates the version is for use with CS+. E2S indicates the version is for use with the e^2 studio. yyy: version and revision number)

Figure 2-4 shows the configuration of folders and files generated by the SC.

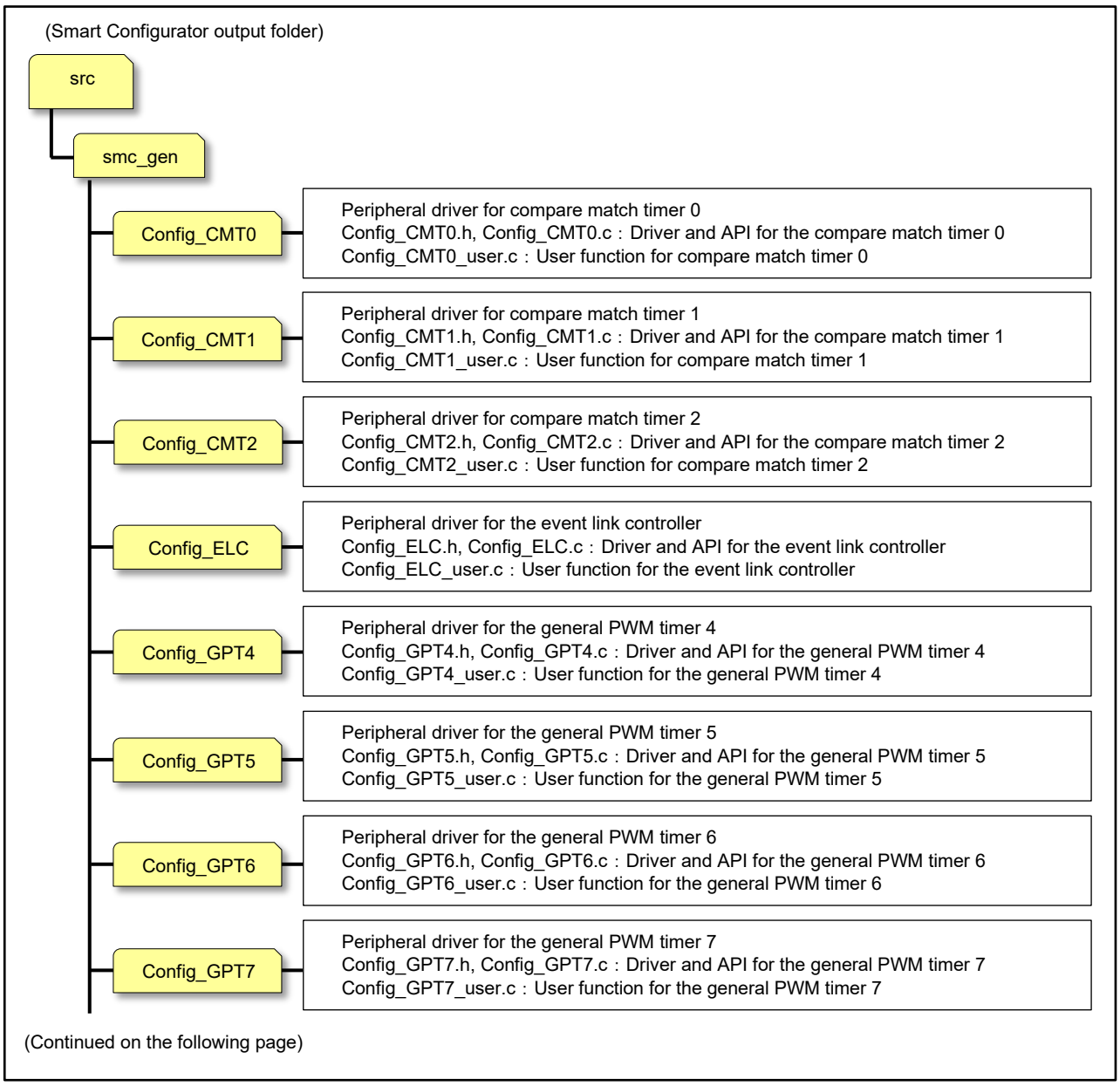


Figure 2-4 Configuration of Folders and Files from the Smart Configurator (1/2)

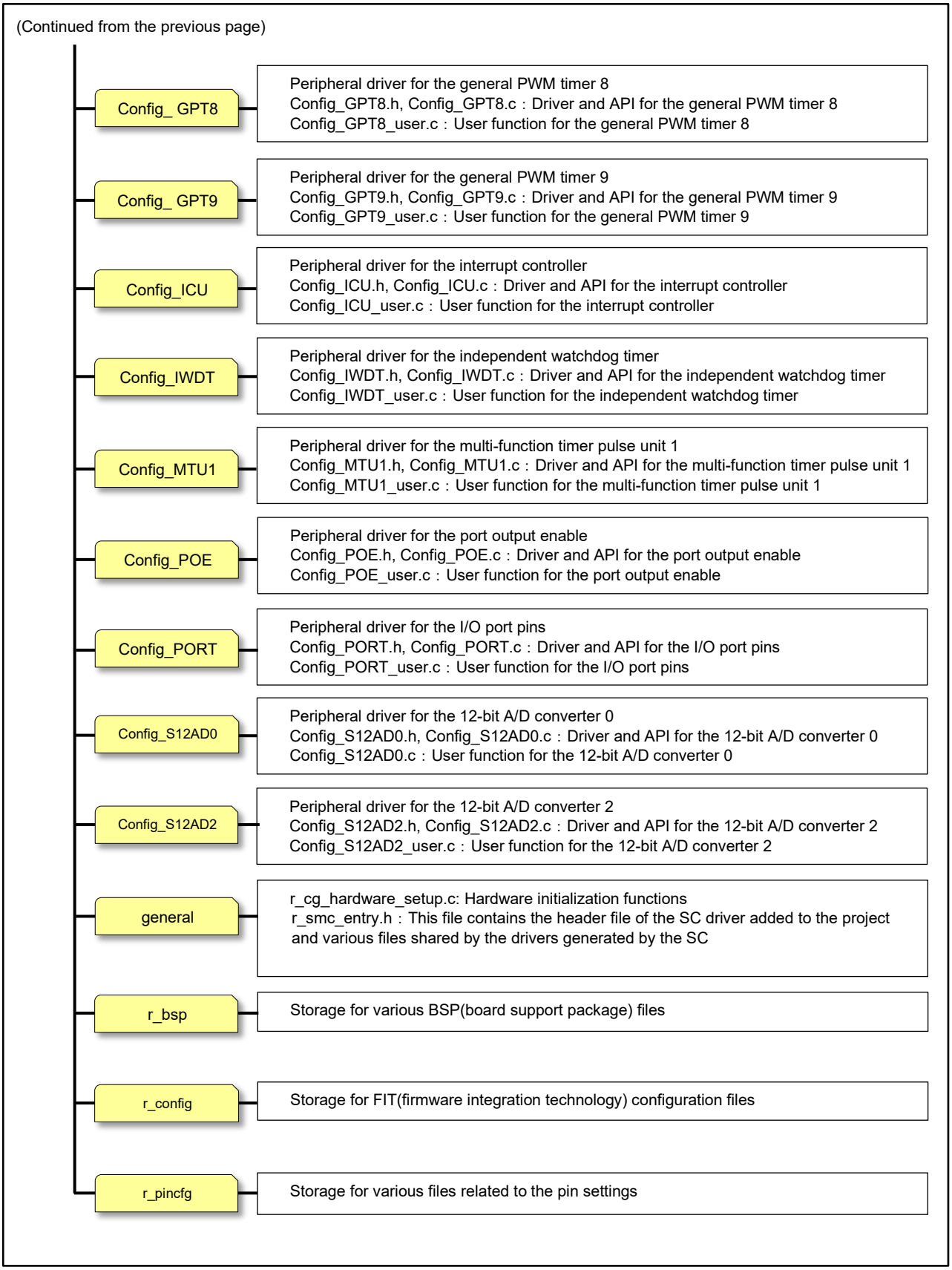


Figure 2-4 Configuration of Folders and Files from the Smart Configurator (2/2)

2.4.3 Module Configuration

Figure 2-5 shows the configuration of the software modules.

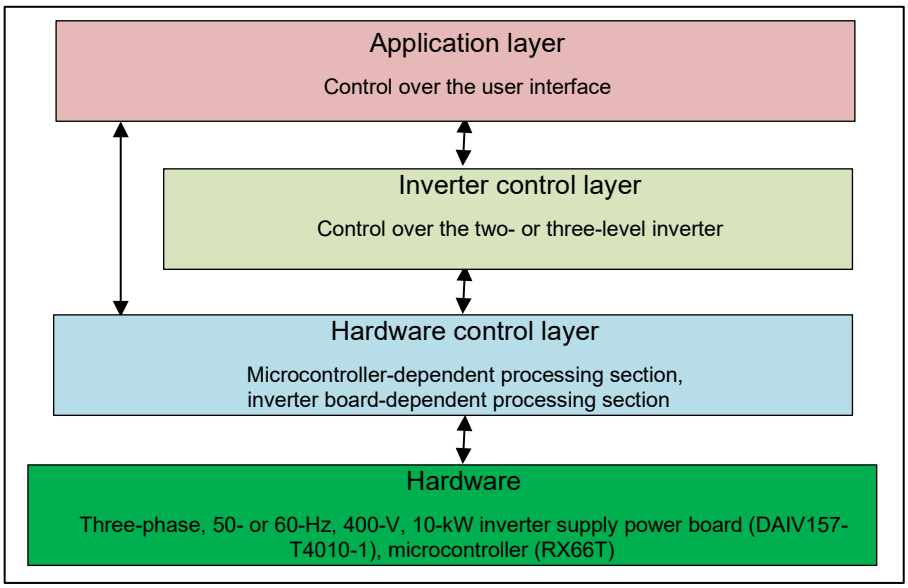


Figure 2-5 Module Configuration

3. Details of the Control Software

This section describes the target software of this application note.

3.1 Details of Control

3.1.1 Starting and Stopping Inverter Output

Input from the operation switch (SW4) is used to control starting and stopping of inverter output.

A general-purpose port pin is assigned to the operation switch (SW4). The MCU determines whether to start or stop inverter output by reading the level on the pin every 10 ms in the main loop of the program. Specifically, driving the pin low or high starts or stops inverter output, respectively.

3.1.2 Switching the Mode

Input from the mode switching switch (SW5) is used to control switching of the mode.

A general-purpose port pin is assigned to the mode switching switch (SW5). The MCU determines the mode by reading the level on the pin only once at the time power is supplied. Specifically, driving the pin low or high selects two- or three-level operation, respectively.

3.1.3 Switching the Frequency

Input from the frequency switching switch (SW3) is used to control switching of the frequency.

A general-purpose port pin is assigned to the frequency switching switch (SW3). The MCU determines the frequency by reading the level on the pin every 10 ms in the main loop of the program. Specifically, driving the pin low or high selects 60 Hz or 50 Hz as the inverter output frequency, respectively.

This operation is only possible while inverter output is stopped.

3.1.4 Changing the Switching Frequency during Operation

Inputs from the mid-operation carrier frequency encoder (RE1) are used to control the switching frequency during operation.

Rotary encoder output signals A and B from the mid-operation carrier frequency encoder (RE1) are changed as shown in Figure 3-1.The phase counting mode of the MTU is used in calculating transitions of the pulse signals. A clockwise change for one pulse cycle during inverter output operation makes the switching frequency higher by 0.1 kHz. On the other hand, a counter-clockwise change for one pulse cycle makes the switching frequency lower by 0.1 kHz.

This operation is only possible during inverter output operation.

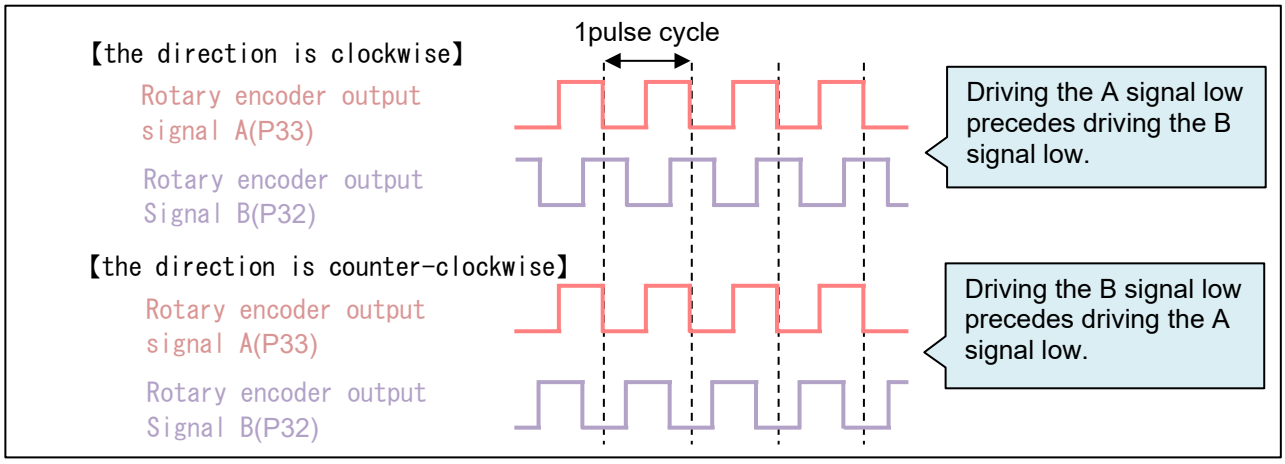


Figure 3-1 Output Signals of the Mid-Operation Carrier Frequency Encoder

3.1.5 Release from the Alarm State

Input from the reset button switch (SW2) is used to control release from the alarm state.

A general-purpose port pin is assigned to the reset button switch (SW2). The MCU reads the level on the pin every 10 ms in the main loop of the program. Changing the level on the pin in the order high to low (for at least 100 ms), and then high, requests release from the alarm state.

3.1.6 A/D Conversion

(1) Detecting Output Currents of the U, V and W Phases

AC output currents of the U, V, and W phases are measured as listed in Table 3-1.

Table 3-1 Conversion Ratio for Currents of the U, V, and W Phases

Item	Conversion Ratio (Results of A/D Conversion for Output Currents of the U, V, and W Phases)	Channel
Output currents of the U, V, and W phases	-62.515 A to 62.485 A: 0000H to 0FFFH	Iu: AN000 Iv: AN001 Iw: AN002

(2) Detecting Output Voltages of the U, V and W Phases

AC output voltages of the U, V, and W phases are measured relative to the neutral point as listed in Table 3-2.

Table 3-2 Conversion Ratio for Voltages of the U, V, and W Phases

Item	Conversion Ratio (Results of A/D Conversion for Output Voltages of the U, V, and W Phases)	Channel
Output voltages of the U, V, and W phases	-633.066 V to 632.757 V: 0000H to 0FFFH	Vu: AN200 Vv: AN201 Vw: AN202

(3) Detecting DC Voltages

The positive voltage of the DC input is measured relative to the negative voltage as indicated in Table 3-3.

Table 3-3 Conversion Ratio for DC Input Voltages

Item	Conversion Ratio (Results of A/D Conversion for DC Input Voltages)	Channel
DC input voltages	0 V to 1315.789 V: 0000H to 0FFFH	AN208

(4) Initial Switching Frequency

The initial switching frequency is determined by A/D converting the value of the initial carrier frequency volume controller (VR4). The value produced by A/D conversion of the voltage from VR4 is used to determine the initial switching frequency as shown in the Figure 3-2.

This operation is only possible while inverter output is stopped.

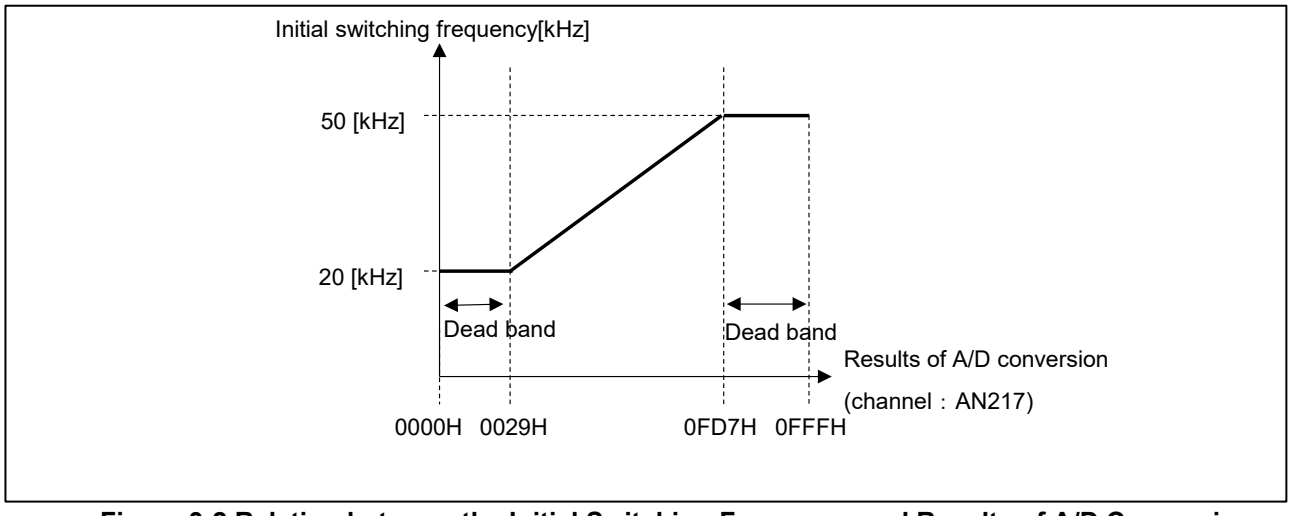


Figure 3-2 Relation between the Initial Switching Frequency and Results of A/D Conversion

3.1.7 Modulation

The target software of this application note generates pulse width modulated (PWM) waveforms to obtain the AC output voltage set by the two- or three-level inverter power supply system.

The ratio of the voltage output pulse to the carrier wave is referred to as the duty cycle and is shown in Figure 3-3.

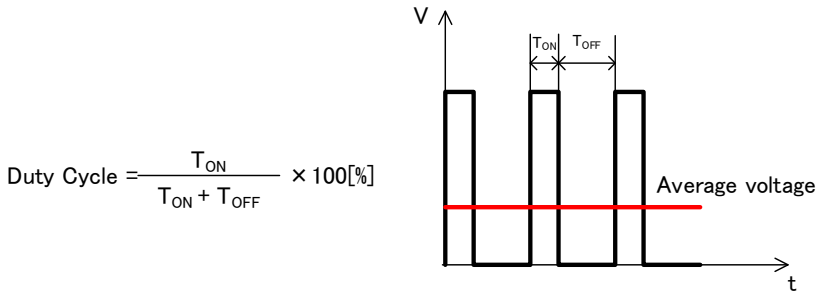


Figure 3-3 Definition of the Duty Cycle

In addition, the modulation depth m is defined as follows:

$$m = \frac{V}{E/2}$$

m: Modulation ratio V: Voltage command value E: DC input voltage

PWM waveforms for two- or three-level operation are generated based on the modulation ratio.

(1) Two-Level Operation

Figure 3-4 shows the concept of generating PWM waveforms during two-level operation.

The duty cycle is determined by comparing the modulation ratio and the amplitude of the carrier wave. Specifically, when the modulation ratio is larger or smaller than the amplitude of the carrier wave, a high-side gate is turned on or off, respectively. Behavior of the low-side gate is complementary to that of the high-side gate. In two-level operation, neutral gates 1 and 2 are not used so are left off.

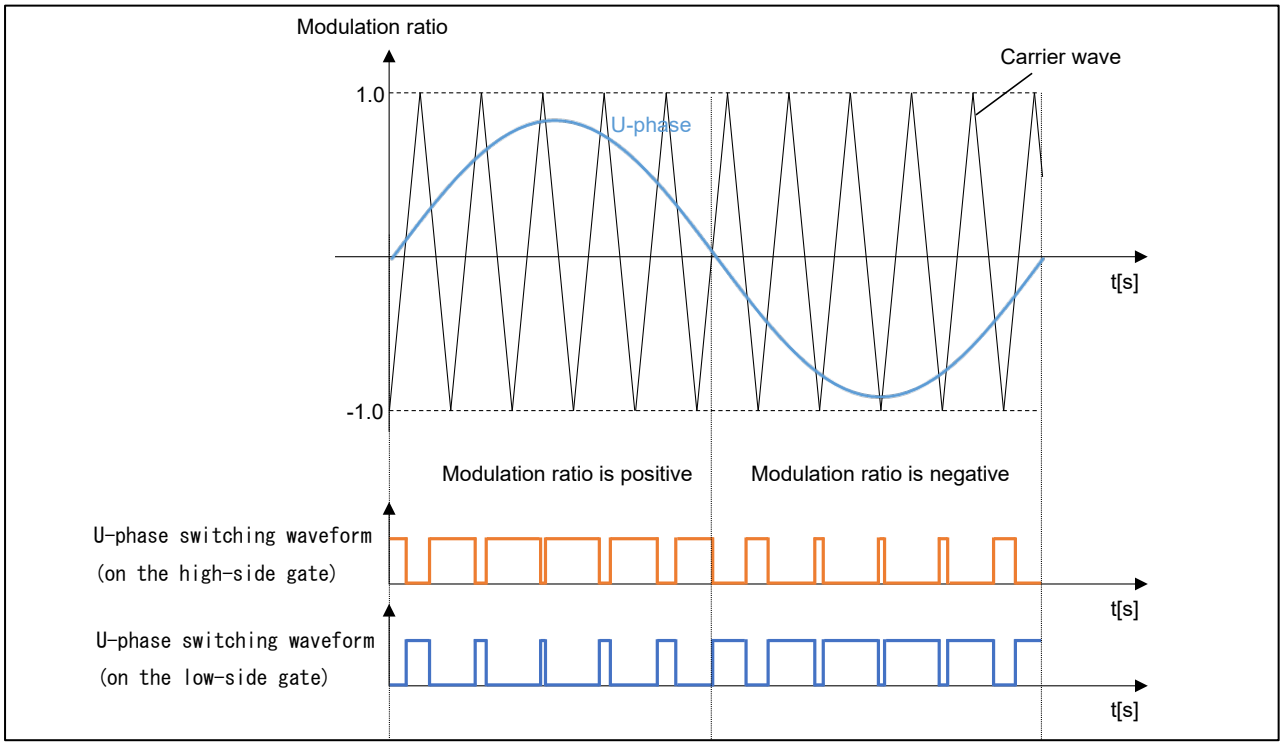


Figure 3-4 Concept of Generating PWM Waveforms during Two-Level Operation

(2) Three-Level Operation

Figure 3-5 shows the concept of generating PWM waveforms during three-level operation.

The duty cycle is determined by comparing the high- or low-side modulation ratio and the amplitude of the carrier wave. The high- and low-side modulation ratio can be calculated from the following expressions.

$$①1.0 \geq \text{Modulation ratio} \geq 0.0(\text{the modulation ratio is positive})$$
$$\text{High side modulation ratio} = 1.0 - \text{modulation ratio} \times 2、\text{Low side modulation ratio} = -1.0$$
$$②-1.0 \leq \text{Modulation ratio} < 0.0(\text{the modulation ratio is negative})$$
$$\text{High side modulation ratio} = 1.0、\text{Low side modulation ratio} = -1.0 - \text{modulation ratio} \times 2$$

For a positive modulation ratio, when the high-side modulation ratio is smaller or larger than the amplitude of the carrier wave, the high-side gate is turned on or off, respectively. The behavior of neutral gate 1 is complementary to that of the high-side gate. The low-side gate is fixed to off and neutral gate 2 is fixed to on.

For a negative modulation ratio, when the low-side modulation ratio is larger or smaller than the amplitude of the carrier wave, the low-side gate is turned on or off, respectively. The behavior of neutral gate 2 is complementary to that of the low-side gate. The high-side gate is fixed to off and neutral gate 1 is fixed to on.

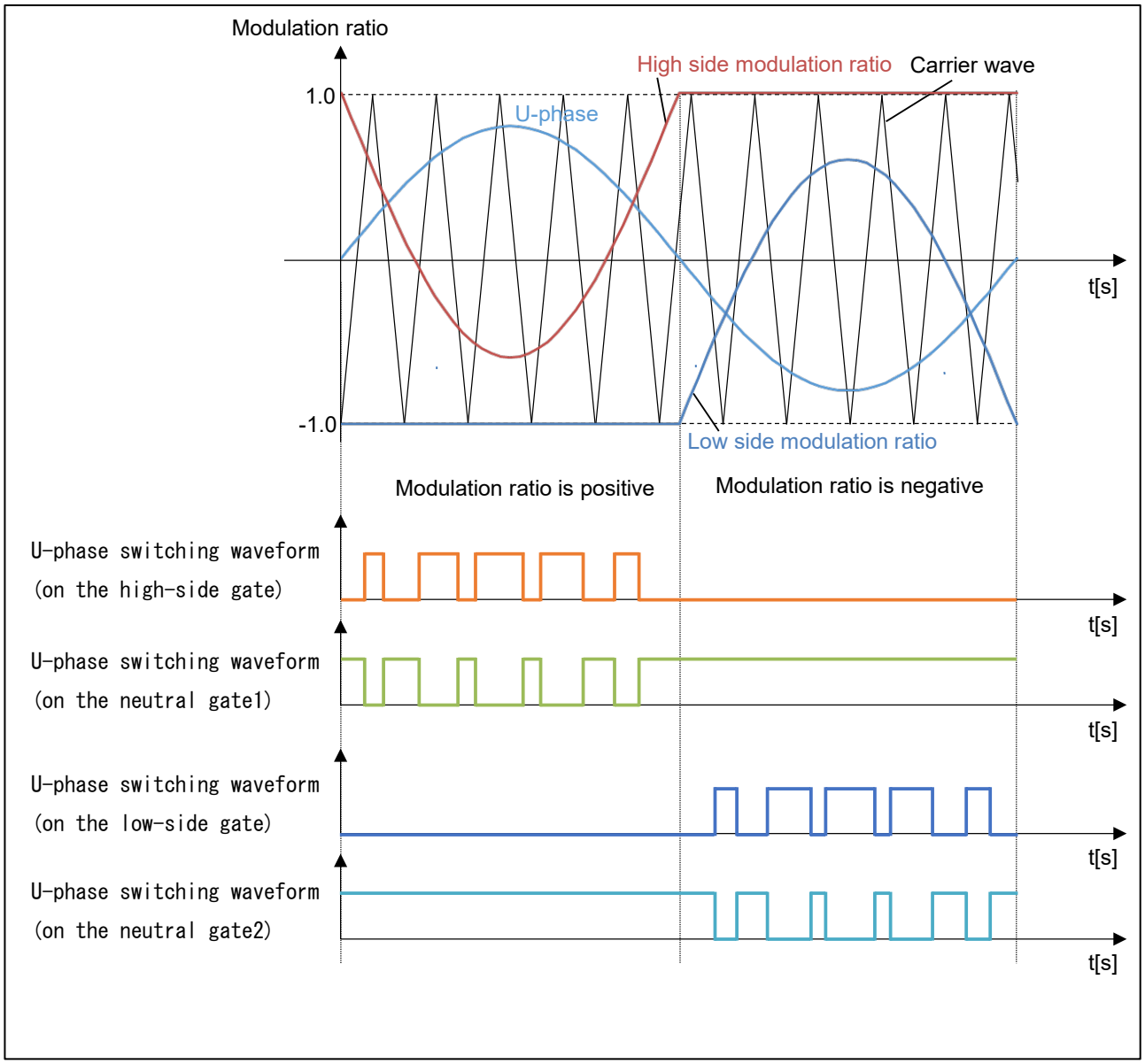


Figure 3-5 Concept of Generating PWM Waveforms during Three-Level Operation

3.1.8 State Transitions

Figures below shows state transitions of the target software of this application note. The software manages the states of operation and alarm states.

(1) States of Operation

Here, “states of operation” indicate the state of inverter output. State transitions proceed in response to conditions as shown in Figure 3-6. The states of operation are “RUN” and “STOP”.

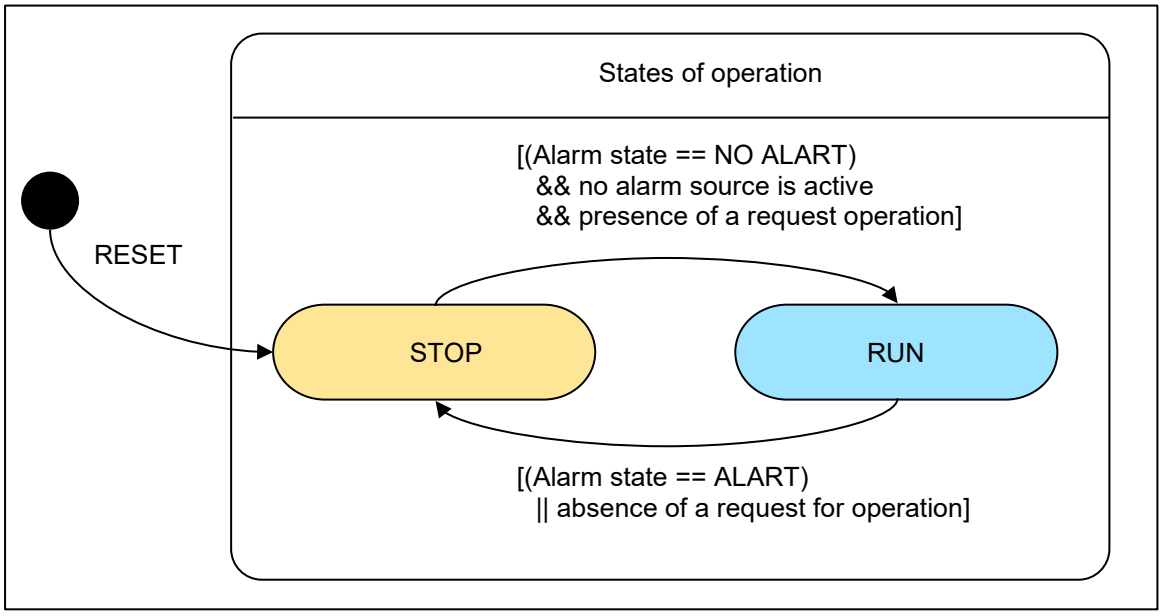


Figure 3-6 Transitions in the State of Operation

(2) Alarm States

The alarm states indicate the state of the software. State transitions proceed in response to conditions as shown in Figure 3-7. The alarm states are “ALART” (an alarm is being generated) and “NO ALART” (no alarm is being generated).

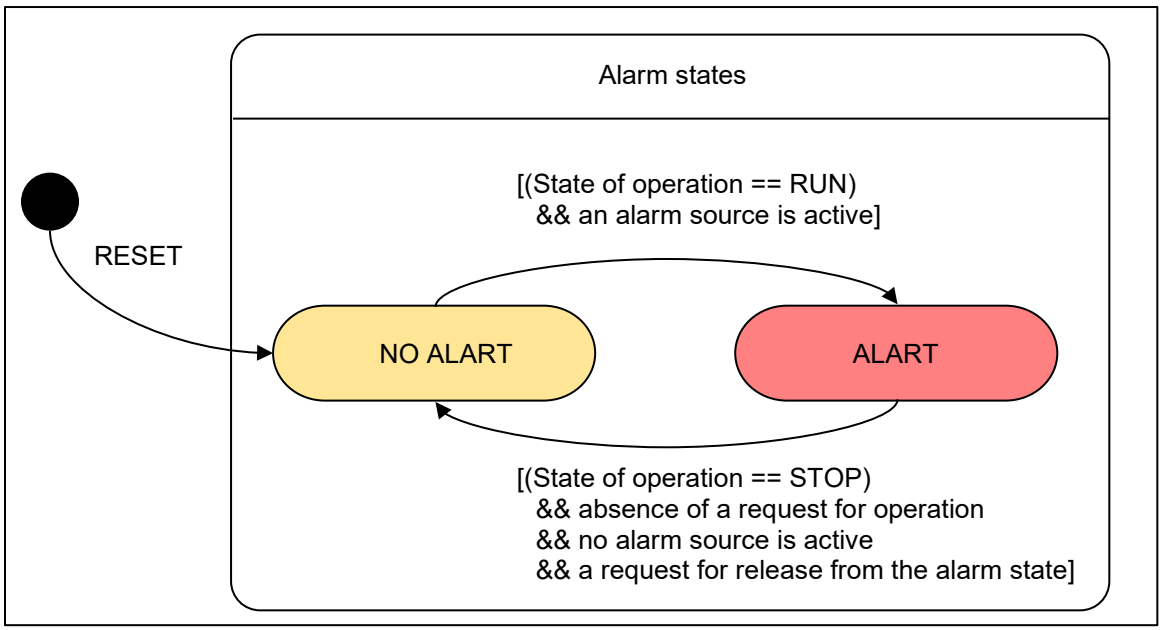


Figure 3-7 Transitions in the Alarm State

3.1.9 Soft Start

On transitions of the state of operation from “STOP” to “RUN”, the internal target voltage changes until the voltage reaches the set target voltage as shown in Figure 3-8. The INV_TARGET_SLEWRATE macro (transition rate of the target voltage in a soft start) is used for the slew rate.

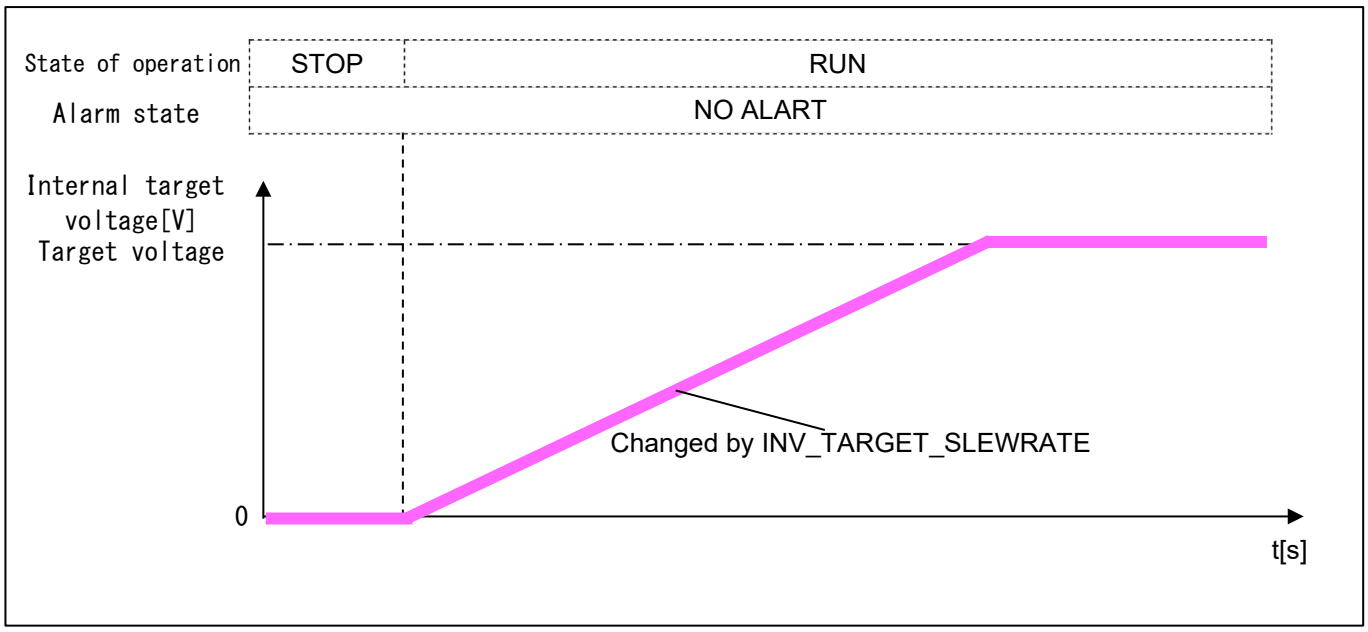


Figure 3-8 Inverter Output in a Soft Start

3.1.10 System Protection

The target software of this application note has the following protection functions.

Table 3-4 lists values to be set for system protection.

(1) Output Overvoltage or Output Overcurrent Error

When the output overvoltage or output overcurrent detection signal from the hardware goes to the low level (to indicate an error), this function stops the gate outputs.

The function sets an alarm source to “yes” and the operation request to “no” in response to the error.

(2) Gate Driver Error

When the FET gate driver error detection signal from the hardware goes to the low level (to indicate an error), this function stops the gate outputs.
The function sets an alarm source to “yes” and the operation request to “no” in response to the error.

(3) Temperature Error

When the SiC FET temperature error detection signal from the hardware goes to the low level (to indicate an error), this function stops the gate outputs.
The function sets an alarm source to “yes” and the operation request to “no” in response to the error.

(4) Temporary Stop Due to an Input Undervoltage

This function monitors the input voltage at the monitoring interval. When the input voltage falls below the judgment threshold value for a temporary stop due to an input undervoltage, the function temporarily stops the gate outputs. The function restarts the gate outputs when the input voltage goes beyond the threshold value for release from a temporary stop due to an input undervoltage.

(5) Input Overvoltage Error

This function monitors the input voltage at the monitoring interval. When the input voltage goes beyond the judgment threshold value for an input overvoltage error, the function stops the gate outputs.
The function sets an alarm source to “yes” and the operation request to “no” in response to the error.

(6) Output Undervoltage Error

This function monitors the effective values of the U-, V-, and W-phase AC output voltages at the monitoring interval. When an effective value continues to be below the judgment threshold value for an output undervoltage error during the judgment delay time for an output undervoltage error, the function stops the gate outputs. The delay time is counted in common for whichever of the U, V, and W phases have effective values below the threshold.
The function sets an alarm source to “yes” and the operation request to “no” in response to the error.

(7) Temporary Stop Due to an Output Overvoltage

This function monitors the U-, V-, and W-phase AC output voltages at the monitoring interval. When an output voltage goes beyond the judgment threshold value for a temporary stop due to an output overvoltage, the function temporarily stops the gate outputs. The function restarts the gate outputs when the AC output voltage falls below the threshold value for release from a temporary stop due to an output overvoltage.

(8) Output Overvoltage Error

This function monitors the U-, V-, and W-phase AC output voltages at the monitoring interval. When an output voltage goes beyond the judgment threshold value for an output overvoltage error, the function stops the gate outputs.
The function sets an alarm source to “yes” and the operation request to “no” in response to the error.

(9) Voltage Dropping Due to an Output Overcurrent

This function monitors the effective values of the U-, V-, and W-phase AC output currents at the monitoring interval. When an effective value goes beyond the threshold value for judging that voltage will drop due to an output overcurrent, the function controls the current by adjusting the voltage command value for the given phase. The control processing makes the current fall below the threshold value for release from the state of a voltage drop due to an output overcurrent, after which the function stops applying the control.

(10) Output Overcurrent Error

This function monitors the effective values of the U-, V-, and W-phase AC output currents at the monitoring interval. When an effective value goes beyond the judgment threshold value for an output overcurrent error, the function stops the gate outputs.
The function sets an alarm source to “yes” and the operation request to “no” in response to the error.

Table 3-4 Values to be Set for System Protection

Type of Protection	Item	Value to be Set
Output overvoltage or output overcurrent error	Monitoring interval [µs]	50
Gate driver error	Monitoring interval [µs]	50
Temperature error	Monitoring interval [ms]	10
Temporary stop due to an input undervoltage	Judgment threshold value for a temporary stop due to an input undervoltage [V]	INV_VIN_LOW_DET macro
	Threshold value for release from a temporary stop due to an input undervoltage [V]	INV_VIN_LOW_REL macro
	Monitoring interval [µs]	50
Input overvoltage error	Judgment threshold value for an input overvoltage error [V]	INV_VIN_OVP_DET macro
	Monitoring interval [µs]	50
Output undervoltage error	Judgment threshold value for an output undervoltage error [V]	INV_VOUT_LOW_DET macro
	Judgment delay time for an output undervoltage error [s]	INV_VOUT_LOW_DELAY macro
	Monitoring interval [ms]	10
Temporary stop due to an output overvoltage	Judgment threshold value for a temporary stop due to an output overvoltage [V]	INV_VOUT_HIGH_DET macro
	Threshold value for release from a temporary stop due to an output overvoltage [V]	INV_VOUT_HIGH_REL macro
	Monitoring interval [µs]	50
Output overvoltage error	Judgment threshold value for an output overvoltage error [V]	INV_VOUT_OVP_DET macro
	Monitoring interval [µs]	50
Voltage dropping due to an output overcurrent	Threshold value for judging that voltage will drop due to an output overcurrent [A]	INV_IOUT_HIGH_DET macro
	Threshold value for release from the state of a voltage drop due to an output overcurrent [A]	INV_IOUT_HIGH_REL macro
	Monitoring interval [µs]	50
Output overcurrent error	Judgment threshold value for an output overcurrent error [A]	INV_IOUT_OCP_DET macro
	Monitoring interval [µs]	50

3.2 Functional Specifications of the Two- or Three-Level Inverter Control Software

The control processing of the target software of this application note is driven by the following three interrupts: low-speed timer (1-ms-periodic), high-speed timer (50-µs-periodic), and switching period timer interrupts.

Figure 3-9 is a schematic view of the control over a two- or three-level inverter. For the 1-ms-periodic process, the low-speed timer interrupt processing is used to manage the 1-ms lapse event flag. The 1-ms-periodic process is executed in the main process.

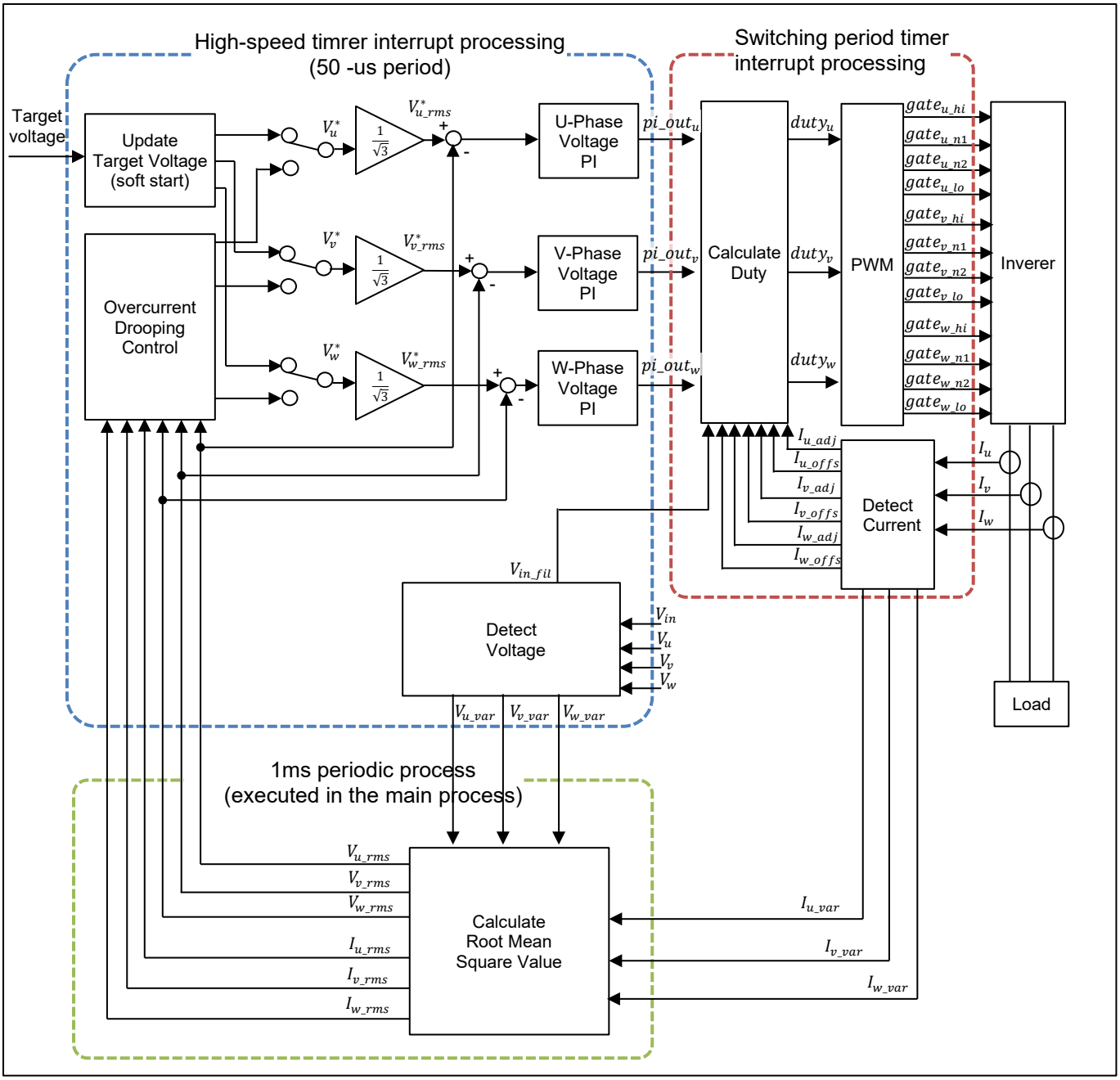


Figure 3-9 Schematic View of the Control over a Two- or Three-Level Inverter

The body of this subsection consists of Table 3-5 to Table 3-9, which give summaries of the specifications of the three interrupt functions and functions executed in the main process. Note that the tables only cover the primary functions for use in control over the two- or three-level inverter. For details on functions not listed in the tables, refer to the source code.

Table 3-5 List of Interrupt Functions

File Name	Outline of Function	Outline of Processing
Config_CMT0_user.c	r_Config_CMT0_cmi0_interrupt Input: None Output: None	Called every 1 ms ▪ Low-speed timer interrupt processing (the r_inv_slow_int_proc function)
Config_CMT1_user.c	r_Config_CMT1_cmi1_interrupt Input: None Output: None	Called every 50 µs ▪ High-speed timer interrupt processing (the r_inv_dsp_int_proc function)
Config_S12AD0_user.c	r_Config_S12AD0_interrupt Input: None Output: None	Called every PWM period ▪ Switching period timer interrupt processing (the r_inv_pwm_int_proc function)

Table 3-6 List of Functions Executed in the Low-Speed Timer Interrupt Processing

File Name	Outline of Function	Outline of Processing
r_inv_main.c	r_inv_slow_int_proc Input: None Output: None	Low-speed timer interrupt processing

Table 3-7 List of Functions Executed in the High-Speed Timer Interrupt Processing (1/2)

File Name	Outline of Function	Outline of Processing
r_inv_smps_ctrl.c	r_inv_dsp_int_proc Input: None Output: None	High-speed timer interrupt processing ▪ Voltage detection processing ▪ System protection monitoring processing ▪ Inverter output stop processing, inverter output temporary stop processing, or inverter output processing ▪ Mean-square operations for the U-, V-. and W-phase voltages ▪ Mean-square operations for the U-, V-. and W-phase currents
	r_inv_smps_update_observer Input: None Output: None	System protection monitoring processing
	r_inv_smps_dsp_stop Input: None Output: None	Inverter output stop processing
	r_inv_smps_dsp_standby Input: None Output: None	Inverter output temporary stop processing
	r_inv_smps_dsp_active Input: None Output: None	Inverter output processing ▪ Overcurrent voltage-drop control ▪ Updating the target voltage ▪ PI control over the U-, V-, and W-phase voltages
	r_inv_smps_update_target Input: (float) f4_old / Target voltage (before updating) Output: (float) f4_new / Target voltage (after updating)	Updating the target voltage (in soft start processing)
	r_inv_absmax_3val Input: (float) vout_u_adj / Numerical value 1 (float) vout_v_adj / Numerical value 2 (float) vout_w_adj / Numerical value 3 Output: (float) abs_max / Maximum absolute value among values	Getting the maximum absolute value among values
	r_inv_macro_calc_var Input: (float) a / Previous value of the result of mean-square operation (float) b / Input value Output: (float) calc_answer / Result of mean-square operation	Mean-square operation
	r_inv_smps_request_stop Input: None Output: None	Request to stop inverter output
	r_inv_smps_request_standby Input: None Output: None	Request to temporarily stop inverter output
	r_inv_smps_req_immediate_end Input: None Output: None	Request for emergency ending inverter output

Table 3-7 List of Functions Executed in the High-Speed Timer Interrupt Processing (2/2)

Config_S12AD2_user.c	r_inv_get_adc_vout_u_phase Input: None Output: (uint16_t) data / A/D converted U-phase output voltage	Getting the A/D converted U-phase output voltage
	r_inv_get_adc_vout_v_phase Input: None Output: (uint16_t) data / A/D converted V-phase output voltage	Getting the A/D converted V-phase output voltage
	r_inv_get_adc_vout_w_phase Input: None Output: (uint16_t) data / A/D converted W-phase output voltage	Getting the A/D converted W-phase output voltage
	r_inv_get_adc_vin_dc Input: None Output: (uint16_t) data / A/D converted input voltage	Getting the A/D converted input voltage
Config_PORT_user.c	r_inv_get_ovpocpb_status Input: None Output: (uint8_t) ret / Getting the state in terms of output overvoltage or output overcurrent detection	Getting the state in terms of output overvoltage or output overcurrent detection
	r_inv_get_gatedrvb_status Input: None Output: (uint8_t) ret / State in terms of detecting a gate driver error	Getting the state in terms of detecting a gate driver error
Config_GPT4_user.c	r_inv_pwm_enable_output Input: None Output: None	Enabling PWM output
	r_inv_pwm_disable_output Input: None Output: None	Disabling PWM output

Table 3-8 List of Functions Executed in the Switching Period Timer Interrupt Processing

File Name	Outline of Function	Outline of Processing
r_inv_smps_ctrl.c	r_inv_pwm_int_proc Input: None Output: None	Switching period timer interrupt processing ▪ Current detection processing ▪ Calculating the duty cycle while inverter output is stopped or calculating the duty cycle ▪ Setting the output duty cycles
	r_inv_smps_switch_stop Input: None Output: None	Calculating the duty cycle while inverter output is stopped
Config_S12AD0_user.c	r_inv_get_adc_iout_u_phase Input: None Output: (uint16_t) data / A/D converted U-phase current	Getting the A/D converted U-phase current
	r_inv_get_adc_iout_v_phase Input: None Output: (uint16_t) data / A/D converted V-phase current	Getting the A/D converted V-phase current
	r_inv_get_adc_iout_w_phase Input: None Output: (uint16_t) data / A/D converted W-phase current	Getting the A/D converted W-phase current
r_inv_smps_switch_active.c	r_inv_smps_switch_active Input: None Output: None	Calculating the duty cycle
	r_inv_sinf Input: (float) f4_phase / Phase Output: (float) f4_sin / Calculated sine value	Sine calculation
Config_CMT2_user.c	r_inv_ac_get_phase Input: None Output: (float) f4_phase / Phase	Getting the voltage phase of the U-phase output
Config_GPT4_user.c	r_inv_pwm_set_onduty Input: (float) f4_duty_u / U-phase duty cycle (float) f4_duty_v / V-phase duty cycle (float) f4_duty_w / W-phase duty cycle Output: None	Setting the output duty cycles

Table 3-9 List of Functions Executed in the Main Process

File Name	Outline of Function	Outline of Processing
r_inv_main.c	main Input: None Output: None	Main Process ▪ Initializing the software ▪ Clearing the watchdog timer ▪ Low-speed periodic process
	r_inv_normal_proc Input: None Output: None	Low-speed periodic process ▪ 1-ms-periodic process ▪ 10-ms-periodic process ▪ 100-ms-periodic process
r_inv_proc_ctrl.c	r_inv_init_proc Input: None Output: None	Initializing the software ▪ Initializing the state ▪ Starting signal detection by the rotary encoder
r_inv_proc_ctrl.c	r_inv_1ms_cycle_proc Input: None Output: None	1-ms-periodic process
r_inv_proc_ctrl.c	r_inv_10ms_cycle_proc Input: None Output: None	10-ms-periodic process
r_inv_proc_ctrl.c	r_inv_100ms_cycle_proc Input: None Output: None	100-ms-periodic process
r_inv_smps_ctrl.c	r_inv_smps_init_proc Input: (*st_smps_if_v1_t) smps_if / Initial state value Output: None	Initializing the state
Config_MTU1_user.c	r_inv_rotenc_start_timer Input: None Output: None	Starting signal detection by the rotary encoder
Config_IWDT.c	R_Config_IWDT_Restart Input: None Output: None	Clearing the watchdog timer

3.3 Macro Definitions of the Two- or Three-Level Inverter Control Software

Macro definitions used in the target software of this application note are listed in Table 3-10. Note that the table only covers the macro definitions for use in setting the software configuration. For details on macro definitions not listed in the table, refer to the source code.

Table 3-10 List of Macro Definitions in r_inv_targetdef.h

File Name	Macro Name	Definition Value	Remarks
r_inv_targetdef.h	SQRT2	1.41421356237310f	Square root of two
	SQRT3	1.73205080756888f	Square root of three
	DSPSMPLCLK	20.0e + 3f	Sampling frequency [Hz]
	INV_VOUT_GAIN	0.00395f	Gain for output voltage detection (analog input voltage/actual voltage)
	INV_IOUT_GAIN	0.04f	Gain for output current detection (analog input voltage/actual current)
	INV_VIN_GAIN	0.0038f	Gain for input voltage detection (analog input voltage/actual voltage)
	INV_VIN_LOW_DET	600.0f * 0.85f	Judgment threshold value for a temporary stop due to an input undervoltage [V]
	INV_VIN_LOW_REL	600.0f * 0.95f	Threshold value for release from a temporary stop due to an input undervoltage [V]
	INV_VIN_OVP_DET	850.0f * 1.10f	Judgment threshold value for an input overvoltage error [V]
	INV_VOUT_LOW_DET	400.0f / SQRT3 * 0.85f	Judgment threshold value for an output undervoltage error (as an effective value of the phase voltage) [V]
	INV_VOUT_LOW_DELAY	2.0f	Judgment delay time for an output undervoltage error [s]
	INV_VOUT_HIGH_DET	400.0f / SQRT3 * 1.10f * SQRT2	Judgment threshold value for a temporary stop due to an output overvoltage (as an instantaneous value of the phase voltage) [V]
	INV_VOUT_HIGH_REL	400.0f / SQRT3 * 1.01f * SQRT2	Threshold value for release from a temporary stop due to an output overvoltage (as an instantaneous value of the phase voltage) [V]
	INV_VOUT_OVP_DET	400.0f / SQRT3 * 1.15f * SQRT2	Judgment threshold value for an output overcurrent error (as an instantaneous value of the phase voltage) [V]
	INV_IOUT_HIGH_DET	18.0f * 1.10f	Threshold value for judging that voltage will drop due to an output overcurrent (as an effective value of the phase current) [A]
	INV_IOUT_HIGH_REL	18.0f * 1.01f	Threshold value for release from the state of a voltage drop due to an output overcurrent (as an effective value of the phase current) [A]
	INV_IOUT_HIGH_COEF	0.01f / 1.0f	Current drop coefficient (duty cycle/effective value of the phase current)

	INV_IOUT_OCP_DET	18.0f * 1.20f * SQRT2	Judgment threshold value for an output overcurrent error (as an instantaneous value of the phase current) [A]
	INV_TARGET_VOLTAGE	400.0f	Target output voltage (as an effective value of the line voltage) [V]
	INV_TARGET_SLEWRATE	INV_TARGET_VOLTAGE / 0.60f	Transition rate of the target voltage in a soft start [V/s]
	INV_PIC_COEF_PAR	5.0f / INV_TARGET_VOLTAGE	Proportional coefficient for use in PI control
	INV_PIC_COEF_INT	5.0f / INV_TARGET_VOLTAGE / DSPSMPLCLK	Integral coefficient for use in PI control
	INV_DUTY_CMPL_COEF	0.00f / 1.0f	Duty cycle correction coefficient by current (duty cycle/instantaneous value of the phase current)
	INV_PWM_DEAD_TIME	200.0f	Dead time [ns]
	INV_PWM_FREQ_MAX	50000.0f	Upper limit of the switching frequency [Hz]
	INV_PWM_FREQ_MIN	20000.0f	Lower limit of the switching frequency [Hz]

3.4 Control Flowcharts

3.4.1 Main Process

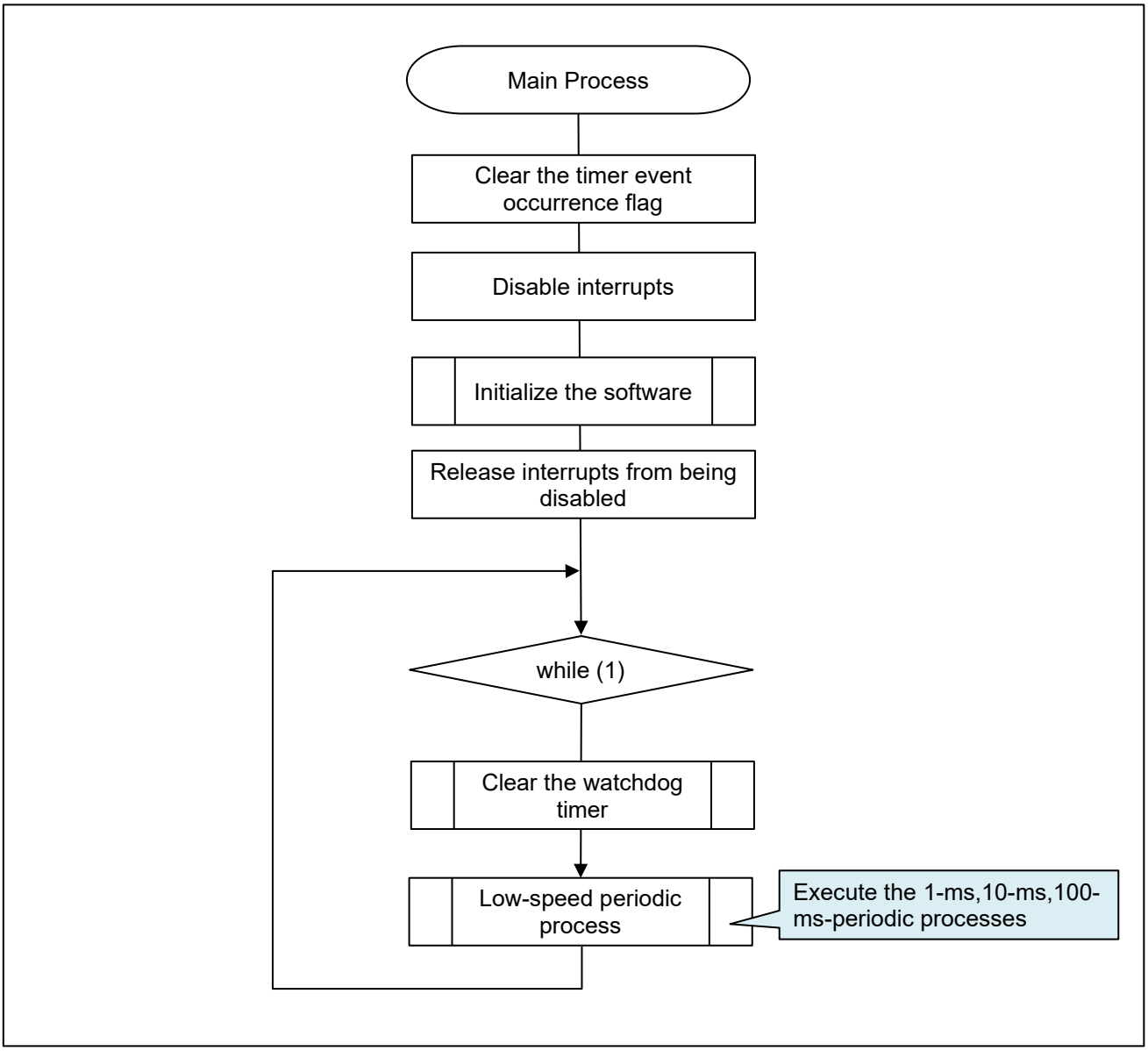


Figure 3-10 Flowchart of the Main Process

3.4.2 Low-Speed Timer Interrupt Processing (1-ms Period)

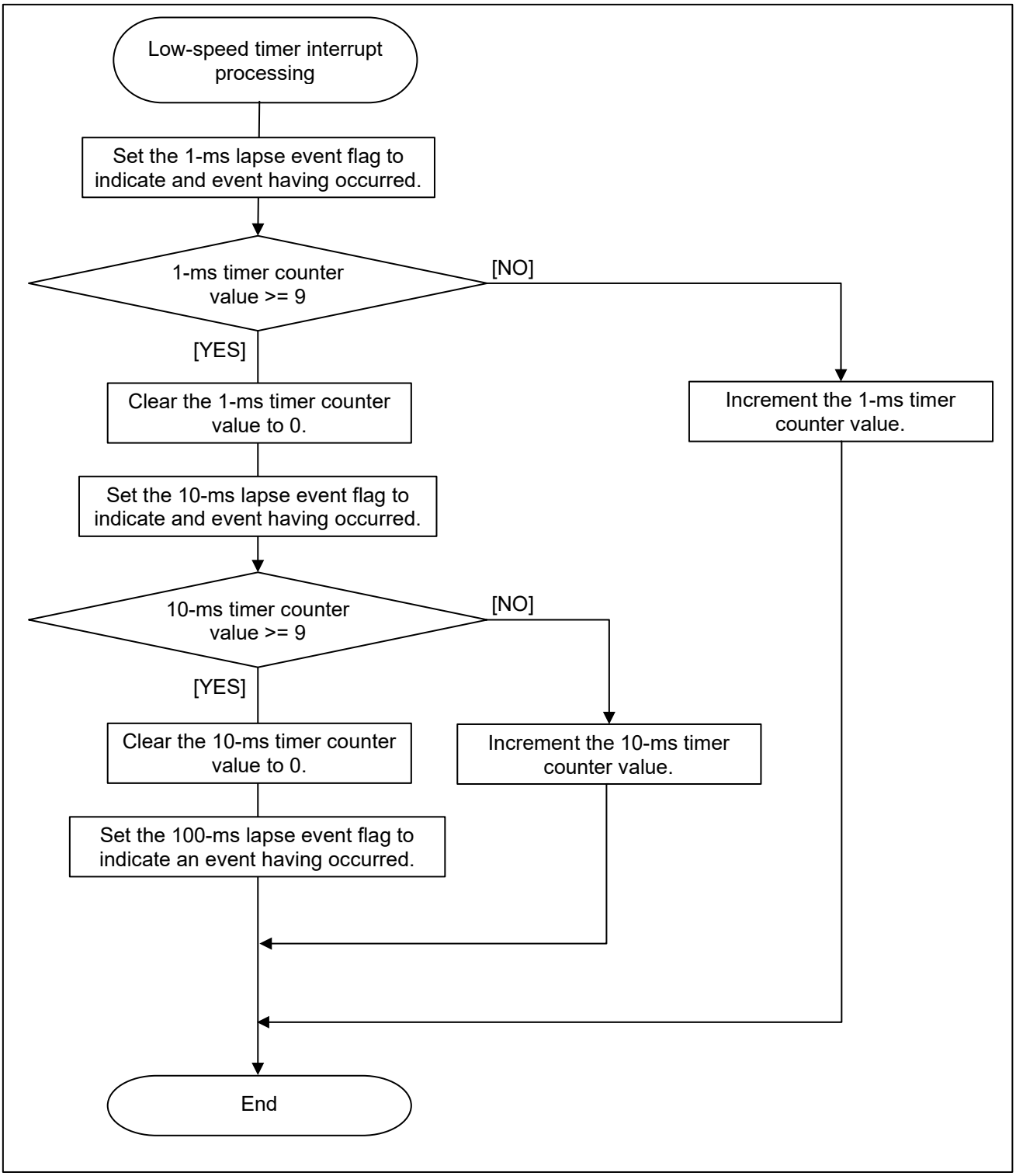


Figure 3-11 Flowchart of the Low-Speed Timer Interrupt Processing

3.4.3 High-Speed Timer Interrupt Processing (50-µs Period)

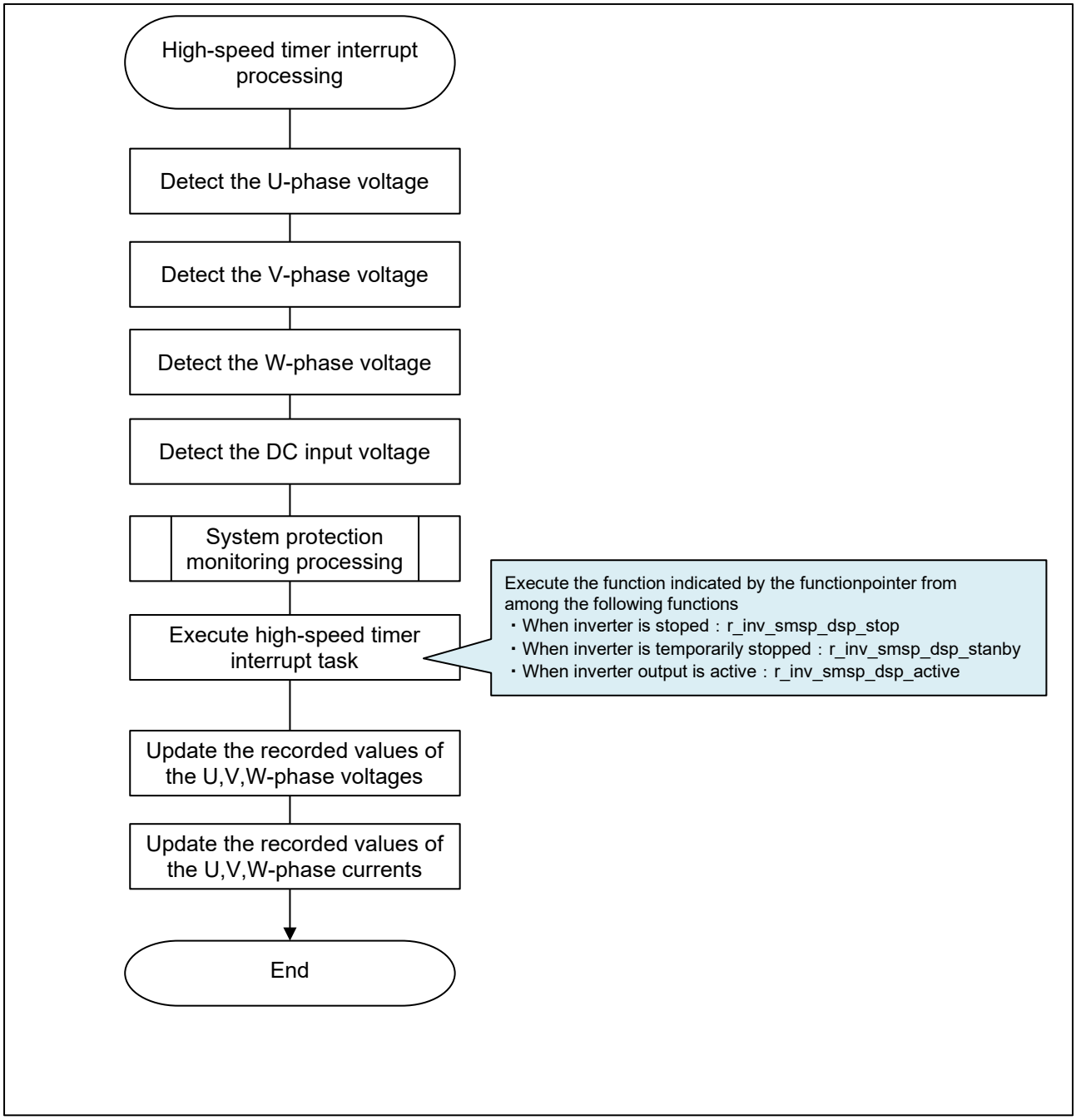


Figure 3-12 Flowchart of the High-Speed Timer Interrupt Processing

3.4.4 Switching Period Timer Interrupt Processing

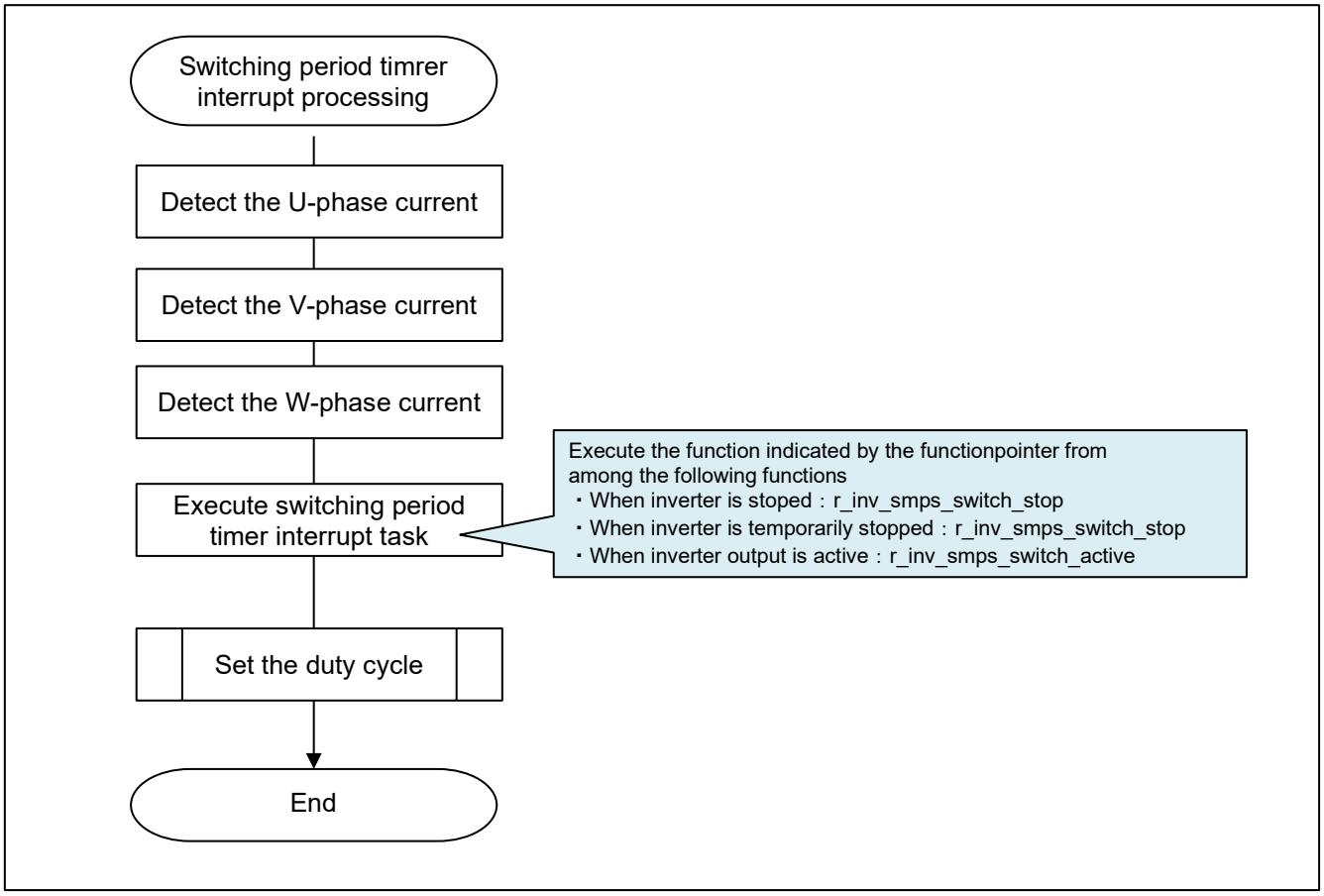


Figure 3-13 Flowchart of the Switching Period Timer Interrupt Processing

4. Motor Control Development Support Tool: Renesas Motor Workbench

4.1 Overview

The Renesas Motor Workbench, a motor control development support tool, can be used as a state monitor for the target software of this application note. For details on variables that the Renesas Motor Workbench can monitor, refer to 4.2, List of Variables for Analysis. In addition, refer to the Renesas Motor Workbench User's Manual for details on usage and other points. The Renesas Motor Workbench can be downloaded from our Web site.

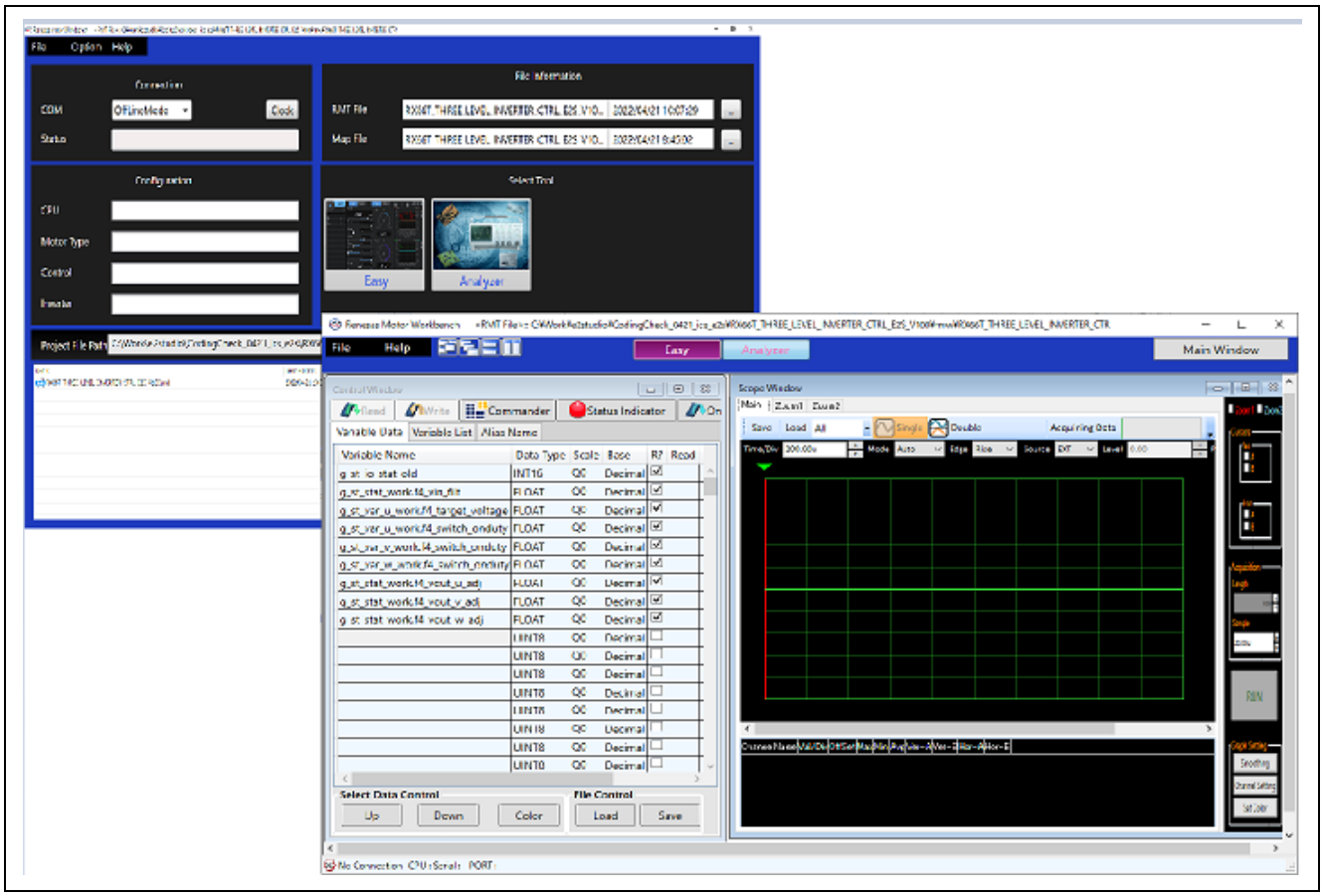


Figure 4-1 Windows of the Renesas Motor Workbench

How to use the Renesas Motor Workbench, a motor control development support tool

(1) Start the Renesas Motor Workbench by clicking on this icon. 

(2) Click on [File] and select [Open RMT File(O)] from the drop-down menu.
Select the RMT file from the following location under the e^2 studio or CS+ project folder.
'[Project Folder]/application/user_interface/ics/'

(3) Use [COM] in the [Connection] panel to choose the COM port.

(4) Click on the 'Analyzer' icon in the [Select Tool] panel to open the analyzer function window.

4.2 List of Variables for Analysis

Table 4-1 lists variables for use in displaying waveforms when the Analyzer user interface is in use.

Table 4-2 to Table 4-5 list the members of the structures listed in Table 4-1.

Table 4-1 List of Variables for Analysis

Variable Name	Type	Description	Remarks
g_st_ctrl_work	st_smps_ctrl_t	Information on st_smps_ctrl1 (values to be set)	See Table 4-2.
g_st_stat_work	st_smps_stat_t	Measured values and the presence or absence of an alarm source	See Table 4-3.
g_st_io_stat_old	u_io_stat_t	IO states (16-bit information)	See Table 4-4.
g_st_var_u_work	st_smps_variable_t	Registered information on the U phase	See Table 4-5.
g_st_var_v_work	st_smps_variable_t	Registered information on the V phase	See Table 4-5.
g_st_var_w_work	st_smps_variable_t	Registered information on the W phase	See Table 4-5.

Table 4-2 List of Members of the st_smps_ctrl_t Structure

Member of the st_smps_ctrl_t Structure	Type	Description
f4_vout_gain	float	Gain for output voltage detection
f4_iout_gain	float	Gain for output current detection
f4_vin_gain	float	Gain for inut voltage detection
f4_vin_low_det	float	Judgment threshold value for a temporary stop due to an input undervoltage
f4_vin_low_rel	float	Threshold value for release from a temporary stop due to an input undervoltage
f4_vin_ovp_det	float	Judgment threshold value for an input overvoltage error
f4_vout_low_det	float	Judgment threshold value for an output undervoltage error
f4_vout_low_delay	float	Judgment delay time for an output undervoltage error
f4_vout_high_det	float	Judgment threshold value for a temporary stop due to an output overvoltage
f4_vout_high_rel	float	Threshold value for release from a temporary stop due to an output overvoltage
f4_vout_ovp_det	float	Judgment threshold value for an output overvoltage error
f4_iout_high_det	float	Threshold value for judging that voltage will drop due to an output overcurrent
f4_iout_high_rel	float	Threshold value for release from the state of a voltage drop due to an output overcurrent
f4_iout_high_coef	float	Voltage-drop coefficient for output overcurrent
f4_iout_ocp_det	float	Judgment threshold value for an output overcurrent error
f4_duty_cmpl_coef	float	Duty cycle correction coefficient
f4_pic_coef_par	float	Proportional gain for constant voltage control
f4_pic_coef_int	float	Integral gain for constant voltage control
f4_target_slewrate	float	Slew rate of the target voltage in a soft start
f4_target_voltage	float	Target control voltage

Table 4-3 List of Members of the st_smps_stat_t Structure

Member of the st_smps_stat_t Structure	Type	Description
f4_vout_u_filt	float	U-phase output voltage before DC adjustment
f4_vout_v_filt	float	V-phase output voltage before DC adjustment
f4_vout_w_filt	float	W-phase output voltage before DC adjustment
f4_vout_u_adj	float	U-phase output voltage after DC adjustment
f4_vout_v_adj	float	V-phase output voltage after DC adjustment
f4_vout_w_adj	float	W-phase output voltage after DC adjustment
d8_vout_u_offs	double	DC offset value of the U-phase voltage
d8_vout_v_offs	double	DC offset value of the V-phase voltage
d8_vout_w_offs	double	DC offset value of the W-phase voltage
f4_vout_u_var	float	Mean squared value of the U-phase voltage
f4_vout_v_var	float	Mean squared value of the V-phase voltage
f4_vout_w_var	float	Mean squared value of the W-phase voltage
f4_iout_u_filt	float	U-phase output current before DC adjustment
f4_iout_v_filt	float	V-phase output current before DC adjustment
f4_iout_w_filt	float	W-phase output current before DC adjustment
f4_iout_u_adj	float	U-phase output current after DC adjustment
f4_iout_v_adj	float	V-phase output current after DC adjustment
f4_iout_w_adj	float	W-phase output current after DC adjustment
d8_iout_u_offs	double	DC offset value of the U-phase current
d8_iout_v_offs	double	DC offset value of the V-phase current
d8_iout_w_offs	double	DC offset value of the W-phase current
f4_iout_u_var	float	Mean squared U-phase current for use in calculating effective values
f4_iout_v_var	float	Mean squared V-phase current for use in calculating effective values
f4_iout_w_var	float	Mean squared W-phase current for use in calculating effective values
f4_vin_filt	float	Input voltage

Table 4-4 List of Members of the u_io_stat_t Structure

Bit Position	Description
15	AC output frequency; 0: 60 Hz, 1: 50 Hz
14	Reserved
13	Switching operation; 0: two-level, 1: three-level
12	Request to turn on or off; 0: request to turn on, 1: request to turn off
11	Request for release from the alarm state; 0: request for release, 1: not in effect
10	Reserved
9	Reserved
8	Reserved
7	Operating state; 0: operating, 1: stopped
6	Alarm state; 0: an alarm is being generated, 1: no alarm is being generated
5	Reserved
4	Reserved
3	Request for release from the alarm state in the software; 0: not in effect, 1: request for release
2	Request to turn on or off operation in the software; 0: request to turn off, 1: request to turn on
1	Completion of initialization; 0: not completed, 1: completed
0	Used to drive a blinking signal

Table 4-5 List of Members of the st_smps_variable_t Structure

Member of the st_smps_variable_t Structure	Type	Description
f4_target_voltage	float	Current target control voltage, which is updated during a soft start or in a voltage drop
d8_dsp_int	double	Cumulative value of the difference from the target values in filter outputs
f4_dsp_output	float	Filter outputs
f4_switch_onduty	float	On time determining the duty cycle of PWM output
u4_iout_high_flag	uint32_t	This member indicates the state of voltage dropping due to an overcurrent. 0: Normal constant voltage control, 1: dropping due to an overcurrent

5. Test results

5.1 Operation waveforms

Figure 5-1~Figure 5-6 shows the waveforms at startup and steady state in 2-level and 3-level operation mode.Table 5-1 shows the evaluation conditions.

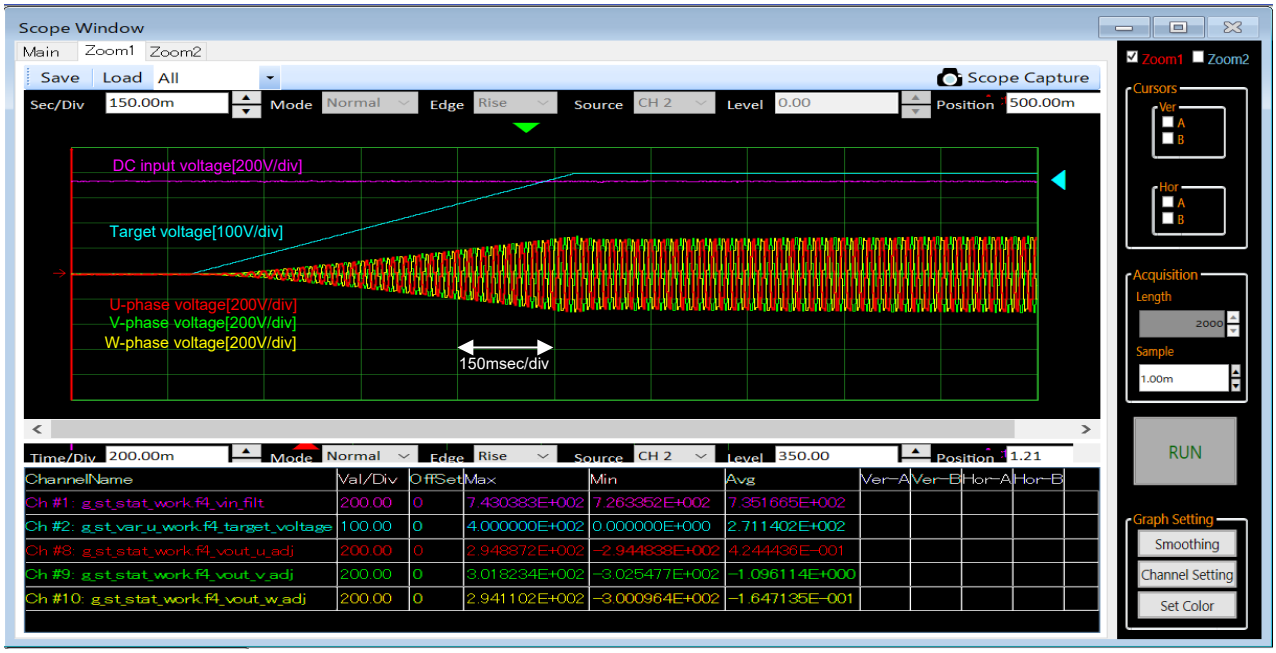
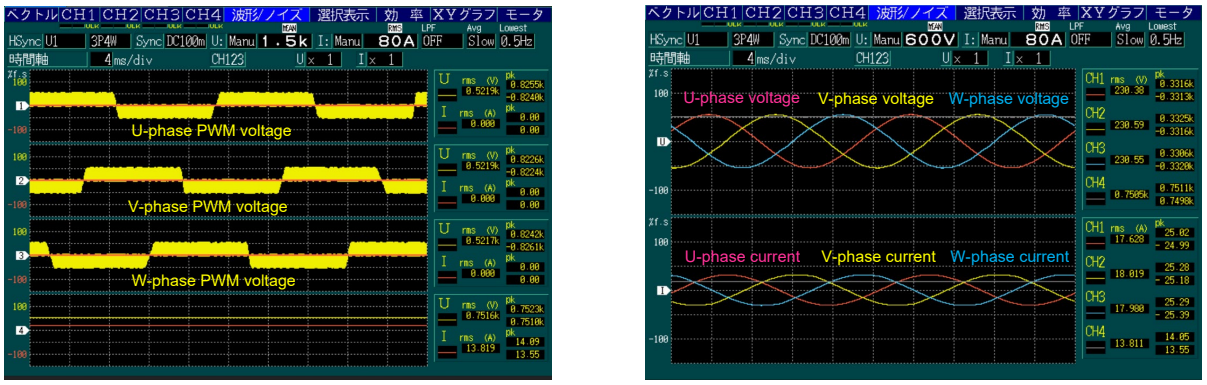


Figure 5-1 Startup waveform at 2Level/20kHz



(a)PWM voltage waveform (b)Output phase voltage/current waveform

Figure 5-2 Steady State waveforms at 2Level/20kHz

Table 5-1 Evaluation conditions

Items	Evaluation conditions
DC input voltage	750[Vdc]
Output Power	10kW, Power factor:0.8
PWM Operation mode	2-level, 3-level
Output voltage	3Φ, 400Vrms(line to line)
Output frequency	50Hz
Carrier freqeuency	2-level：20kHz, 3-level：20kHz,50kHz

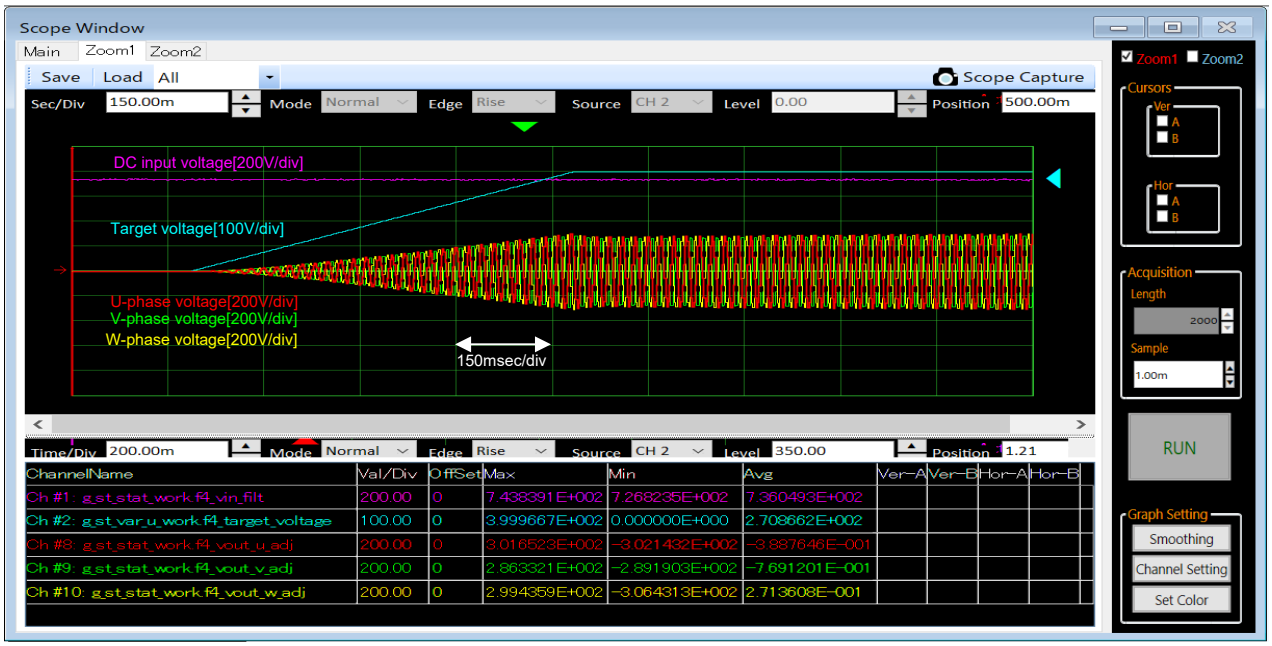
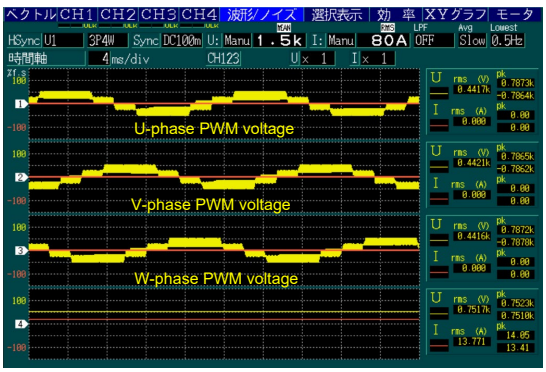
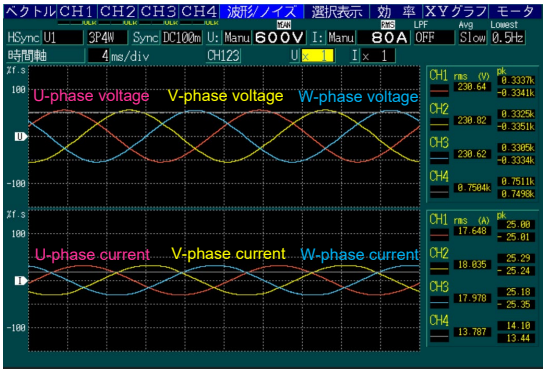


Figure 5-3 Startup waveform at 3Level/20kHz



(a) PWM voltage waveform



(b) Output phase voltage/current waveform

Figure 5-4 Steady State waveforms at 3Level/20kHz

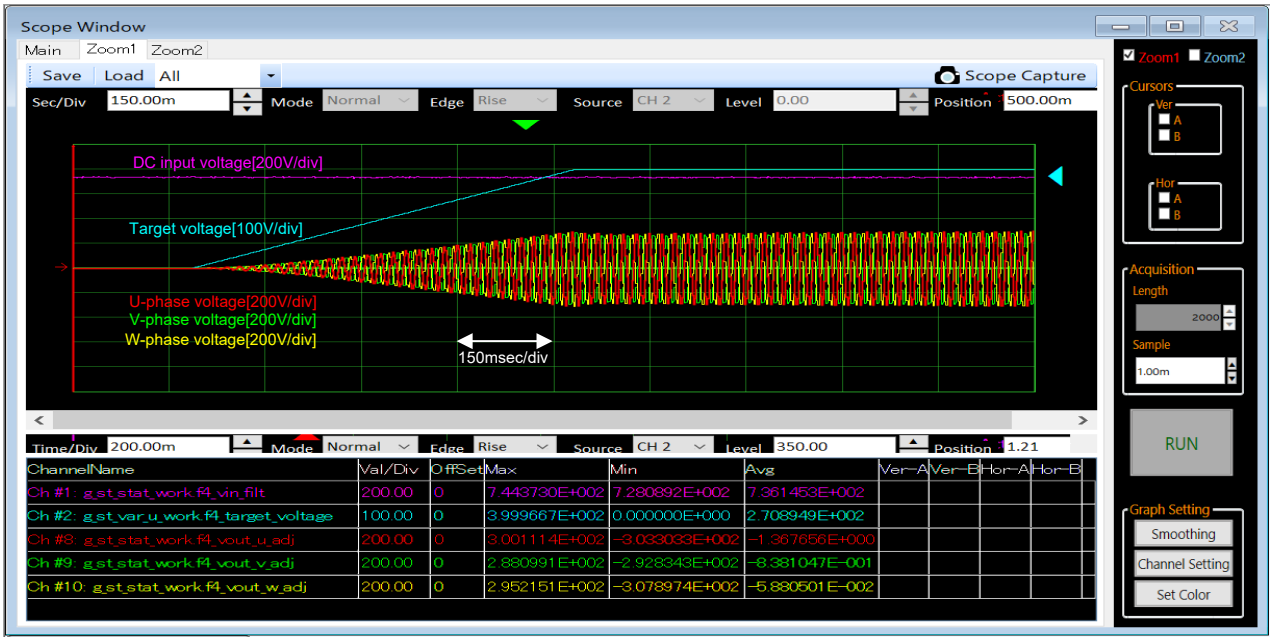
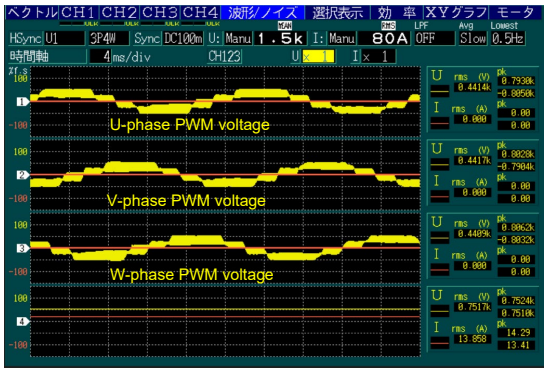
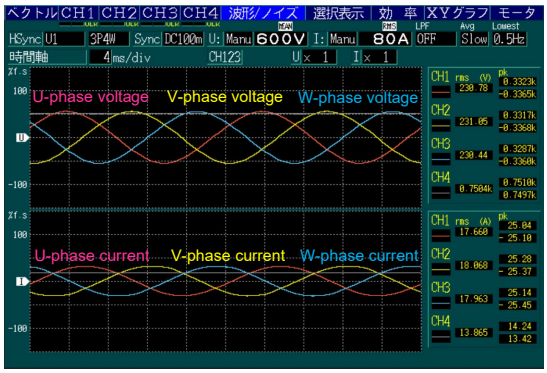


Figure 5-5 Startup waveform at 3Level/50kHz





- (a) PWM voltage waveform (b) Output phase voltage/current waveform

Figure 5-6 Steady State waveforms at 3Level/50kHz

5.2 Comparison of efficiency and filter reactors

Figure 5-7 shows the comparison results of system efficiency and inverter efficiency in 2-level and 3-level operation mode. The voltage fluctuation amplitude of each switching operation of the 3-level inverter is half that of a 2-level inverter. This brings about an almost 50% reduction in the switching loss of the switching element. therefore, even under 3-level/50kHz operation, the efficiency is equivalent to 2-level/20kHz.

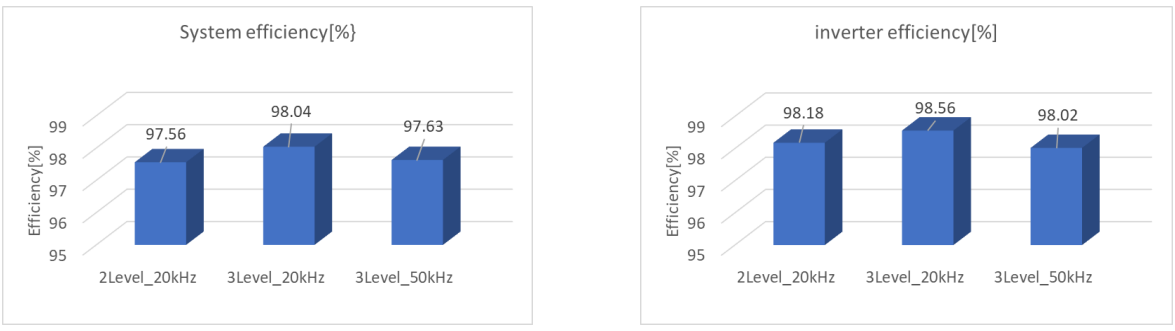


Figure 5-7 Efficiency comparison between the 2-level and 3-level operating mode

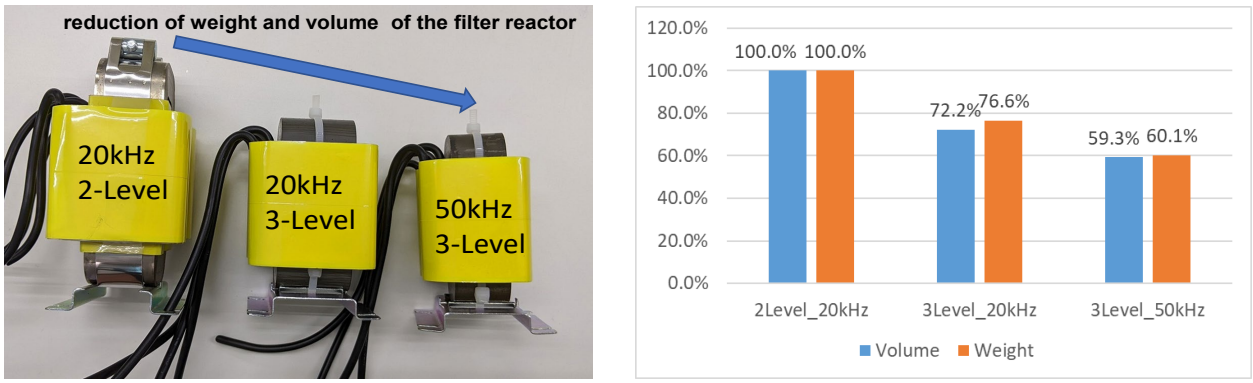


Figure 5-8 Comparison of volume and weight of filter reactors

As shown in Figure 5-8, the PWM output voltage waveform of the inverter in the 3-level operation mode, due to less high-order harmonic distortion components, compared with the 2-level/20kHz filter reactor,the volume and weight at the 3-level/20kHz can be reduced by 20%~30%, and at the 3-level/50kHz operation can be reduced by 40%.

5.3 CPU Utilization

Table 5-2 and Table 5-3 shows the CPU processing time and utilization for each control interval.

Conditions：CPU clock frequency：160 MHz、PWM carrier frequency：20 KHz

Table 5-2 CPU Utilization

Control interval	2-Level mode		3-Level mode	
	Processing time[μs]	CPU Utilization [%]	Processing time[μs]	CPU Utilization [%]
Low-Speed Timer Interrupt Processing(1ms-period)	0.18	0.02	0.18	0.02
High-Speed Timer Interrupt Processing(50us-period)	4.59	9.18	4.60	9.20
PWM Period Timer Interrupt Processing(50us-period)	4.06	8.12	4.88	9.76
Total	8.83	17.32	9.66	18.98

Conditions：CPU clock frequency：160 MHz、PWM carrier frequency：50 KHz

Table 5-3 CPU Utilization

Control interval	2-Level mode		3-Level mode	
	Processing time[μs]	CPU Utilization [%]	Processing time[μs]	CPU Utilization [%]
Low-Speed Timer Interrupt Processing(1ms-period)	0.18	0.02	0.18	0.02
High-Speed Timer Interrupt Processing(50us-period)	4.58	9.16	4.56	9.12
PWM Period Timer Interrupt Processing(20us-period)	4.04	20.20	4.84	24.20
Total	8.80	29.38	9.58	33.34

5.4 Program size

Table 5-4 shows the size of the sample program.

Table 5-4 ROM/RAM usage

Memory	Usage
ROM	25.3KB
RAM	9.1KB

Revision History

Rev.	Date of issue	Amendments	
		Page	Point
1.00	July.01.22	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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