RZ/A1H Group

High Speed Sync Serial DMA Transfer

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Introduction

This application note describes the operation of a sample embedded firmware project to demonstrate the transmission and reception of high-speed serial data, greater than 3Mb/s, using the on-board serial peripheral interface (RSPI) module and DMA. The sample is designed to be operated on two RSK+RZA1H development boards.

Target Device

RZ/A1H

When applying the sample program covered in this application note to another microcontroller, modify the program according to the specifications for the target microcontroller and conduct an extensive evaluation of the modified program.

The following documents in Table 1-1 apply to the RZK+RZ/A1H Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's Manual	Describes the technical details of the RSK hardware.	RSK+RZA1H User's Manual	R20UT3007EG
Quick Start Guide	Provides simple instructions to setup the RSK and run the first sample, on a single A4 sheet.	RSK+RZA1H Quick Start Guide	R20UT3006EG
Schematics	Full detail circuit schematics of the RSK.	RSK+RZA1H Schematics	R20UT2586EG
Hardware Manual	Provides technical details of the RZK+RZ/A1H microcontroller.	RZK+RZ/A1H Group User's Manual: Hardware	R01UH0403EJ

Table 1-1 Relevant Documents

1. List of Abbreviations

List of abbreviations used in this document is available in Table 1-1.

Abbreviation	Full Form
CPU	Central processing unit
CRC	Cyclic redundancy check
DACK	Transfer request acknowledge signal
DMAC	Direct memory access controller
DMAC3	Direct memory access controller channel 3
DMAC5	Direct memory access controller channel 5
GND	Ground reference
IIC	Inter-integrated circuit
IRQ	Interrupt request
MISO	Master in slave out
MOSI	Master out slave in
NOR	NOR flash memory
OSTM	Operating system timer
RAM	Random access memory
RSK	Renesas starter kit
RSPCK	RSPI clock
RSPI	Renesas serial peripheral interface
RSPI RX	RSPI receive buffer
RSPI TX	RSPI transfer buffer
RSPI1	Renesas serial peripheral interface channel 1
RSPI4	Renesas serial peripheral interface channel 4
SSL	Slave select

Table 1-1 List of Abbreviations

Table of Contents

2. Specifications

The DMAC can be used in place of the CPU to perform high-speed transfers between external devices that have DACK, external memory, on-chip memory, memory-mapped external devices, and on-chip peripheral modules.

This application note explains how to use the RZ/A1H DMA controller for transmission and reception of data via the RSPI module. The sample application uses a DMAC channel to transmit ASCII data from on-chip RAM memory to the transfer buffer of RSPI. This data is sent through MISO or MOSI pin depending on whether the RSK is configured as a master or a slave device. A different DMA channel is used to load the received data into RAM. The movement of data between RSPI and on-chip RAM is carried out using only DMAC without any CPU intervention.

Peripheral Function	Use
DMAC5	DMAC5 will be configured to transfer data from RSPI4 RX to RAM.
DMAC3	DMAC3 will be configured to transfer data from RAM to RSPI4 TX.
RSPI4	Used for serial transmission.
RSPI1	Used for communication with the PMOD LCD screen.
OSTM	Used to create a timer to measure the transfer rate

Table 2-1 Peripheral Function to be Used and Their Uses

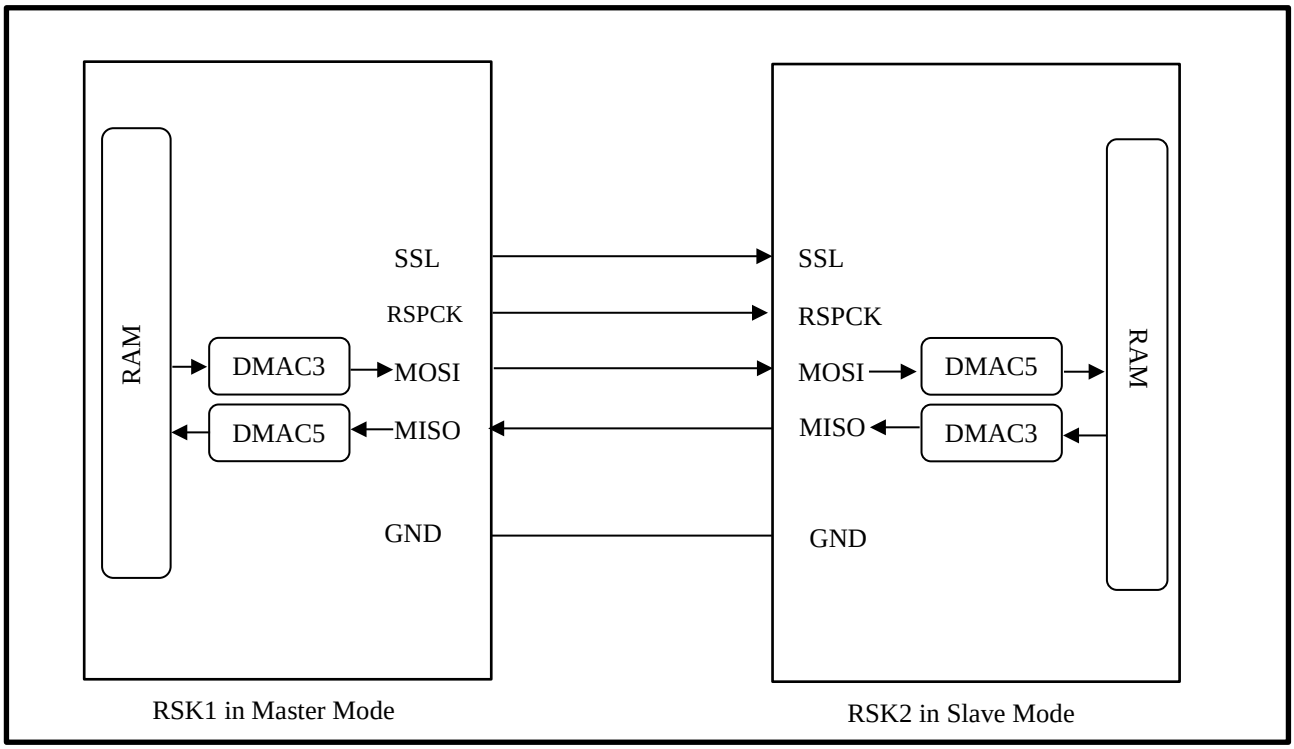

Figure 2-1 Outline of Operation for Two Devices

The arrows in Figure 2-1 indicate the direction of data flow.

3. Operating Check Conditions

The sample code described in this application note has been checked under the conditions listed in Table 3-1.

Item	Description
Microcontroller used	RZA1H (R7S721001)
Operating frequency	- Maximum operating frequency : 400MHz - Image processing clock : 266.67MHz - Internal bus clock : 133.33MHz - Peripheral clock1 : 66.67MHz - Peripheral clock0 : 33.33MHz
RSK Operating voltage	5.0V
Integrated development environment	e^{2}studio version 4.0.1.007
C Compilers	KPIT GNUARM-NONE_EABI Toolchain v14.02
Board used	RSK+RZ/A1H board

Table 3-1 Operating Check Conditions

4. Description of Hardware

The sample is intended to be run on the RSK+RZA1H. For more information on the RSK+RZA1H hardware please refer to the User's Manual (R20UT3007EG) and the RSK+RZA1H schematics (R20UT2586EG).

4.1 List of Pins to be used

Table 4-1 lists the pins to be used and their functions.

Port Name	Signal Name	I/0	Description
P2_8	P2_8_RSPCK4	Input/output	Used for RSPI4 clock input or output
P2_9	P2_9_SSL40	Input/output	Used for RSPI4 slave select
P2_10	P2_10_MOSI4	Input/output	Used for RSPI4 MOSI
P2_11	P2_8_MISO4	Input/output	Used for RSPI4 MISO
P11_12	P11_12_RSPCK1	Output	Used for PMOD CLK line
P4_15	PMOD_RST	Output	Used for PMOD command line
P3_7	PMOD_PIN10	Output	Used to for PMOD Command line
P1_9	IRQ3	Input	SW1. Connects to an IRQ input for user controls
P1_8	IRQ2	Input	SW2. Connects to an IRQ input for user controls.
P1_11	IRQ5	Input	SW3. Connects to an IRQ input for user controls.

Table 4-1 Pins to be Used and their Functions

4.2 Configuration

Please make sure that both used boards have the following settings.

4.2.1 Switches

Ensure that SW4 has the settings shown in Table 4-2.

SW4	SW4-1	SW4-2	SW4-3	SW4-4	SW4-5	SW4-6	SW4-7	SW4-8
State	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Table 4-2 SW4 Settings

Ensure that SW6 has the settings shown in Table 4-3.

SW6	SW6-1	SW6-2	SW6-3	SW6-4	SW6-5	SW6-6
State	ON	ON	ON	ON	ON	ON

Table 4-3 SW6 Settings

4.2.2 Jumpers

All Jumpers shall not be fitted with the following exceptions:

- JP11 1-2 connected
- JP12 1-2 connected
- JP21 1-2 connected
- JP18 1-2 connected

4.2.3 Resistor Modifications

No resistor modification from the default RSK state is required for this sample code.

4.2.4 Connections

For transmission and reception to take place over two boards, the connections outlined in Table 4-4 are required.

RSK 1	RSK 2	Function
CN15_1	CN15_1	MISO to MISO
CN15_3	CN15_3	MOSI to MOSI
CN15_5	CN15_5	RSPCK to RSPCK
CN15_7	CN15_7	SSL to SSL
GND	GND	GND to GND

Table 4-4 Board to Board Connection

4.2.5 Caution

When carrying out transmission and reception between two boards, please make sure that there is a connection between the grounds of the two boards. I.e. any GND on board 1 to any GND on board 2. Not connecting the two grounds could result in track and/or component damage.

5. Description of Software

The sample application covered in this application note uses the DMAC to move the data between RSPI data buffer and the on-board RAM. DMAC3 is used to move data from the on-chip RAM to RSPI data buffer while DMAC5 is used to move data from RSPI data buffer to the on-chip RAM. If data is written to RSPI data buffer, it automatically gets transferred to the RSPI TX. However, if the RSPI data buffer is read, data is automatically fetched from the RSPI RX. The progress/outcome of the transmission and reception is displayed on PMOD

5.1 Operation Outline

The operation outline of the sample code is described below in sections (a) to (f).

(a) **Display introduction message**

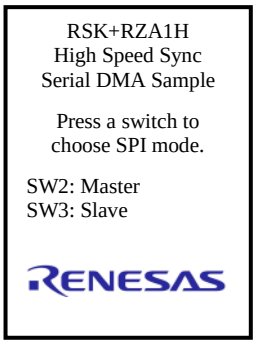

Figure 5-1 Introduction Message

(b) **Switch press**

- Wait for either SW2 or SW3 press.

(c) **Display chosen mode and initialise RSPI4 accordingly**

- If SW2 was pressed initialise, RSPI4 in master mode. The display should resemble **Figure 5-2**.

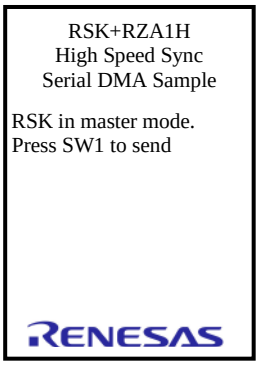

Figure 5-2 Display after SW2 Press

- IF SW3 was pressed, initialise RSPI4 in slave mode. The display should look like **Figure 5-3**.

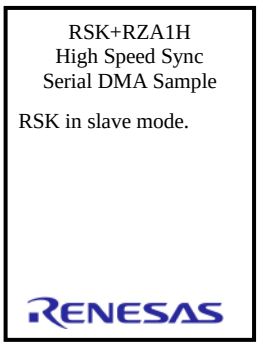

Figure 5-3 Display after SW3 Press

(d) **Wait for SW1 to be pressed on the master RSK.**

(e) **Enable transmission**

- Take first time stamp. Wait for DMA channel three to complete. The PMOD should look like **Figure 5-4**.

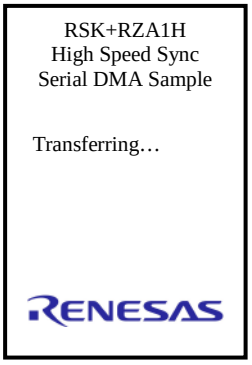

Figure 5-4 Display During Transfer

(f) **Display transmission rate and check received data integrity**

- Take another time stamp and calculate data rate. On transfer completion PMOD should look like **Figure 5-5**.

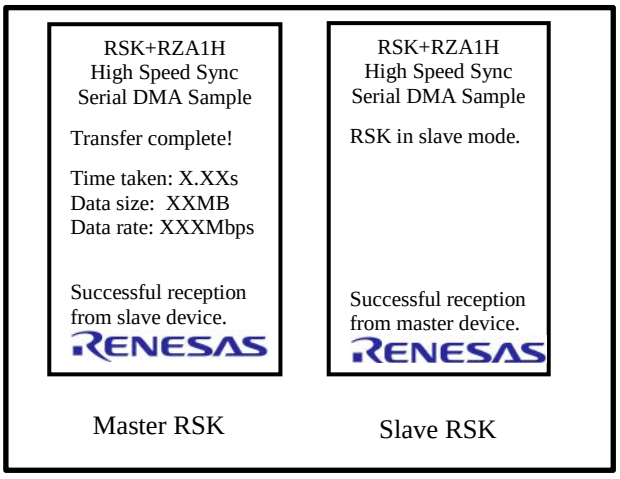

Figure 5-5 Display After Transmission and Reception

5.2 Data Integrity

This sample code uses an extremely efficient and fast implementation of CRC16 algorithm as a means of error checking. The data that is sent from one RSK to another has a CRC value appended to it. The receiving board will calculate the CRC value of the received data and compare the result to the appended CRC. If the CRC values do not match, the PMOD display will resemble to Figure 5-6.

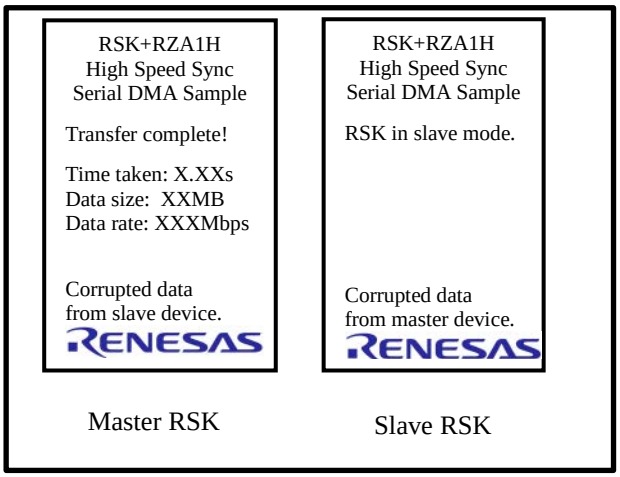

Figure 5-6 Corrupted Data

To alter the amount of data to be transferred the user can configure a macro (DATA_SIZE), which is found in ‘configuration.h’. The CRC value will be calculated for the new data size. However, if DATA_SIZE is to be set to more than 100000, please make sure to update the size and add appropriate number of bytes to the array ‘g_dmac_src_data_internalram’ found in ‘data.c’.

5.3 Flow Charts

Figure 5-7 shows the overall flow of the sample program described in this application note.

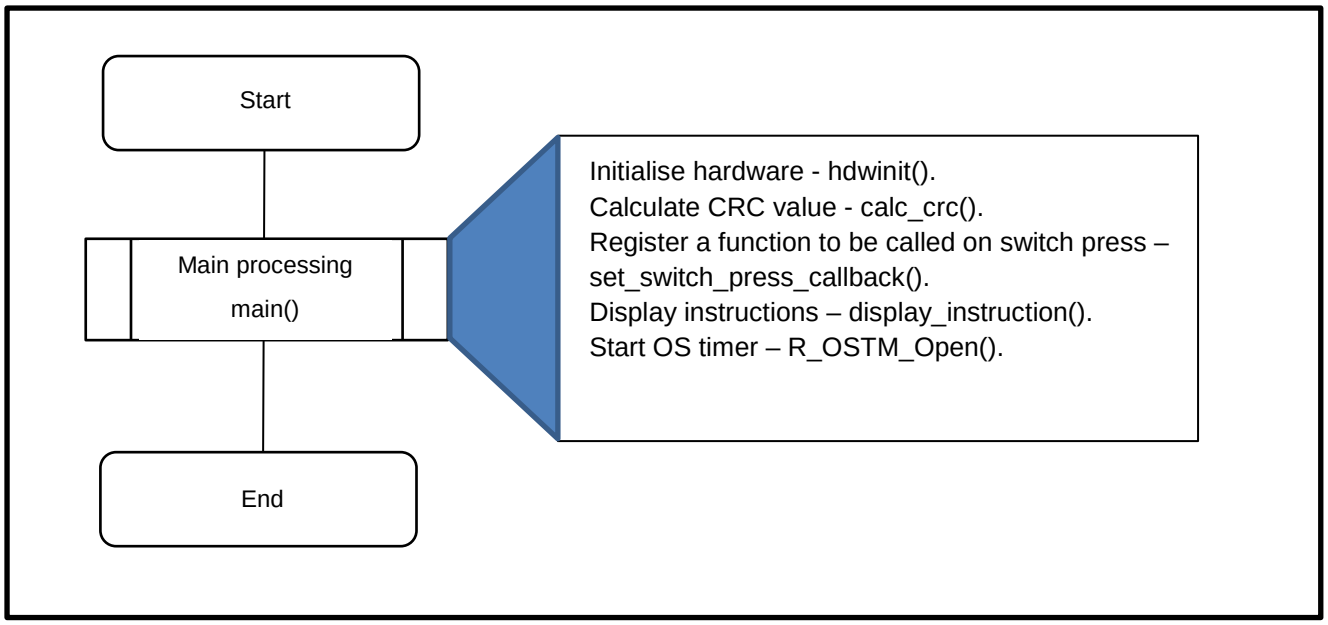

Figure 5-7 Overall Flow

5.3.1 Peripheral Initialisation

Figure 5-8 shows the hdwinit() function flow.

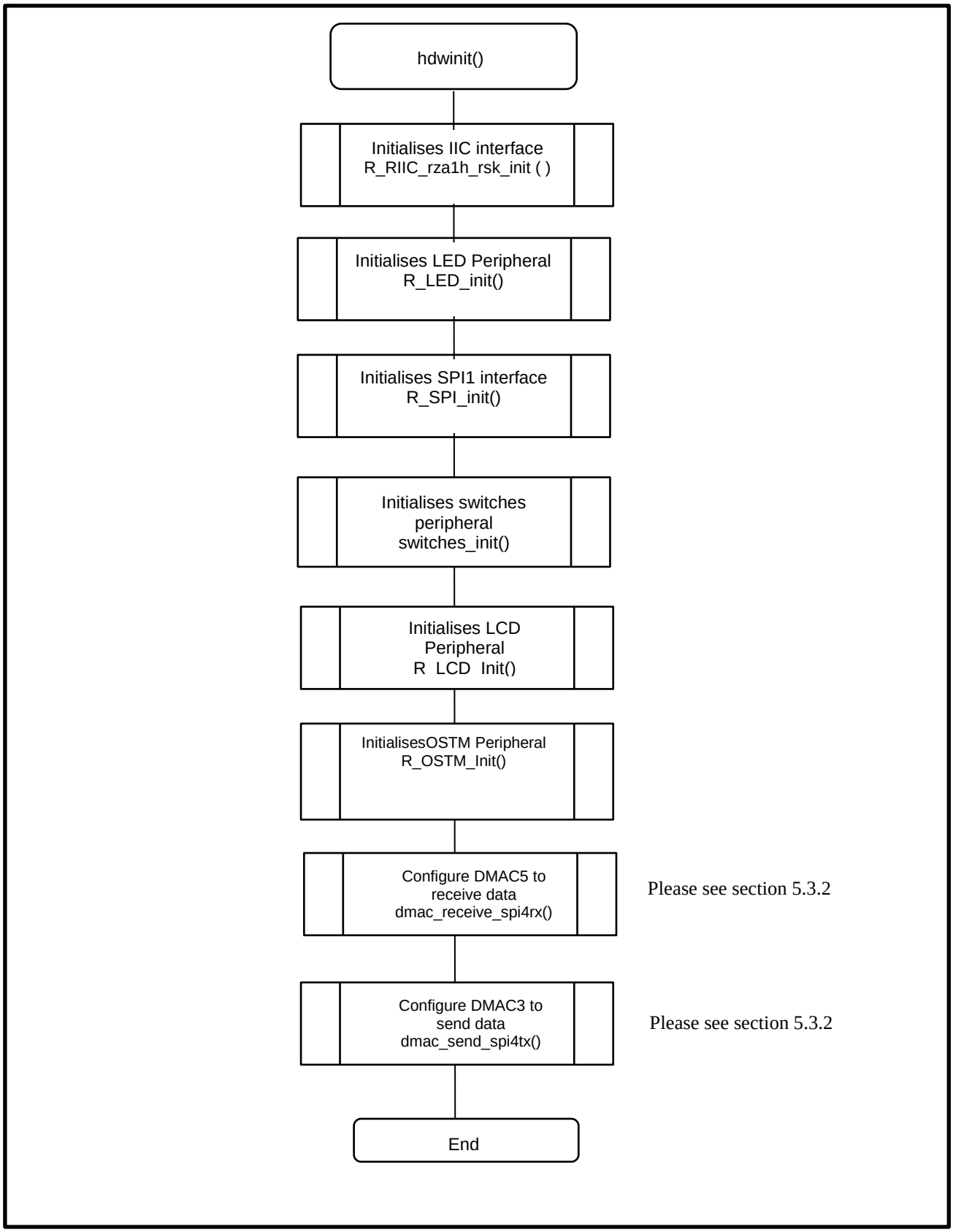

Figure 5-8 Initialisation Function

5.3.2 DMA Configuration

Figure 5-9 shows the DMA configuration

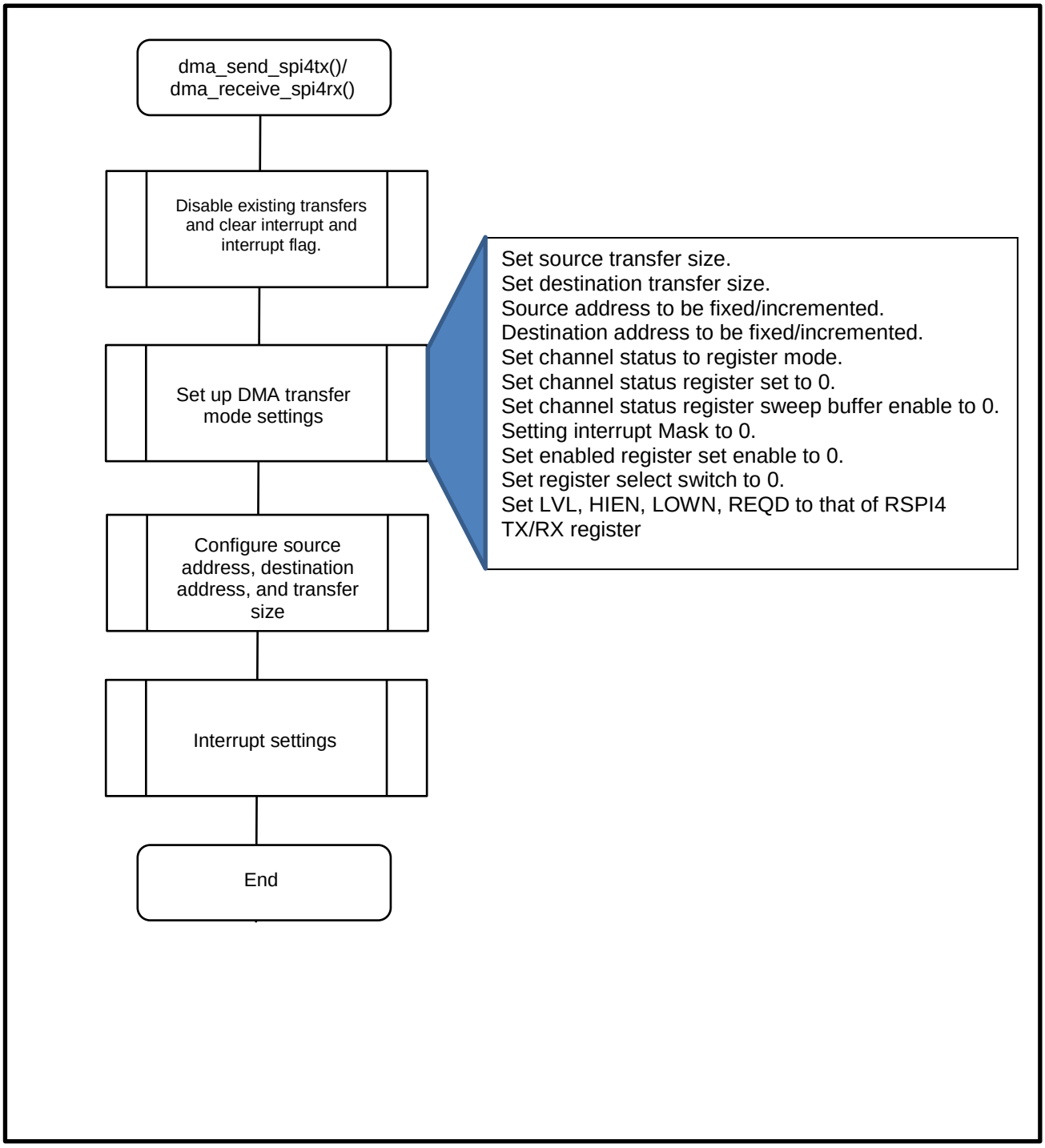

Figure 5-9 DMA Configuration

5.3.3 RSPI Configuration

Figure 5-10 shows the RSPI4 configuration in slave mode. RSPI4 configuration occurs when either SW2 or SW3 is pressed after the user is prompted to choose an SPI mode.

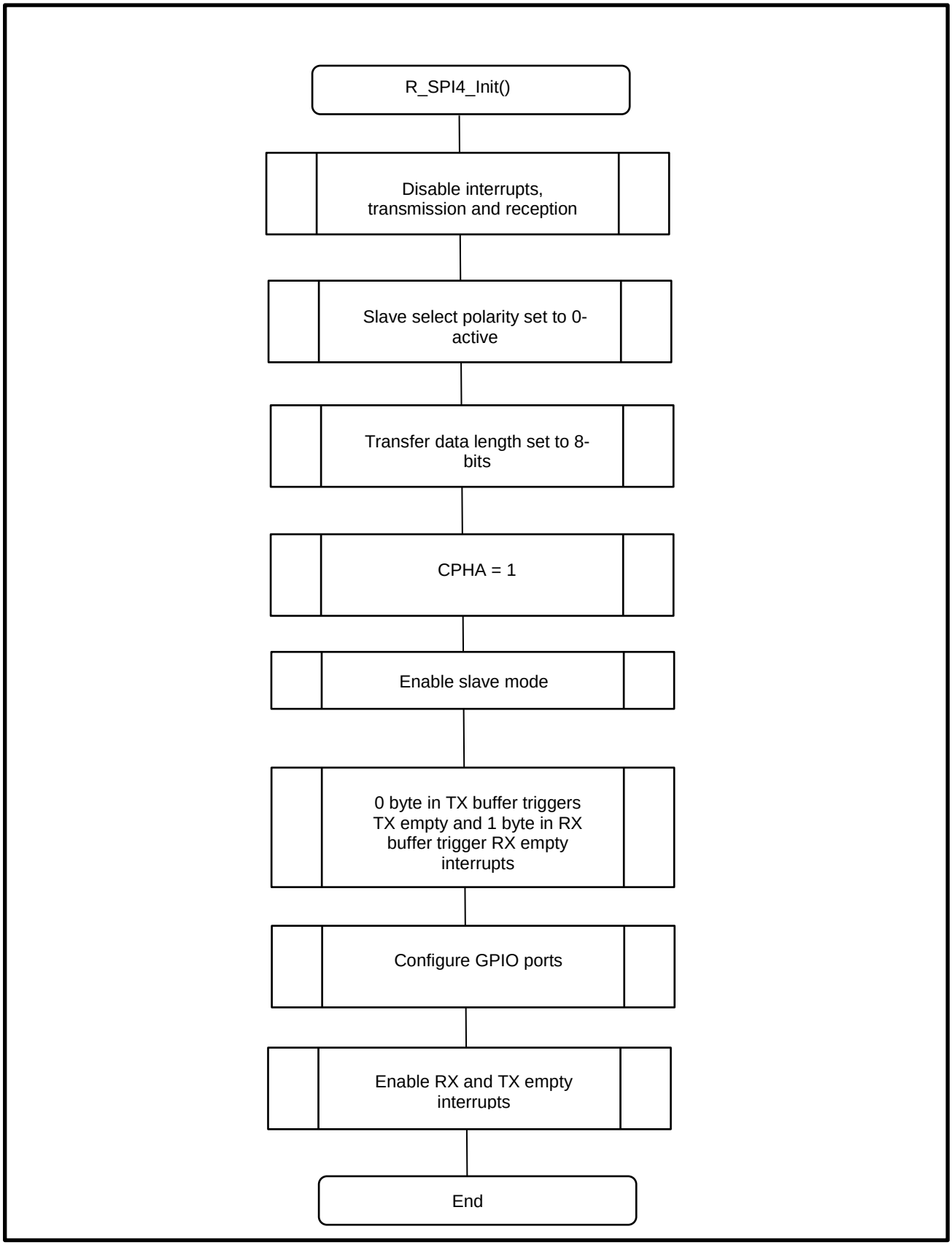

Figure 5-10 Slave Mode SPI Configuration

Figure 5-11 shows RSPI4 configuration in master mode.

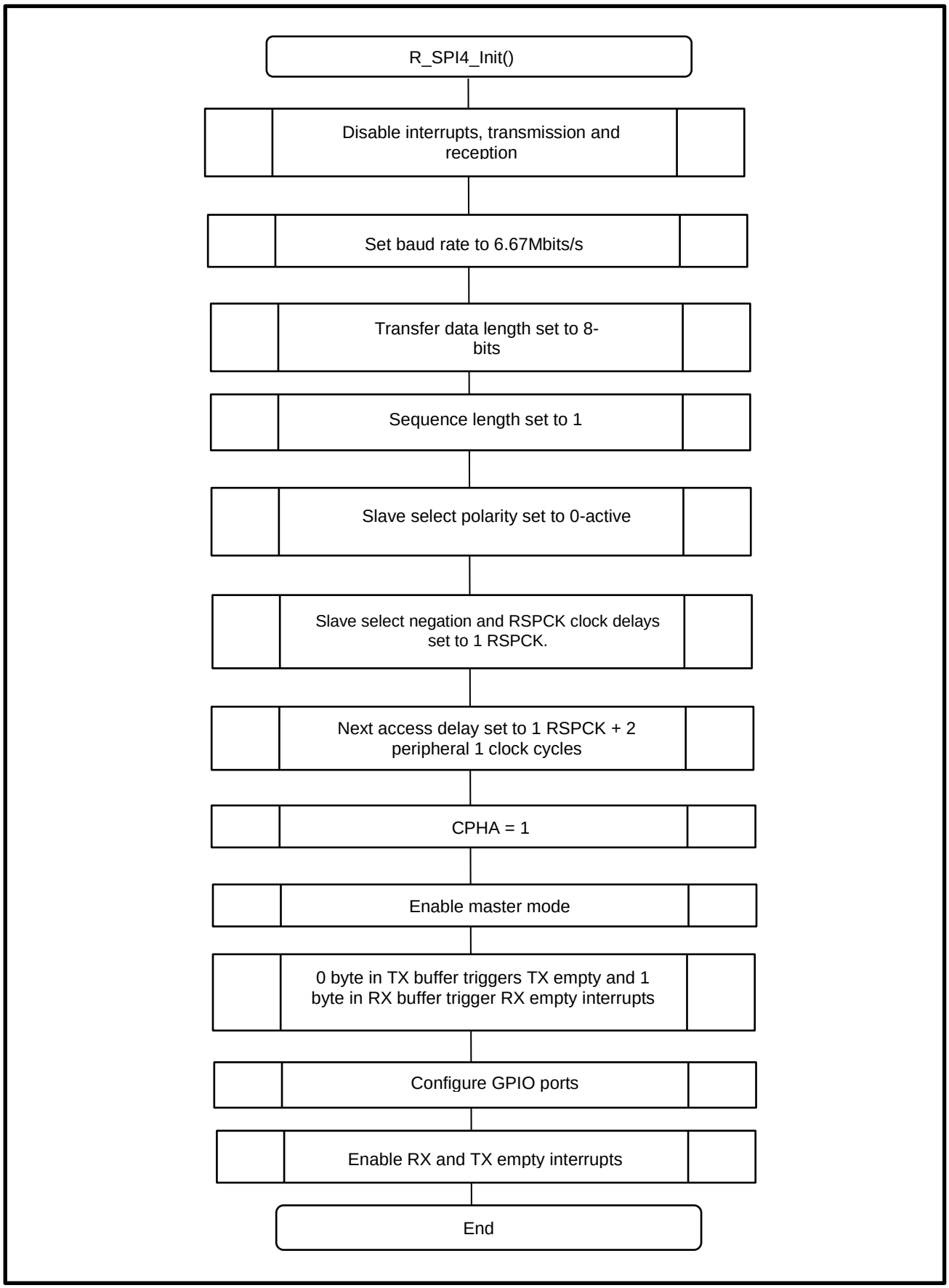

Figure 5-11 Master Mode SPI Configuration

5.3.4 Main Processing

Figure 5-12 shows the flow of the sample program.

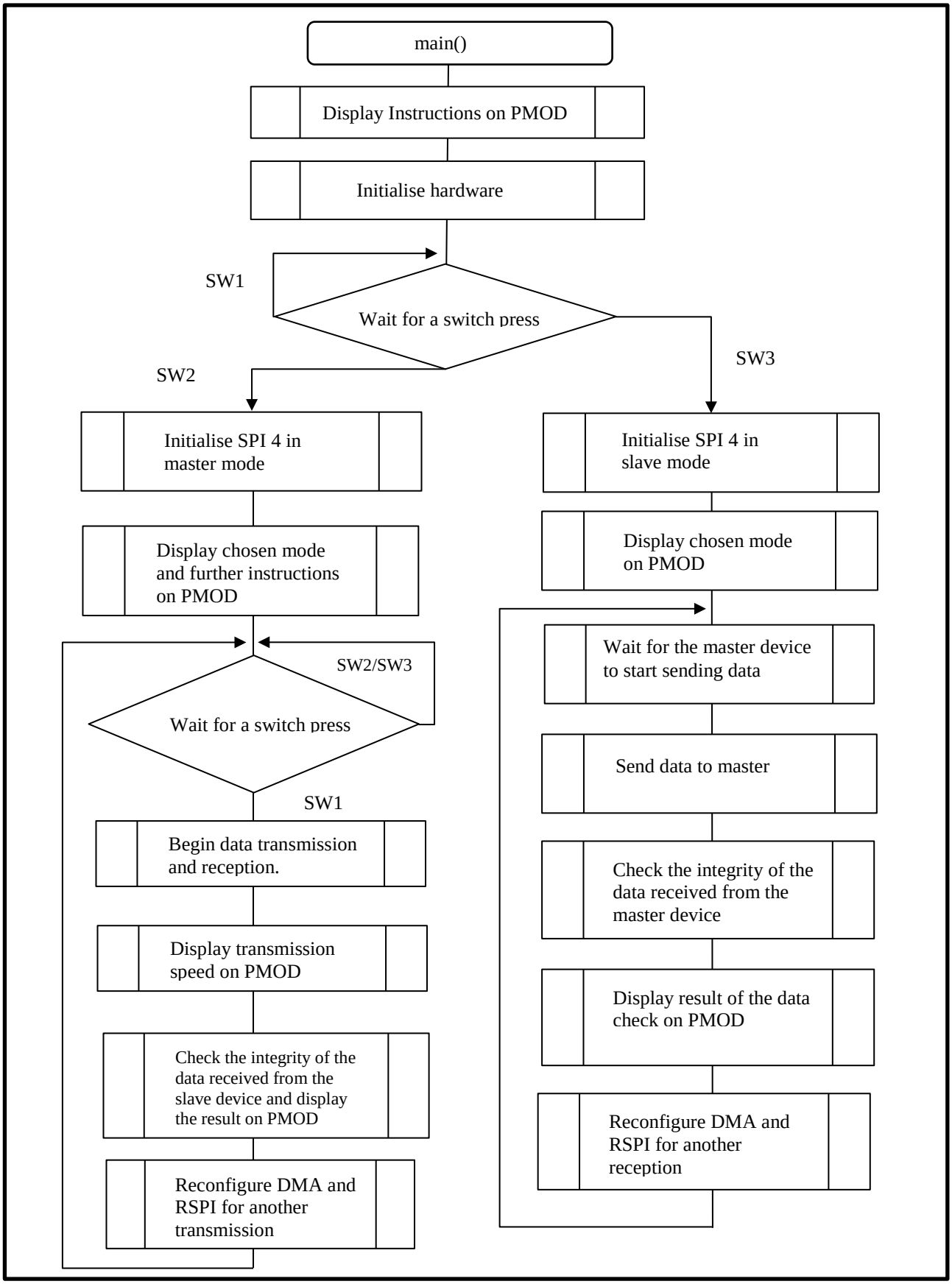

Figure 5-12 Main Processing

6. Two Board reception and transmission

If one PC is to be used for transmission across two RSK+RZA1Hs, it will be necessary to bootload the sample code into the NOR of one or both RSKs. The PC can be used to run one of the RSKs via the debugger and the other RSK can run from NOR. Alternatively, both RSKs can run from NOR.

For stand-alone operation of both RSKs, load the same sample code on both boards as outlined in section 6.1. Once the sample code is successfully loaded onto both boards, follow the instructions on PMOD to carry out data transmission.

6.1 Bootloading in NOR

This section is used for reference to program sample code into NOR flash to allow stand-alone operation. This requires SEGGER J-Link programmer/debugger.

Supplied with this sample is a batch file 'LoadUserApplicationToNor.bat'

The instructions follows as;

- Build the 'RZ_A1H_HSSS_DMA' sample in either/both 'HardwareDebug' and/or 'Release' mode.
- Setting the correct path to JLink.exe might be necessary. To do this, open 'LoadUserApplicationToNor.bat' using any text editing program and set the correct path to where JLink.exe is located on the PC being used. Only lines 48, 53, 59 and 64 of the .bat file need to be modified depending on whether PC being used is 32-bit or 64-bit.
- Ensure that SW6 is configured as outlined in Table 6-1.

SW6	SW6.1	SW6.2	SW6.3	SW6.4	SW6.5	SW6.6
STATE	ON	ON	ON	ON	ON	ON

Table 6-1 SW6 Setting

- Double click on 'LoadUserApplicationToNor.bat' and follow the on-screen instructions.

7. Sample Code

The sample code is available on the Renesas Electronics Website.

Website and Support

Renesas Electronics Website
http://www.renesas.com/

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Jan 11, 2016	All	Created.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

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