RZ/N2L Group

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RZ/N2L Industrial Network SOM Kit Application Note: HTTP Server Sample Program

Introduction

This document explains the setup procedure and operation of HTTP server sample program.

Target Device

RZ/N2L

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1. Overview

This document describes the setup and debug procedure of this sample program for RZ/N2L Industrial Network SOM Kit.

In the sample program, TCP/IP communication function is implemented by FreeRTOS plus TCP.

When this SOM Kit is shipped, this sample program is written in the flash memory.
If you want to restore shipment state, execute this sample program.
Executing this sample program writes the program to the flash memory.

1.1 Reference

Technical information about RZ/N2L is available via Renesas.

Table 1. Technical Inputs

Index	Technical Inputs
1	r01uh0955ejxxxx-rzn2l.pdf (RZ/N2L User's Manual: Hardware)
2	r01an6434ejxxxx-rzt2-rzn2-fsp-getting-started.pdf (Getting started with Flexible Software Package)
3	r12ut0020edxxxx-rzn2l-som-kit-hw.pdf (RZ/N2L Industrial Network SOM Kit Use's Manual)

2. Project Setup

2.1 Requirements

Table 2. Requirements

Item	Vender	Description
Board	Renesas Electronics	RZ/N2L Industrial Network SOM Kit
IDE	IAR Systems	● Embedded Workbench® for ARM Version 9.30.1 Please apply patch (EWARM_Patch_for_RZN2L) which is available in http://www.renesas.com/rzn2l. Regarding how to apply the patch, please read the readme file in patch file.
	Renesas Electronics	● e² studio 2023-04 ● FSP Smart Configurator 2023-04 ● RZ/N2L Flexible Software Package (FSP) v1.2.0 Please download from the link below. https://github.com/renesas/rzn-fsp/releases/tag/v1.2.0
Emulator	IAR Systems	I-jet
	SEGGER	Hardware: J-Link Software: J-Link Commander V7.82f *1

*1: J-Link Commander is used for erasing flash memory.
J-Link Commander is included in “J-Link Software and Documentation Pack” on the following site.
https://www.segger.com/downloads/jlink/

2.2 Hardware

This document describes the major hardware. Refer to RZ/N2L Industrial Network SOM Kit user's manual and schematic for more board details.

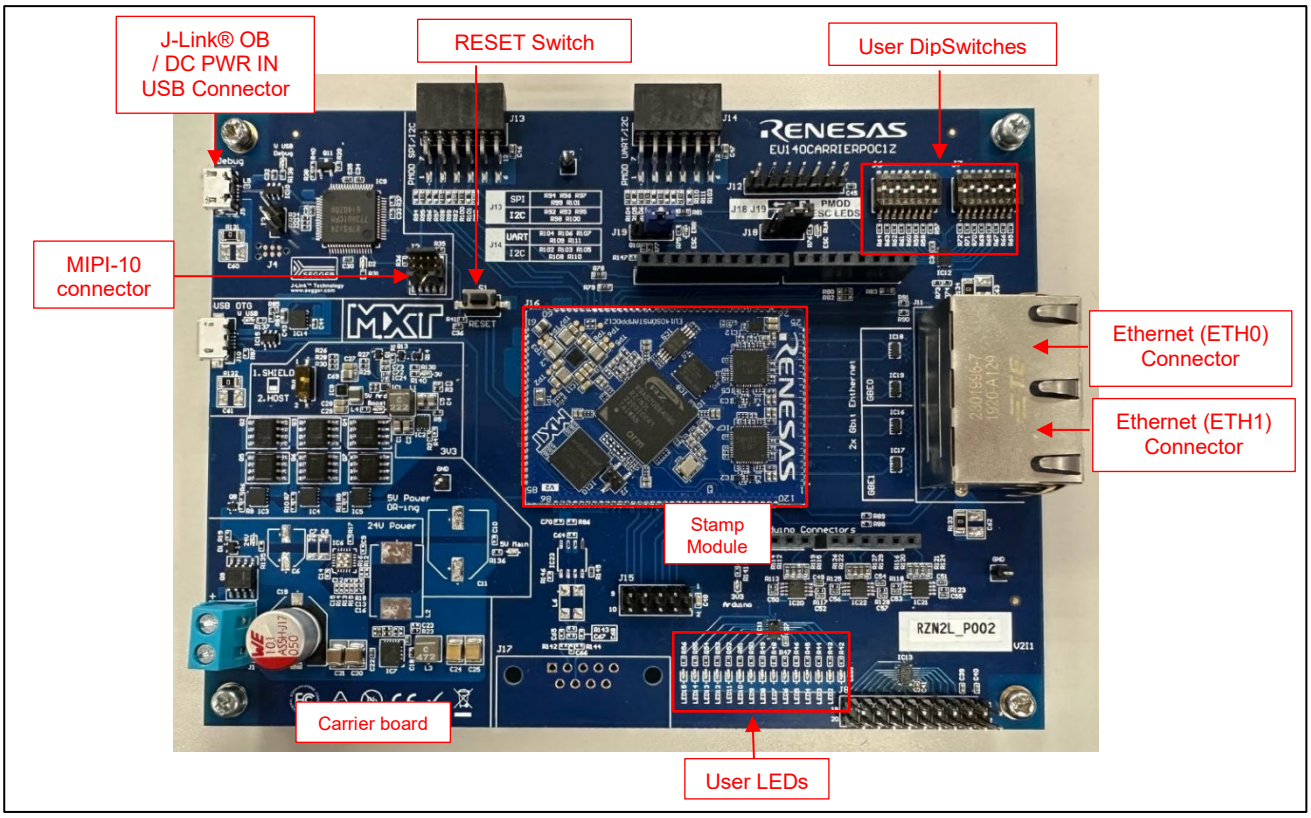


Figure 2-1 RZ/N2L Industrial Network SOM Kit

2.3 Setup the Board

Setting the board for running sample program is shown below.

1. Connect the I-jet to J2 or the USB cable to J5 for J-link OB on Carrier board.

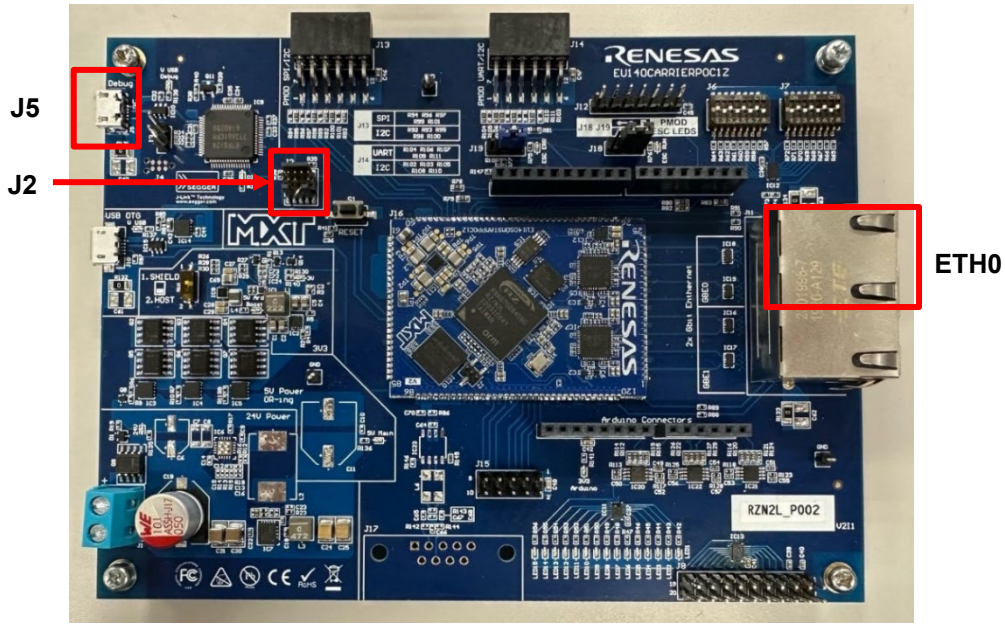


Figure 2-2 Setup the SOM Kit

2. Power is supplied by connecting USB Micro-B cable to the USB connector “J5) of the Carrier board.
3. Connect Ethernet Cable to the Ethernet Connector “ETH0”.

2.4 Board IP address setting

The IP address of this sample program is set in src/net_thread_entry.c.

IP address : 192.168.10.100

Subnet mask : 255.255.255.0

Default gateway : 192.168.10.254

DNS server address : 192.168.10.1

```
static  uint8_t ucIPAddress[ 4 ]        = {192, 168, 10, 100};
static  uint8_t ucNetMask[ 4 ]          = {255, 255, 255, 0};
static  uint8_t ucGatewayAddress[ 4 ]   = {192, 168, 10, 254};
static  uint8_t ucDNSServerAddress[ 4 ] = {192, 168, 10, 1};
```

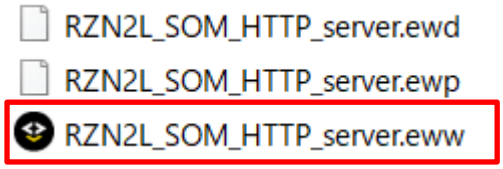
3. Running the sample application

3.1 Build and debug sample code for EWARM

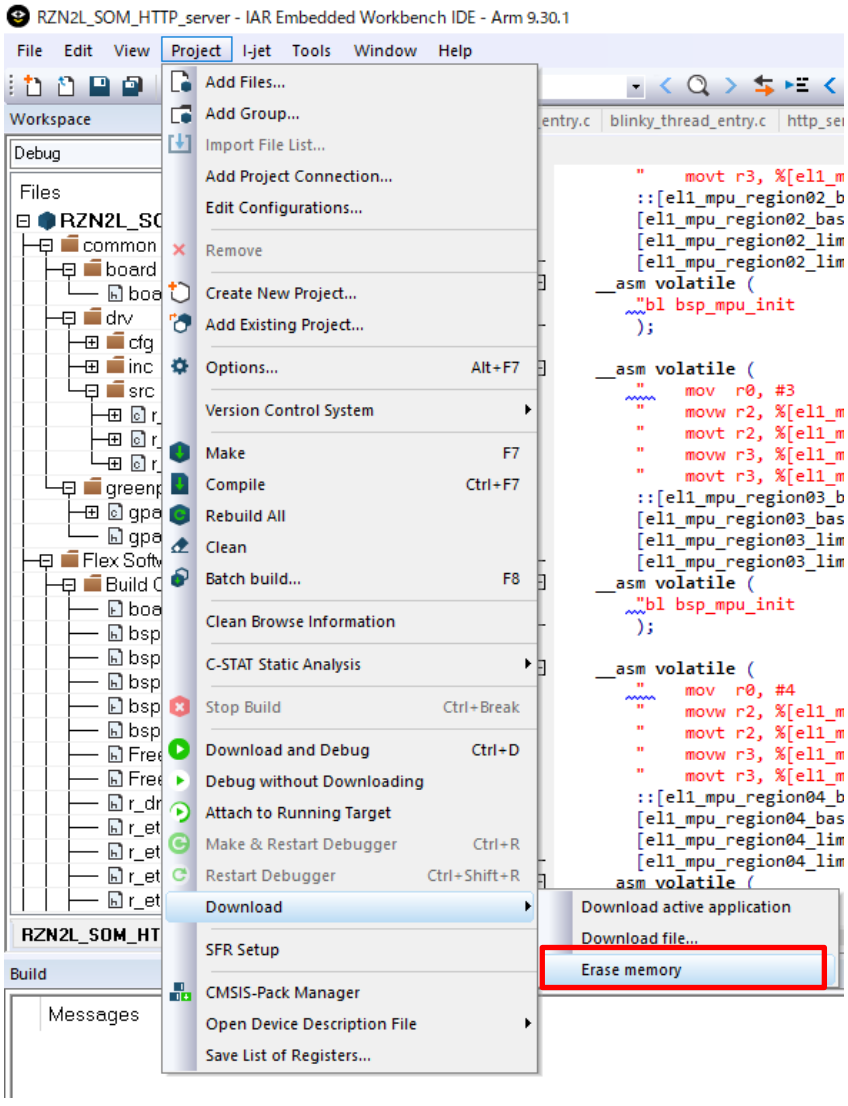
3.1.1 Erasing the flash memory

If you want to erase the flash memory on this SOM Kit using EWARM, execute the following steps.

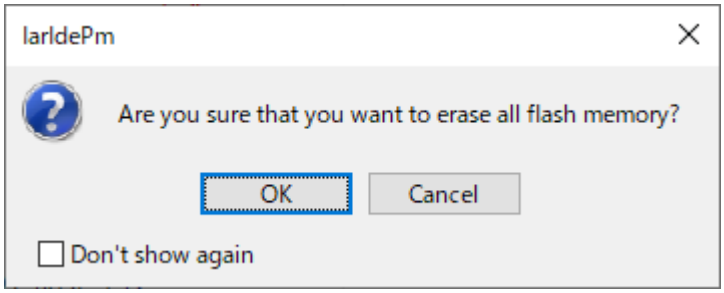
1. Open the sample project.
   “HTTP_server\ewarm\RZN2L_SOM_HTTP_server\RZN2L_SOM_HTTP_server.eww”



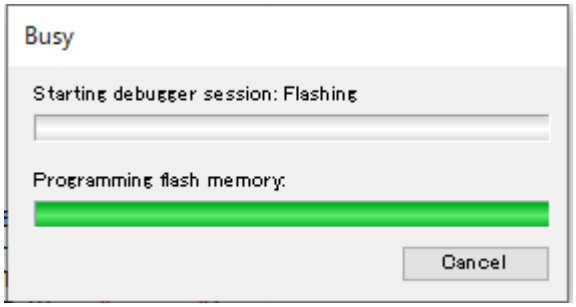
2. Select “Project” -> “Download” -> “Erase memory”.



3. Select “OK”.



4. After the following dialog appears, erasing of the flash is complete if no error occurs.

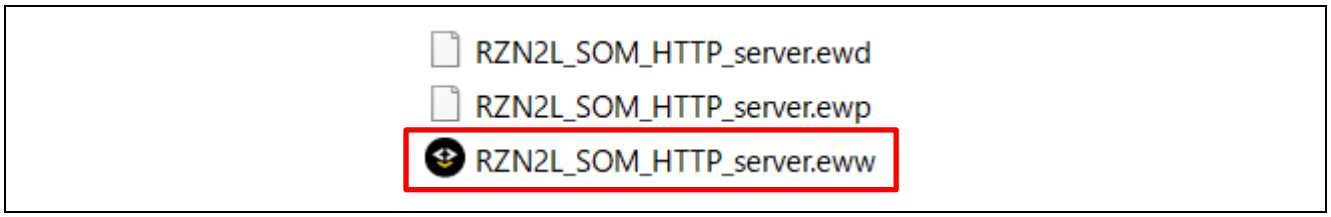


3.1.2 Project build and debug

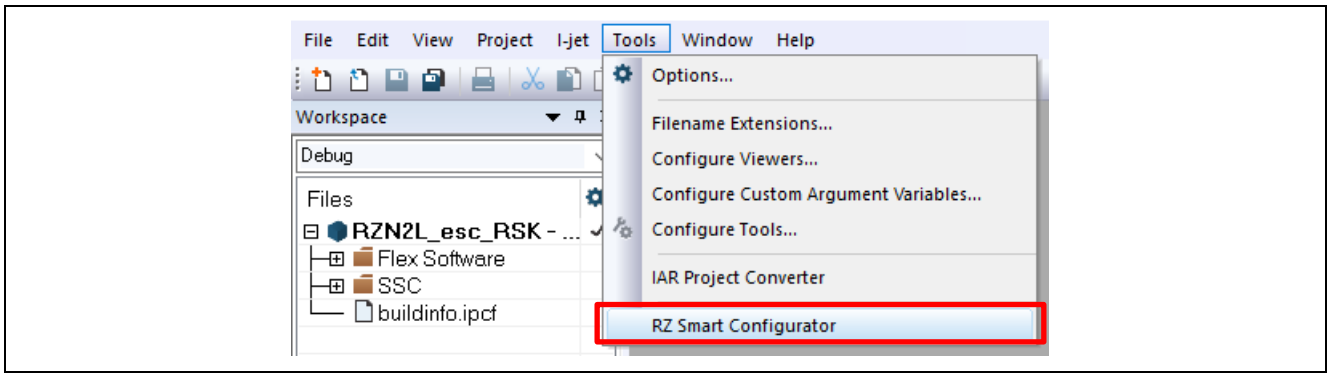
Build and load the sample code using IAR Embedded Workbench.

Note). Please install FSP Smart Configurator in advance.
Refer to the latest getting started guide.(R01an6434ejxxxx- rzt2-rzn2.pdf)
Replace the project name in the figure with the project name of this sample project.

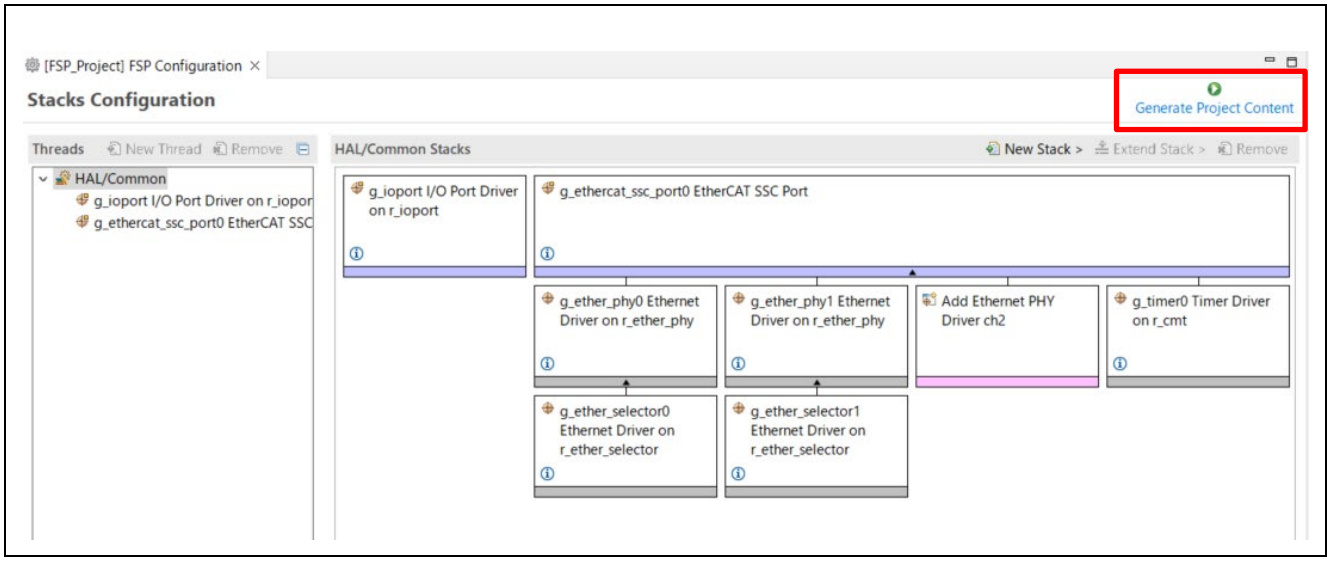
5. Open the sample project.
“HTTP_sever\ewarm\RZN2L_SOM_HTTP_server\RZN2L_SOM_HTTP_server.eww”



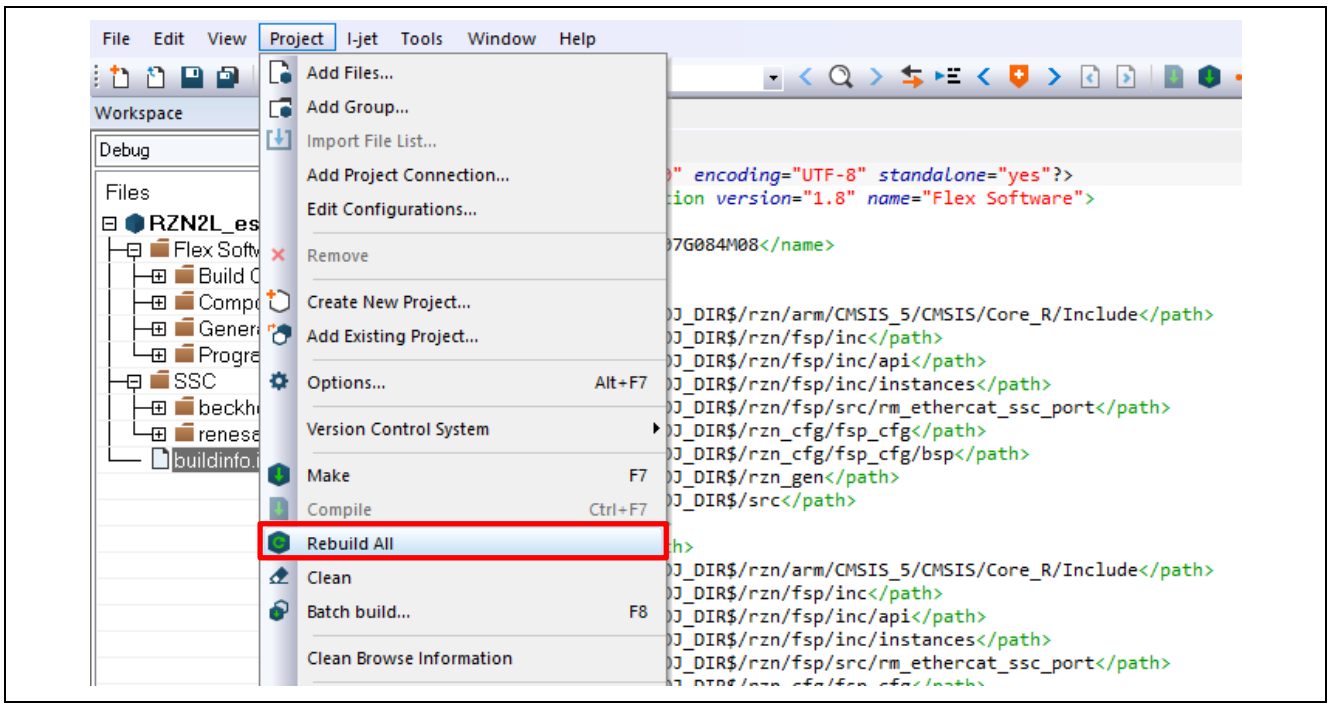
2. Open the “RZ Smart Configurator”



3. Generate the code with "Generate Project Content".

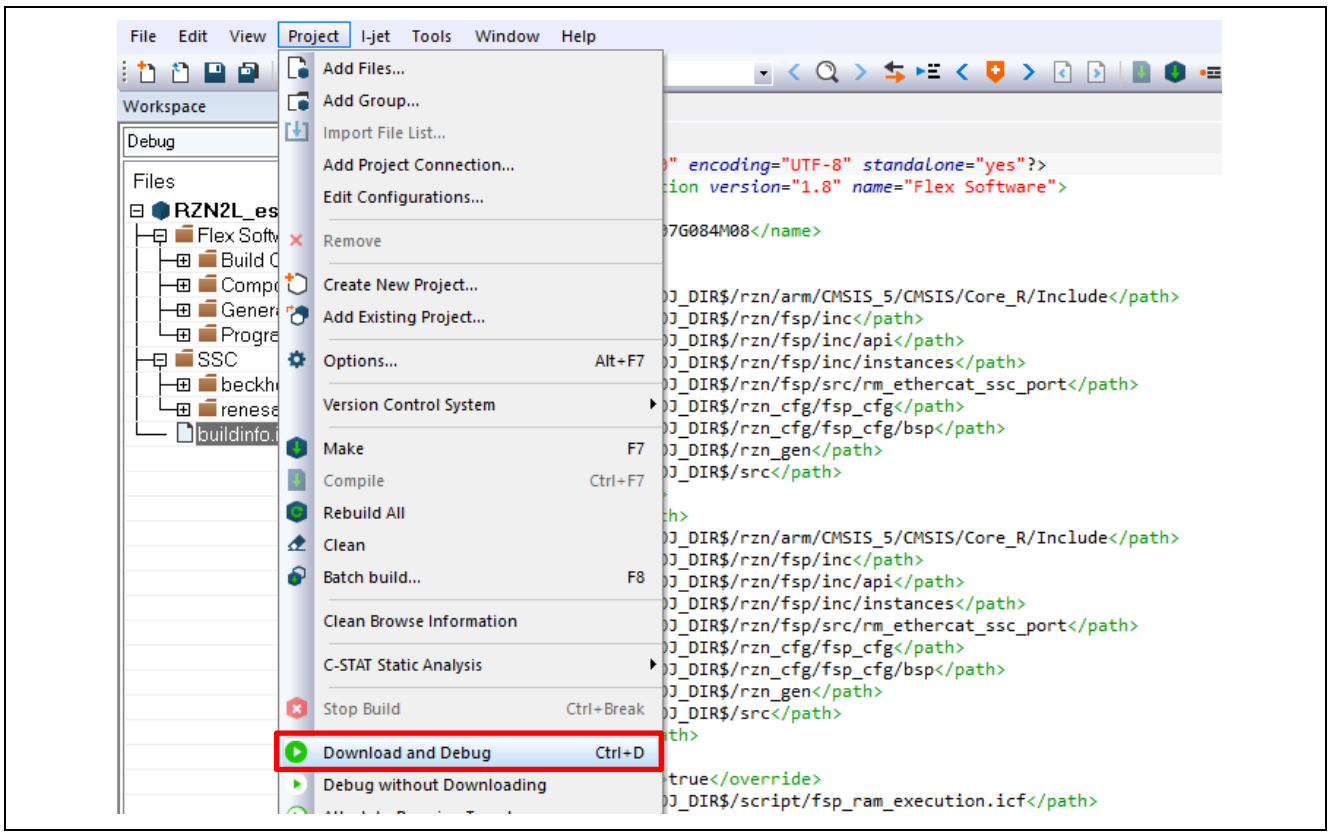


4. Select the “Rebuild All” item from the “Project” menu to rebuild the project.

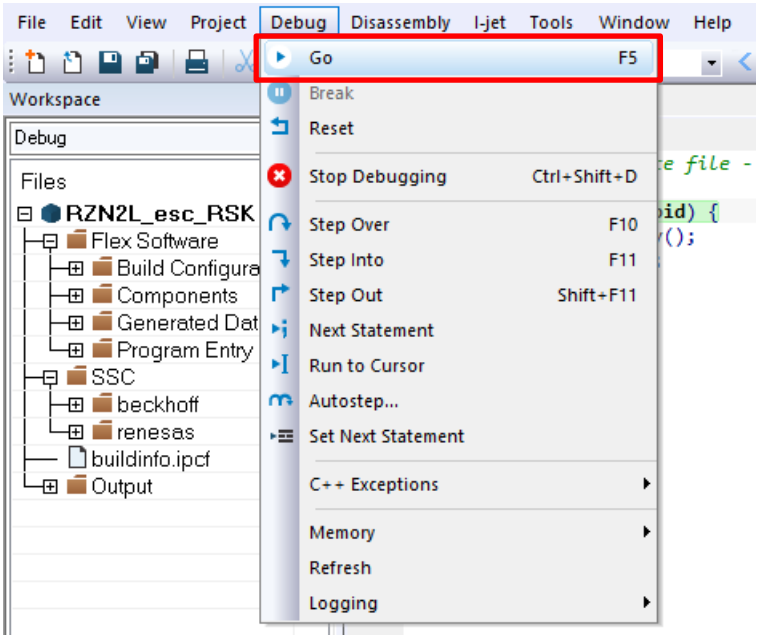


5. Press the “RESET” switch of the RZ/N2L Industrial Network SOM Kit.

6. While the board and I-jet are connected, click on the “Download and debug” button in the “Project” toolbar.



7. Press the "Resume" button for the project. Program is running.



3.2 Build and debug sample code for GCC

3.2.1 Erasing the flash memory

If you want to erase the flash memory on this SOM Kit using J-Link Commander, execute the following steps.

Open the J-Link Commander.

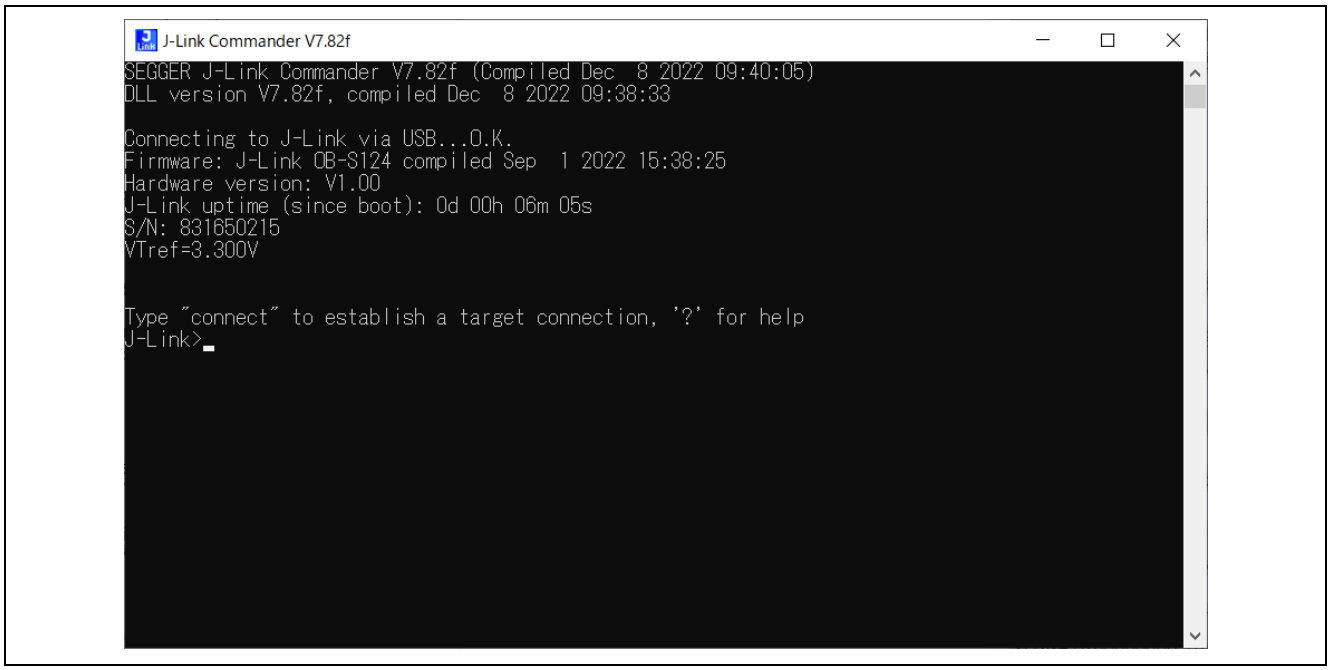


Figure 3-1 Open J-Link Commander

First, type “connect” to establish a target connection and press enter.

Next, specify the connection conditions as follows.

- Device> (Default = press enter)
- TIF>S
- Speed> (Default = press enter)

After that, confirm the message “Cortex-R52 identified.” Is displayed.

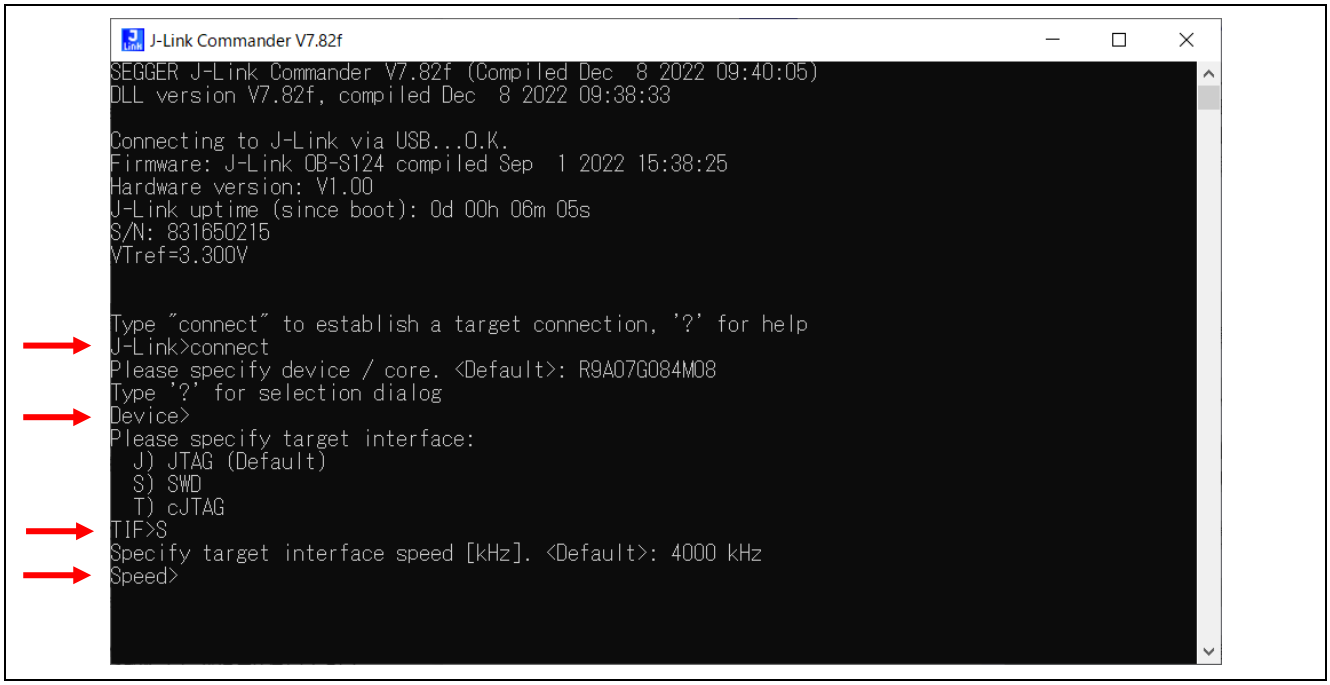


Figure 3-2 Connection conditions (1/2)

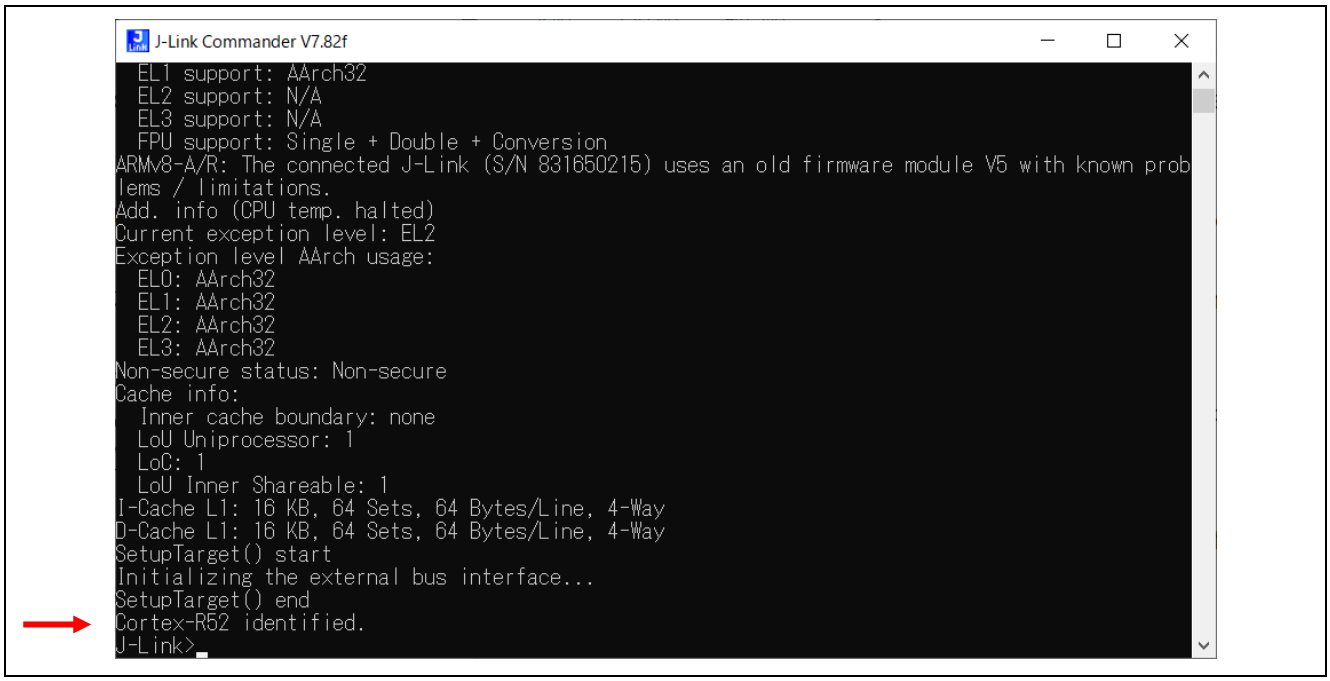


Figure 3-3 Connection conditions (2/2)

Use the commands below to enable flash erase and erase the flash memory.

- >exec EnableEraseAllFlashBanks
- >Erase 0x60000000, 0x60100000

After that, confirm the message “Erasing done.” Is displayed.

Enter “q” to exit J-Link Commander.

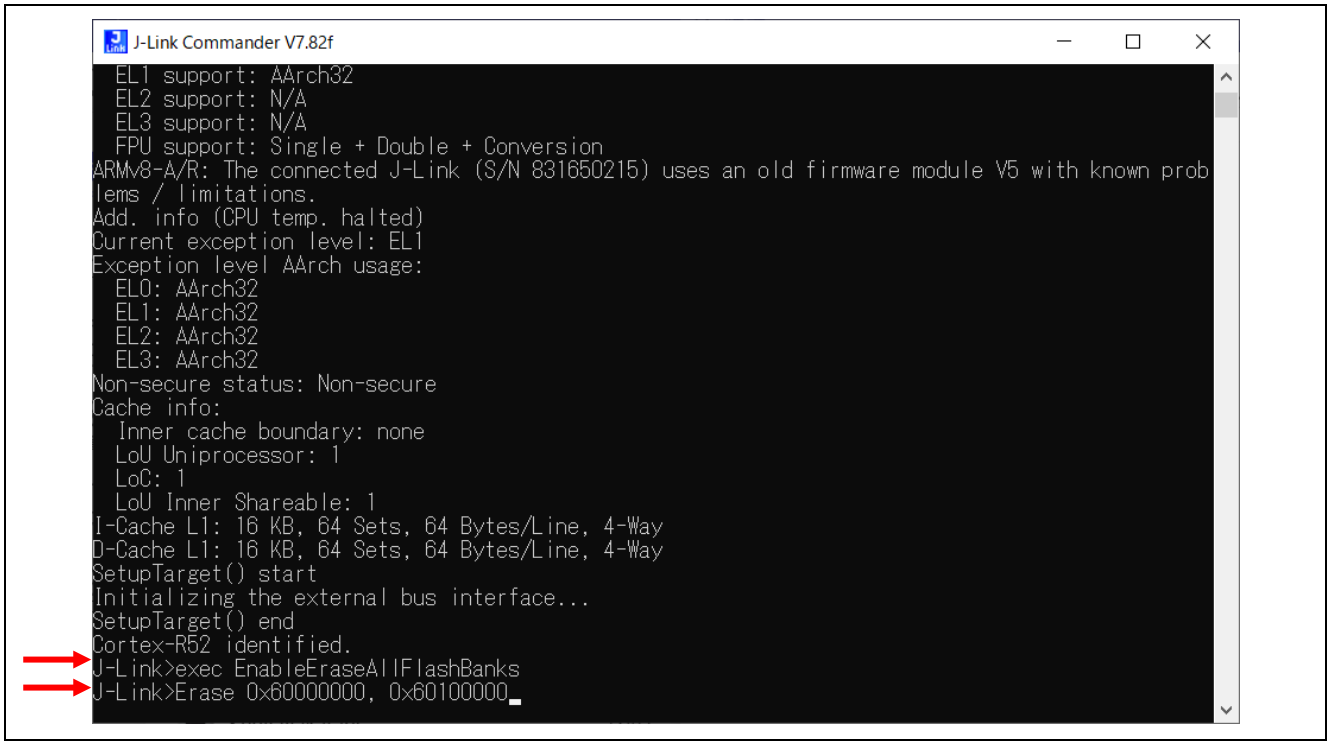


Figure 3-4 Erase flash memory (1/2)

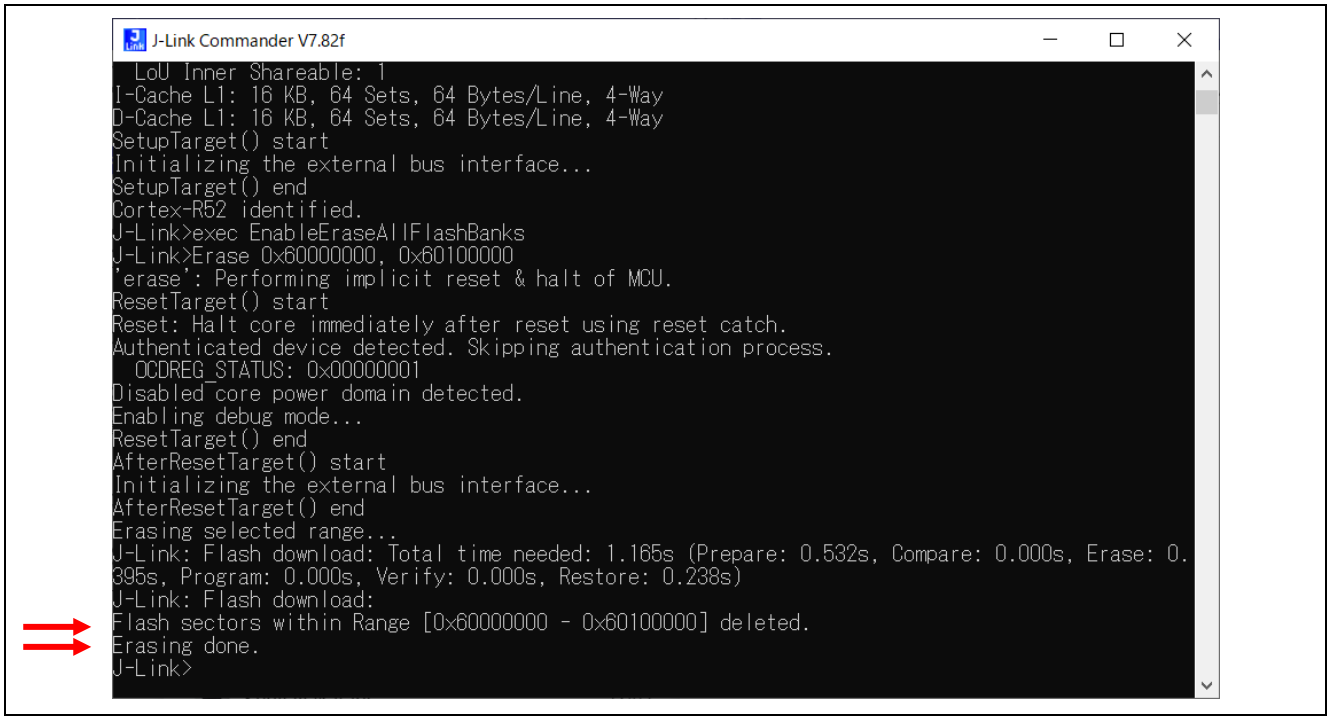


Figure 3-5 Erase flash memory (2/2)

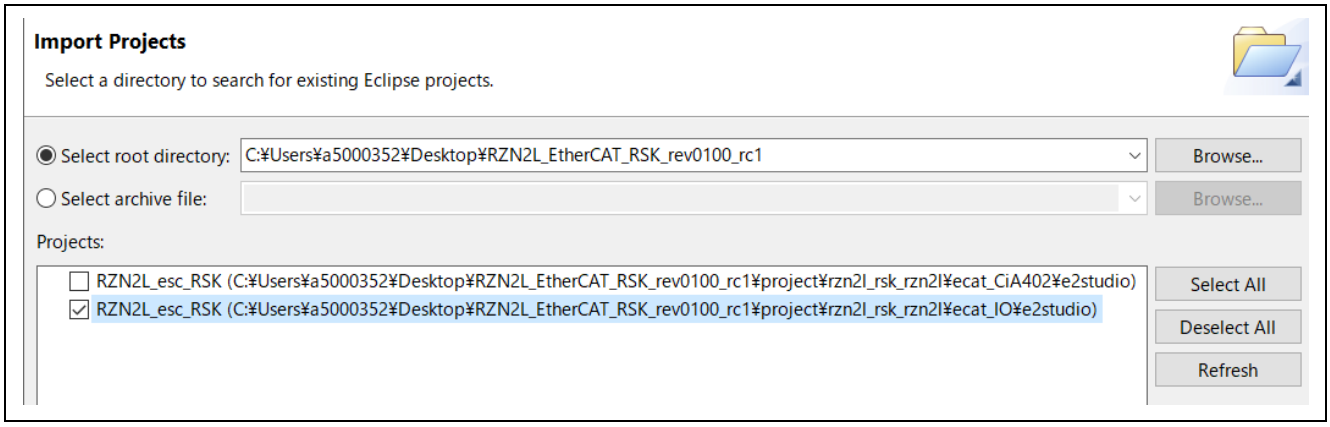
3.2.2 Project build and debug

Build and load the sample code using Renesas Electronics e² studio.

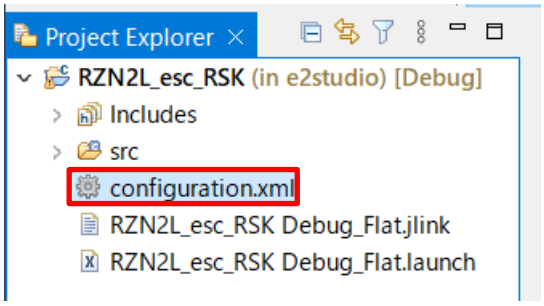
Note). Please install e2studio and adapt the FSP_Packs_v1.0.0 in advance.
Refer to the latest getting started guide.(R01an6434ejxxxx- rzt2-rzn2.pdf)

Replace the project name in the figure with the project name of this sample project.

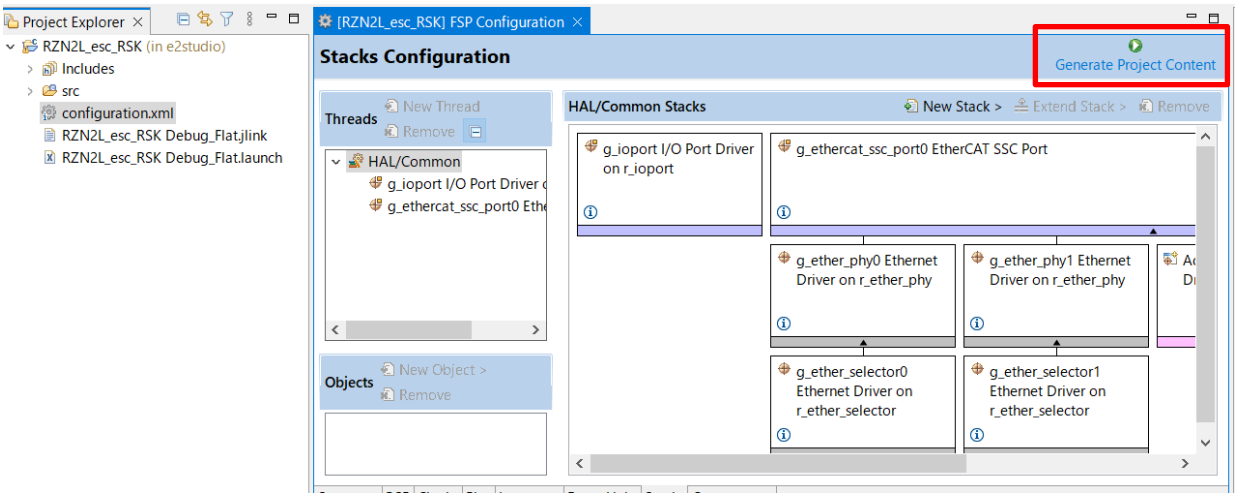
1. Import the sample project. After the program is started, by selecting [File] → [Import] → [Existing Projects into Workspace]. Check the "select root directory" and select “HTTP_server\e2studio\RZN2L_SOM_HTTP_server” folder →[Finish].



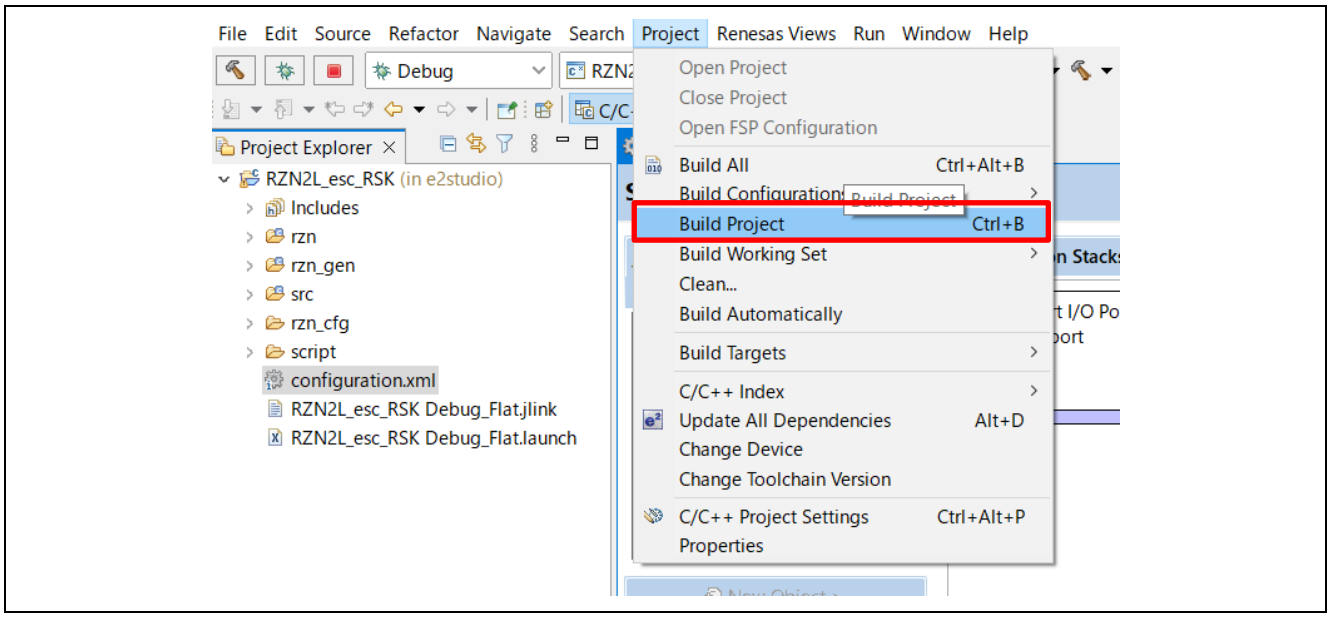
2. Open "cofiguration.xml" in the "RZN2L_SOM_HTTP_server " project



3. Generate the code with "Generate Project Content".

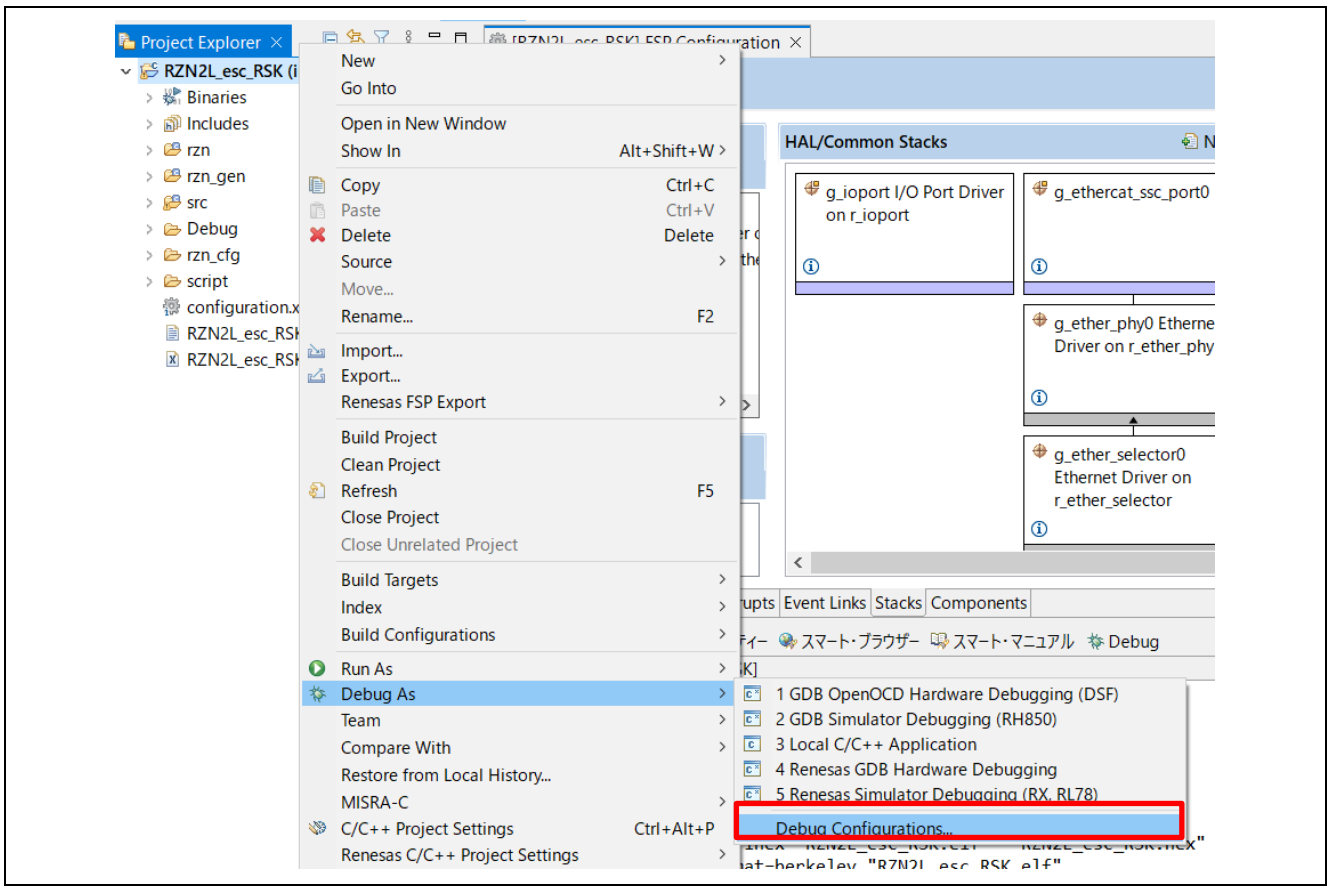


4. Select and build the "RZN2L_SOM_HTTP_server" project.

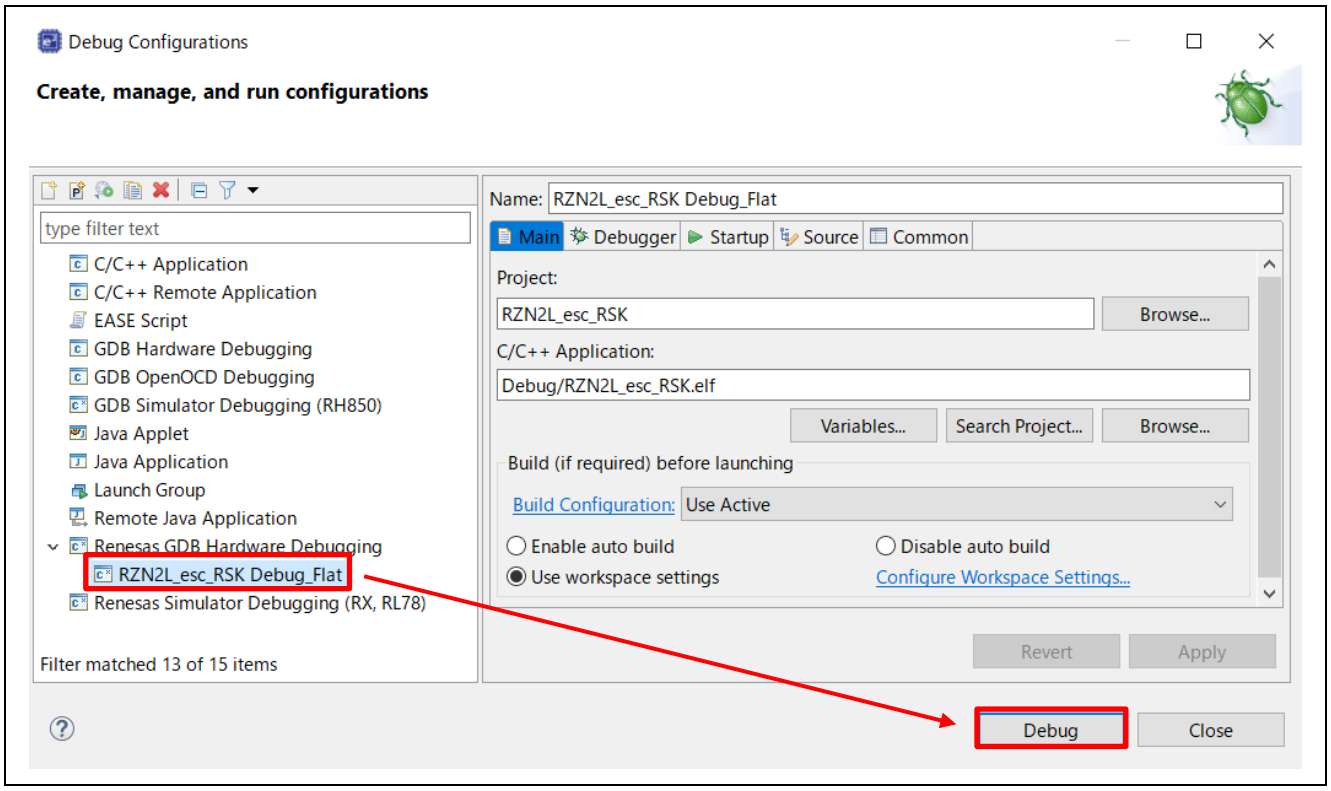


5. Press the “RESET” switch of the RZ/N2L Industrial Network SOM Kit.

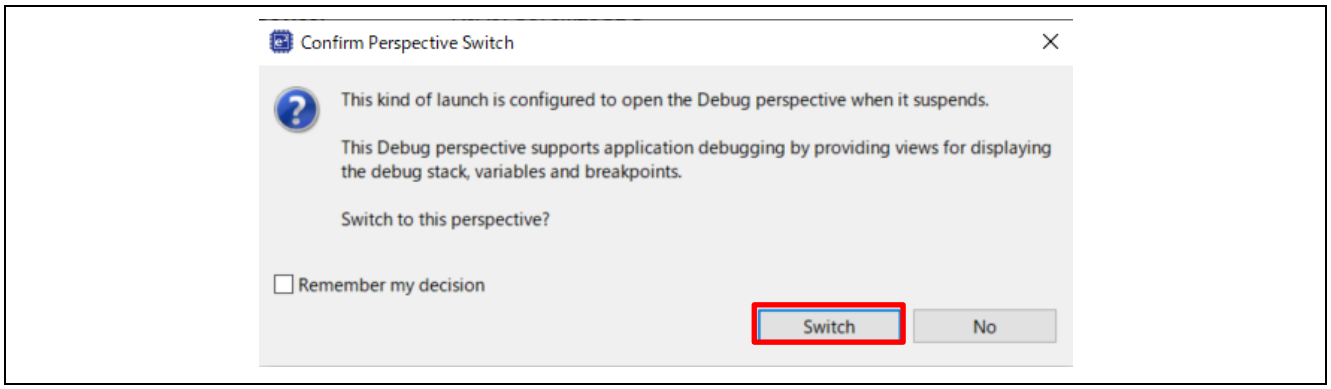
6. Connect J-Link to the SOM Kit, start debugging in the following procedure.
In [Project Explorer] view, right click the node of project to be debugged and select [Debug As] → [Debug Configurations].



[Renesas DBG Hardware Debugging] → [RZN2L_SOM_HTTP_server Debug_Flat] item, then press [Debug]



Following dialog will appear, so switch to the debug screen.



7. Press the "Resume" button. Program is running.

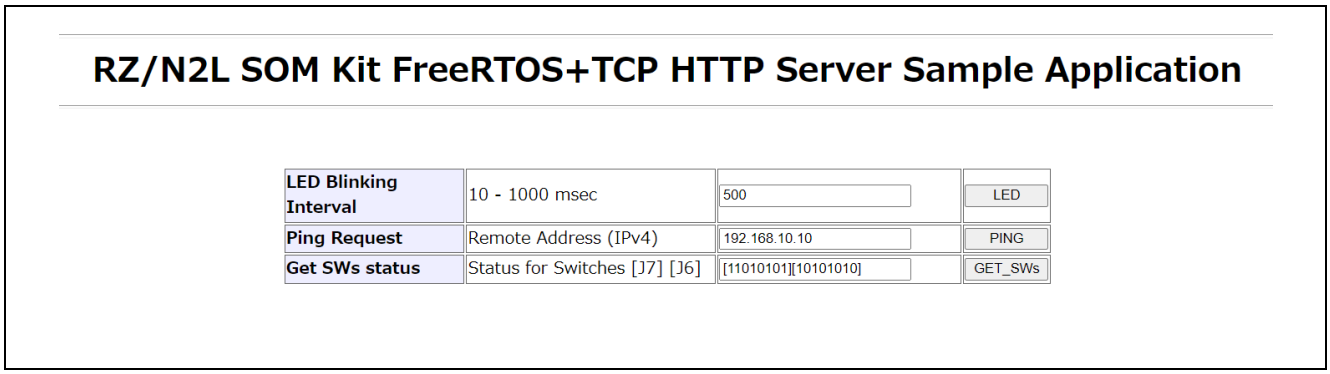
4. Software

Set the IP address of the PC in advance as follows.
IP address : 192.168.10.10
Subnet mask : 255.255.255.0

4.1 Application Operation

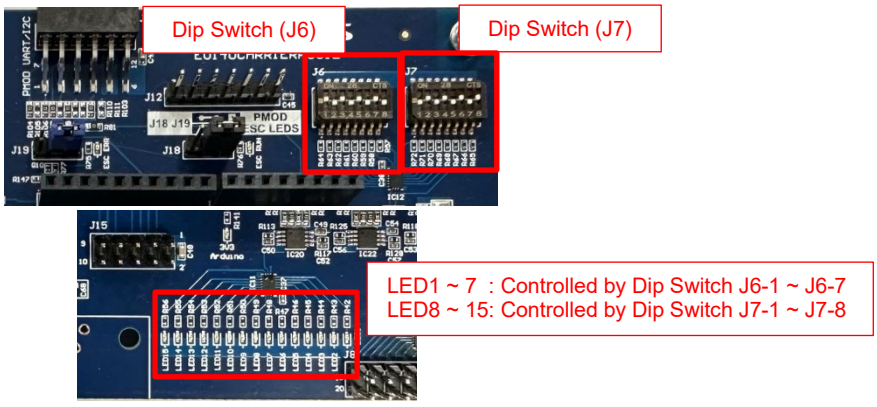
After running the sample program, you can confirm the web page sent from this SOM Kit by accessing 192.168.10.100 with a browser like below figure.

- LED Blinking Interval : Enter LED Blinking Interval between 10ms to 1000ms.
- Ping Request : Enter the IPv4 address to send Ping from RZ/N2L.
- Get SWs status : Display the current Dip Switch (J6 and J7) state.
  ON: 0, OFF: 1

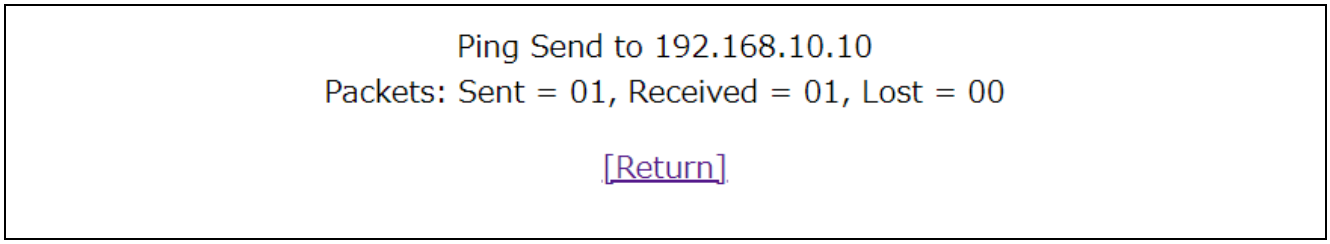


In the sample program, the LED blinks at intervals specified by the HTTP server.

The blinking LED is determined by the Dip Switch value.
J6-1 ~ J6-7 correspond to LED1 ~ LED7, J7-1 ~ J7-8 correspond to LED8 ~ LED15.
When the Dip Switch is ON, the LED is turned off. When Dip Switch is OFF, the LED blinks.



It is also possible to send a Ping request from the kit to the PC.
If the ping request is successful, the following screen will be displayed.



4.2 Notes on the sample program

4.2.1 Writing the sample program to the flash memory

When this sample program is executed, the program is written to the flash memory of this SOM Kit and can be debugged.

In this sample program, code for debugging using flash boot is inserted at the beginning of the startup code. This code is a software loop inserted to prevent the program written at debug connection from running before debugging.

For detailed information, see “Appendix. How to debug FSP project with flash boot mode” in Getting started with Flexible Software Package.

```
BSP_TARGET_ARM BSP_ATTRIBUTE_STACKLESS void system_init (void)
{
#if 1
    /* This software loops are only needed when debugging. */
    __asm volatile (
        "    mov   r0, #0                          \n"
        "    movw  r1, #0xf07f                     \n"
        "    movt  r1, #0x2fa                      \n"
        "software_loop:                            \n"
        "    adds  r0, #1                          \n"
        "    cmp   r0, r1                          \n"
        "    bne   software_loop                   \n"
        ::: "memory");
#endif

     ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
}
```

4.2.2 About SCI_I2C module

This sample program uses simple I2C mode of SCI to communicate with GreenPAK.
RZ/N2L FSP v1.1.0 does not support SCI_I2C driver, so SCI_I2Cdriver is placed under the src folder independently from FSP.

5. Appendix: FSP Configuration for VSC8531

RZ/N2L Industrial Network SOM Kit has VSC8531 as PHY chip.
If reconfiguring by latest FSP, FSP configuration and source code needs to change from default.

(1) Regenerate source files by lates FSP

Remove the following four folders. After that, open the project according to section 5.

- When using e2studio, \project\rzn2l_som\ecat_CiA402\e2studio
- When using EWARM, \project\rzn2l_som\ecat_CiA402\ewarm

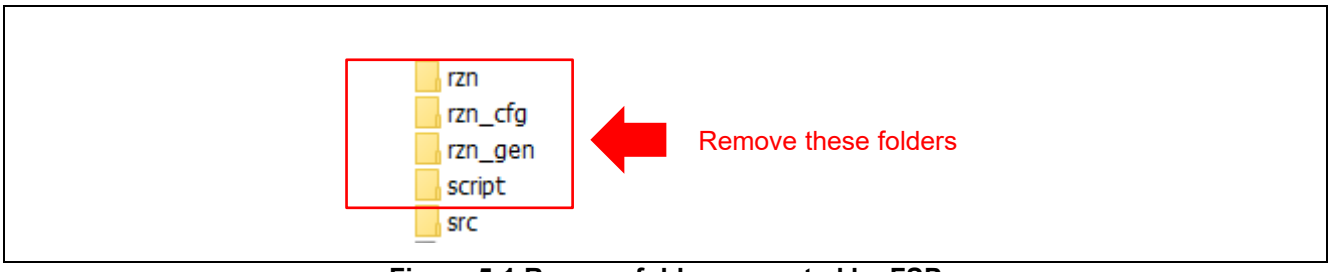


Figure 5-1 Remove folder generated by FSP

(2) Change ethernet driver configuration for VSC8531

Configure g_ether_phy0 Ethernet Driver on r_ether_phy for VSC8531 as shown in Figure 5-2.
Configuration value for VSC8531 shows in Table 5-1.

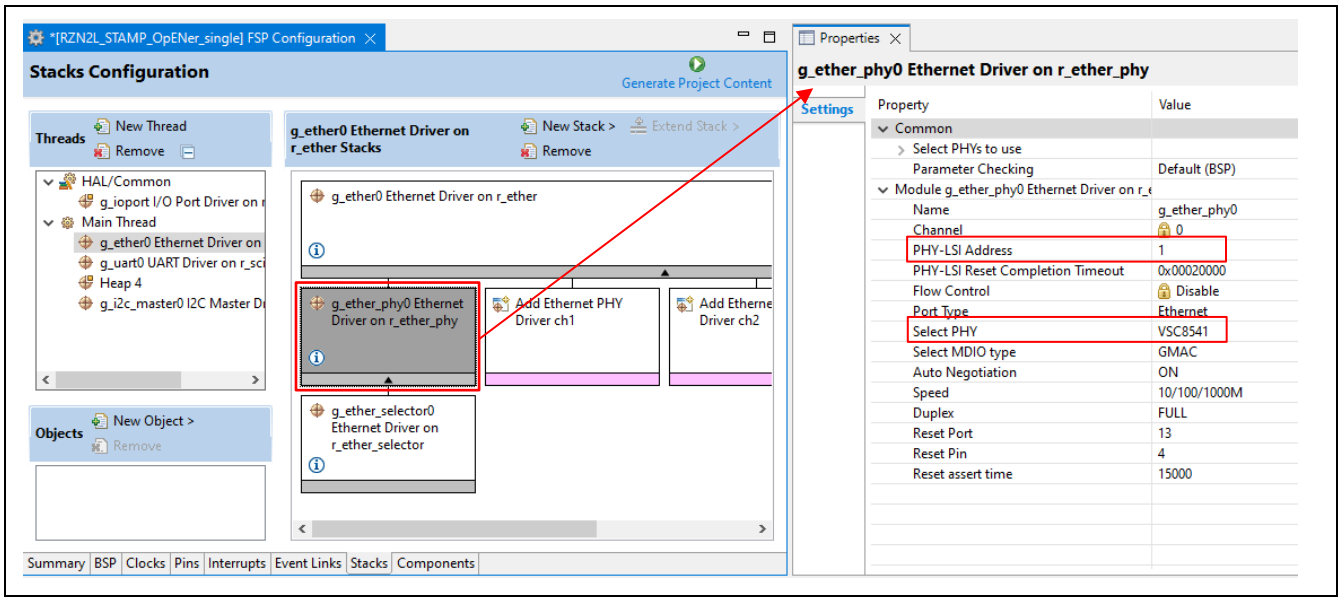


Figure 5-2 Ethernet Driver Configuration for VSC8531 (e.g. ETH0)

Table 5-1 FSP Configuration Value for VSC8531

Items	Default value	Config value for VSC8531	
		ETH0	ETH1
PHY-LSI Address	0	0	1
Select PHY	Default	VSC8541	VSC8541

(3) Add initialization code for VSC8531

The following code for VSC8531 initialization should be added to “ether_phy_targets_initialize_vsc8541” function in rzn/fsp/src/r_ether_phy/r_ether_phy.c.

The inclusion of “board_som.h” is aiso required for code activation.

```
#include "board_som.h"
                                        ~~ Omission ~~

void ether_phy_targets_initialize_vsc8541 (ether_phy_instance_ctrl_t * p_instance_ctrl)
{
                                        ~~ Omission ~~

    /* LED Behavior */
    reg  = ether_phy_read(p_instance_ctrl, ETHER_PHY_REG_LED_BEHAVIOR);
    reg &= ~(1U << ETHER_PHY_REG_LED0_FEATURE_DISABLE_OFFSET);
    reg |= 1U << ETHER_PHY_REG_LED1_FEATURE_DISABLE_OFFSET;
    ether_phy_write(p_instance_ctrl, ETHER_PHY_REG_LED_BEHAVIOR, reg);
#if defined(BOARD_RZN2L_SOM_KIT)  /* for VSC8531 */
    /* select extended page 2 register */
    ether_phy_write(p_instance_ctrl,   ETHER_PHY_REG_EXTEND_GPIO_PAGE, 0x02);

    /* read WoL and MAC Interface Control */
    reg  = ether_phy_read(p_instance_ctrl, 0x1b);

    /* set control to slow */
    reg &= 0xFF9F;
    ether_phy_write(p_instance_ctrl, 0x1b, reg);

    /* Configure RX_CLK delay and TX_CLK delay to 2.0ns */
    ether_phy_write(p_instance_ctrl, ETHER_PHY_REG_EXPAGE2_RGMII_CTRL, 0x0044);

    /* select extended page 0 register */
    ether_phy_write(p_instance_ctrl,   ETHER_PHY_REG_EXTEND_GPIO_PAGE, 0x00);
#endif

}                                       /* End of function ether_phy_targets_initialize() */
```

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar 22, 2023	-	First edition issued
1.10	Aug 7, 2023	-	Support RZ/N2L FSP v1.2.0

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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