RZ/T2H and RZ/N2H Power Requirements

Design of Power Supply Circuits for RZ/T2H and RZ/N2H using DA9080, DA9220 and DA9217.

This document describes all the default register settings of the DA9080, DA9220, and DA9217, for supplying power to the RZ/T2H or RZ/N2H system and associated peripherals. It focuses primarily on DA9080's configuration with respect to the RZ/T2H and RZ/N2H power on/off requirements.

The DA9080 is a high-performance, low cost, five channel PMIC designed for 32-bit and 64-bit MCU / MPU applications. The internally compensated regulators provide a highly integrated, small footprint power solution for System-On-Module (SOM) applications.

DA9220 integrates two single-phase buck converters. Each has the capability to deliver up to 3 A output current at a 0.3 V to 1.9 V output voltage range.

DA9217 operates as a single-channel, dual-phase buck converter capable of delivering up to 6 A output current at a 0.3 V to 1.9 V output voltage range.

Higher output voltages (up to 3.3 V) can be achieved by DA9217 and DA9220 using an external feedback divider network.

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1. Terms and Definitions

ADC	Analog to digital converter
CH<x>	Channel <x>, where x = 1 to 4
LDO	Low drop out (regulator)
OTP	One time programmable
PG	Power good
SOM	System-on-Module
UQFN	Ultra-thin quad flat-pack no-lead (package)
WLCSP	Wafer level chip scale package

2. References

[1] DA9080_Datasheet, Renesas Electronics.

[2] DA9217_Datasheet, Renesas Electronics.

[3] DA9220_Datasheet, Renesas Electronics.

[4] RZ/T2H and RZ/N2H Group Datasheet, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

3. Power Requirements

The power on/off sequence and timings are illustrated in the figure and table below.

For power-up, initiate with a supply of 0.8 V (VDD08), followed by 1.8 V (VDD18 and AVDD), then 1.1 V, and finally 3.3 V (DDR_VDDQ and VDD33).

Ensure the power-up sequence is completed within 100 ms, maintaining the Reset signal (RES#) in a Low state throughout this process.

For power-down, release 1.1 V and 3.3 V (DDR_VDDQ and VDD33) first, followed by 0.8 V and 1.8 V (VDD08, VDD18, and AVDD). Complete the power-down sequence within 100 ms.
Ensure the rise time for each power supply during power-up exceeds 40 µs, and the fall time during power-down exceeds 10 µs.

Apply power supply voltages and reset signals with a monotonic increase. Avoid the application of negative voltage to power supply voltages. Provide a stable clock to the EXTAL/XTAL or EXTCLKIN pin when the reset signal (RES#) is driven high.

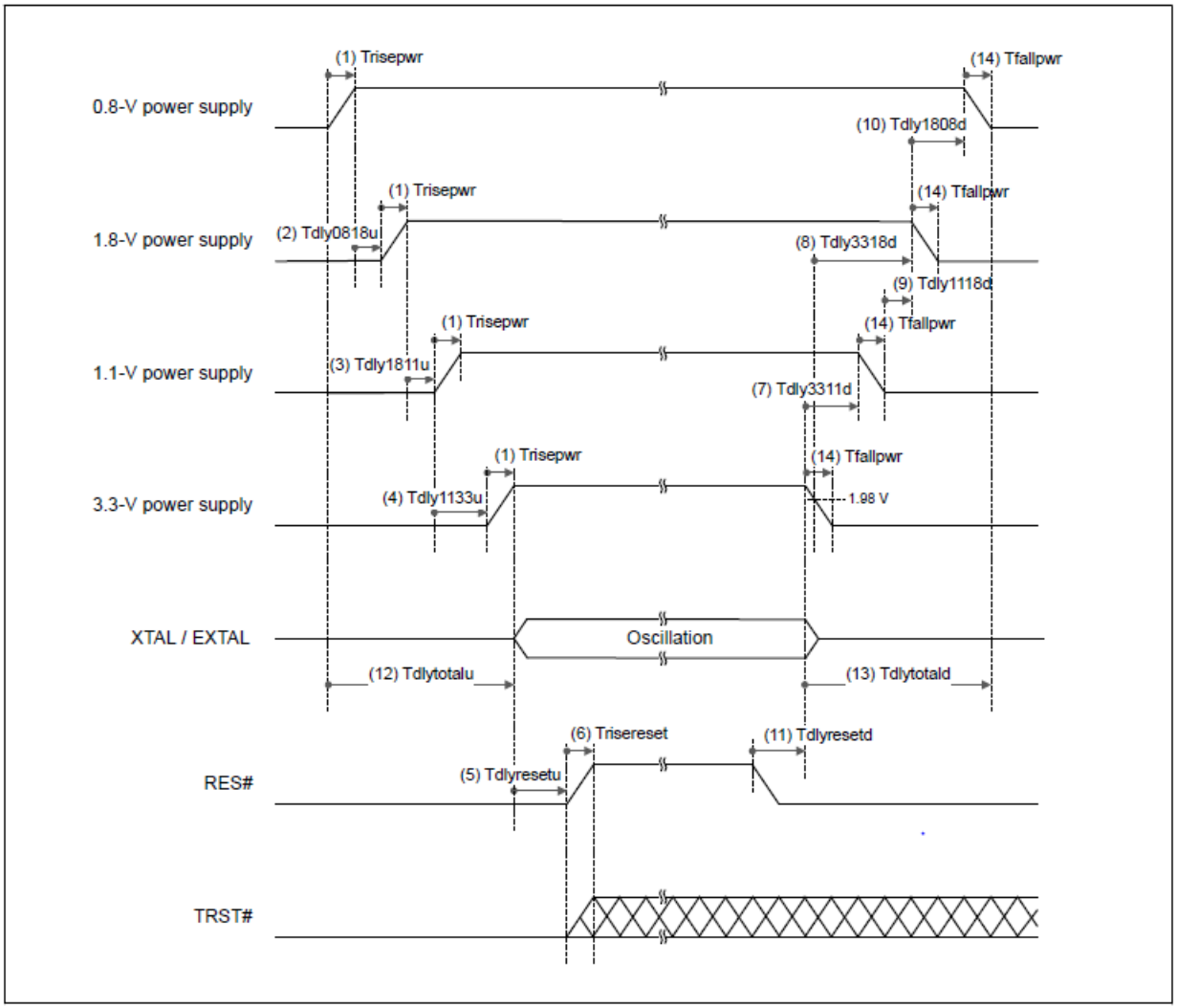

Figure 1. Period for Power Rise for RZ/T2H and RZ/N2H

Table 1. Power on/off Sequence Timing

No	Symbol	Description	Value		
			Min.	Typ.	Max.
(1)	Trisepwr	Rising time of the power supply voltage	40 µs		30 ms
(2)	Tdly0818u	Delay time from completion of rising of the 0.8 V power supply voltage to start of rising of the 1.8 V power supply voltage	1 µs		100 ms
(3)	Tdly1811u	Delay time from completion of rising of the 1.8 V power supply voltage to start of rising of the 1.1 V power supply voltage	0		100 ms
(4)	Tdly1133u	Delay time from start of rising of the 1.1 V power supply voltage to start of rising of the 3.3 V power supply voltage	0		100 ms
(5)	Tdlyresetu	Delay time from completion of rising of the 3.3 V power supply voltage to start of rising of RES#	10 ms		
(6)	Trisereset	Rising time of RES#			150 µs
(7)	Tdly3311d	Delay time from start of falling of the 3.3 V power supply voltage to start of falling of the 1.1 V power supply voltage	0		100 ms
(8)	Tdly3318d	Delay time from the time when 3.3 V power supply voltage drops below 1.98 V to start of falling of the 1.8 V power supply voltage	0		100 ms
(9)	Tdly1118d	Delay time from completion of falling of the 1.1 V power supply voltage to start of falling of the 1.8 V power supply voltage	0		100 ms
(10)	Tdly1808d	Delay time from start of falling of the 1.8 V power supply voltage to start of falling of 0.8 V power supply voltage	0		100 ms
(11)	Tdlyresetd	Delay time from start of falling of RES# to start of falling of the 3.3 V power supply voltage	10 µs		
(12)	Tdlytotalu	Startup time of all power supply voltage	0		100 ms
(13)	Tdlytotald	Shut down time of all power supply voltage	0		100 ms
(14)	Tfallpwr	Falling time of the power supply voltage	10 µs		30 ms

4. Power Supply Tree Diagram

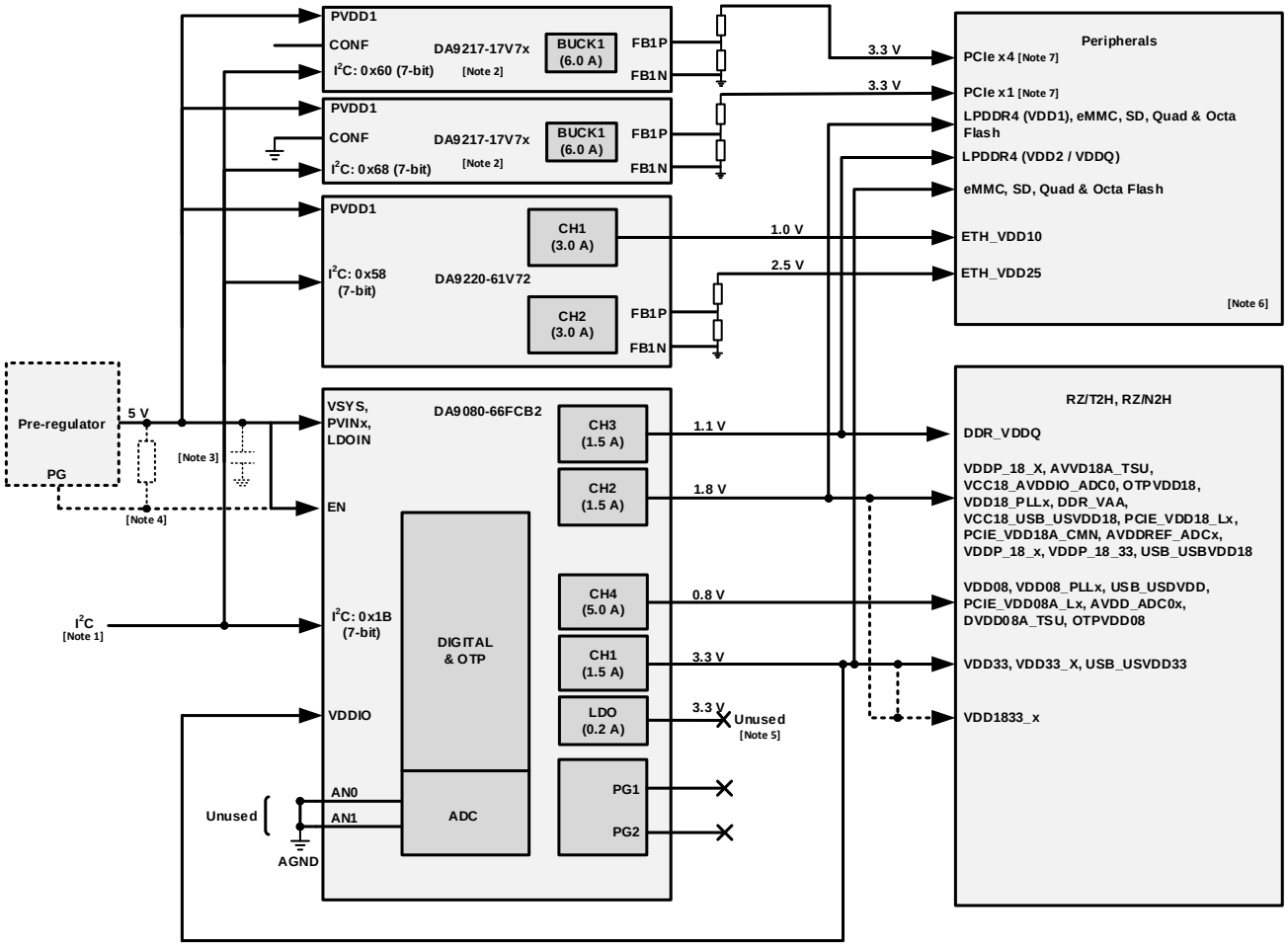

Figure 2. RZ/T2H or RZ/N2H Power Tree with PCI-E

Note 1 The I²C (SCL and SDA) should be connected to the RZ/T2H or RZ/N2H MPU.

Note 2 If PCI-E is unused, the two DA9217 devices can be removed from the system.

Note 3 A large bulk capacitor (100 µF ~ 1000 µF) should be added to the 5V input of DA9080 or to the input of the pre-regulator.

Note 4 If a pre-regulator is used to supply DA9080, it is recommended to connect the pre-regulator's PG to the DA9080's EN.

Note 5 The DA9080 LDO is shown as unused, though as it starts up in Slot 4; it could be used to enable the DA92xx devices.

Note 6 The peripherals included here are for example purposes; others may be able to be powered by the DA92xx/DA9080 devices. Designers should ensure their power demands are appropriate.

Note 7 PCIe 12V rails can be supplied by an external switching regulator (e.g., RAA211650).

5. Power On Sequence

Table 2. Power Sequence

	RZ/N2H or RZ/T2H: DA9080 Channel (Output Voltage)
Slot 1	DA9080 CH4 (0.80 V)
Slot 2	DA9080 CH2 (1.80 V)
Slot 3	DA9080 CH3 (1.10 V)
Slot 4	DA9080 CH1 (3.30 V) DA9080 LDO (3.30 V)

Note 1 The power down sequence is the reverse of the power up sequence.

Channel 1: DA9080 CH1 (3.30 V), Channel 2: DA9080 CH2 (1.80 V), Channel 3: DA9080 CH3 (1.10 V), Channel 4: DA9080 CH4 (0.80 V)

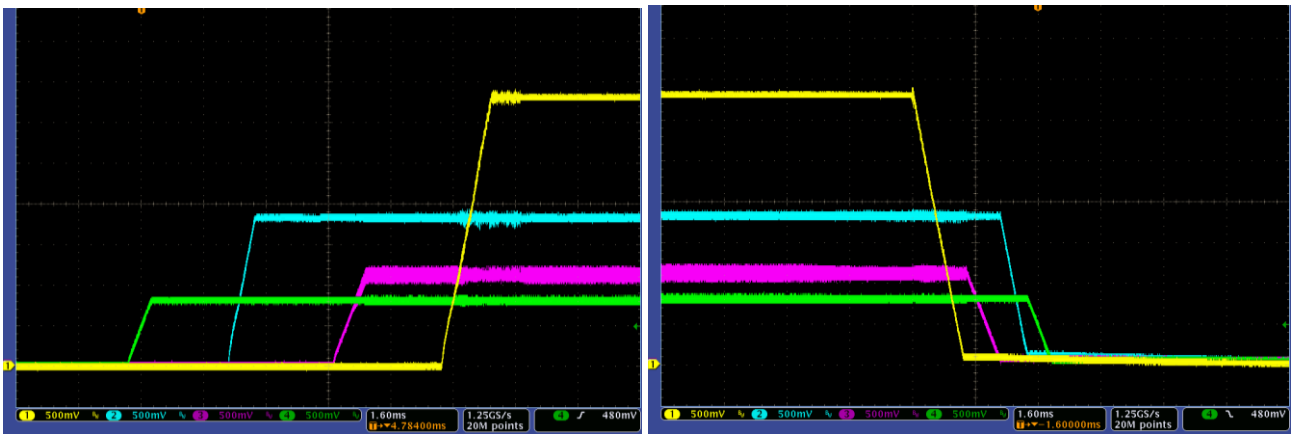

Figure 3. DA9080-66FCB2 Power Up/Down

6. Detailed Description

Table 3. Register Settings DA9080-68FCB2 (I2C slave address is 0x1B (7-bit))

Register Address	Register Name	Default Value	Description
0x04	PMC_ADC_ENABLE	0x00	ADC disabled
0x05	PMC_CH_EN	0x1F	CH1, CH2, CH3, CH4 and LDO enabled
0x07	PMC_VOUT_BUCK1	0x3C	VCH1 = 3.30 V
0x08	PMC_VOUT_BUCK2	0x0F	VCH2 = 1.80 V
0x09	PMC_VOUT_BUCK3	0x28	VCH3 = 1.10 V
0x0A	PMC_VOUT_BUCK4	0x00	VCH4 = 0.80 V
0x0B	PMC_PHASE_INTERLEAVING	0x88	BUCK1_PHASE = 0º BUCK2_PHASE = 180º BUCK3_PHASE = 0º BUCK4_PHASE = 180º
0x0C	PMC_BUCK_SEQ_GRP	0x27	CH1 = SLOT4, CH2 = SLOT2 CH3 = SLOT3, CH4 = SLOT1
0x0D	PMC_LDO_SEQ_GRP	0x03	LDO = SLOT4
0x0E	PMC_PG1	0x1C	CH2, CH3 and CH4 assigned to PG1

Register Address	Register Name	Default Value	Description
0x0F	PMC_PG2	0x03	CH1 and LDO assigned to PG1
0x10	PMC_DISCHARGE	0x1F	CH<x> and LDO discharge enabled
0x62	OTP_CONFIG_ID	0x66	OTP variant number: DA9080-66FCB2

Table 4. Register Settings DA9220-61V72 (I2C slave address is 0x58 (7-bit))

Register Address	Register Name	Default Value	Description
0x07	SYS_MASK_0	0x07	nIRQ interrupt, all masked
0x08	SYS_MASK_1	0xFF	nIRQ interrupt, all masked
0x09	SYS_MASK_2	0x07	nIRQ interrupt, all masked
0x0A	SYS_MASK_3	0x0F	nIRQ interrupt, all masked
0x0D	SYS_CONFIG_2	0x00	Over current latch-off function is disabled. PG and OC are not masked during DVC. 2CH-1PH + 1PH configuration
0x0E	SYS_CONFIG_3	0x02	Oscillator tuning (OSC_TUNE) is off. I2C_TIMEOUT is enabled
0x10	SYS_GPIO0_0	0x00	GPIO0 is set to CONF pin
0x20	BUCK_BUCK1_0	0x48	CH1 is off by default. DVC ramp-up and ramp-down slew rate is set to 20 mV/µs
0x21	BUCK_BUCK1_1	0x48	VOUT discharge resistor is disabled. Soft start and shut-down slew rate is set to 20 mV/µs
0x22	BUCK_BUCK1_2	0x05	ILIM is set to 5.5 A/phase
0x23	BUCK_BUCK1_3	0xBE	Maximum output voltage is set to 1.9 V
0x24	BUCK_BUCK1_4	0x0F	Buck is set to auto mode (both CH1_A_MODE and CH1_B_MODE). CH1_A_VOUT is selected by default
0x25	BUCK_BUCK1_5	0x64	CH1_A_VOUT = 1.00 V
0x26	BUCK_BUCK1_6	0x64	CH1_B_VOUT = 1.00 V
0x27	BUCK_BUCK1_7	0x03	Large ripple cancel
0x28	BUCK_BUCK2_0	0x48	CH2 is off by default. DVC ramp-up and ramp-down slew rate is set to 20 mV/µs
0x29	BUCK_BUCK2_1	0x48	VOUT discharge resistor is disabled. Soft start and shut-down slew rate is set to 20 mV/µs
0x2A	BUCK_BUCK2_2	0x05	ILIM is set to 5.5 A/phase
0x2B	BUCK_BUCK2_3	0xBE	Maximum output voltage is set to 1.9 V
0x2C	BUCK_BUCK2_4	0x0F	Buck is set to auto mode (both CH2_A_MODE and CH2_B_MODE). CH2_A_VOUT is selected by default
0x2D	BUCK_BUCK2_5	0x64	CH2_A_VOUT = 1.00 V
0x2E	BUCK_BUCK2_6	0x64	CH2_B_VOUT = 1.00 V
0x2F	BUCK_BUCK2_7	0x03	Large ripple cancel

Table 5. Register Settings DA9217-17V72, CONF = Low (I2C slave address is 0x68 (7-bits))

Register Address	Register Name	Default Value	Description
0x07	SYS_MASK_0	0x07	nIRQ interrupt, all masked
0x08	SYS_MASK_1	0xFF	nIRQ interrupt, all masked
0x09	SYS_MASK_2	0x07	nIRQ interrupt, all masked
0x0A	SYS_MASK_3	0x0F	nIRQ interrupt, all masked
0x0D	SYS_CONFIG_2	0x01	Over current latch-off function is disabled. PG is not masked during DVC. 1CH-2PH configuration
0x0E	SYS_CONFIG_3	0x02	Oscillator tuning (OSC_TUNE) is off. I2C_TIMEOUT is enabled
0x10	SYS_GPIO0_0	0x00	GPIO0 is set to CONF pin
0x20	BUCK_BUCK1_0	0x49	CH1 is enabled by default. DVC ramp-up and ramp-down slew rate is set to 20 mV/µs
0x21	BUCK_BUCK1_1	0x46	VOUT discharge resistor is enabled. Soft start slew rate is set to 10 mV/µs and shut-down slew rate is set to 20 mV/µs
0x22	BUCK_BUCK1_2	0x05	ILIM is set to 5.5 A/phase
0x23	BUCK_BUCK1_3	0xBE	Maximum output voltage is set to 1.9 V
0x24	BUCK_BUCK1_4	0x0F	Buck is set to auto mode (both CH1_A_MODE and CH1_B_MODE). CH1_A_VOUT is selected by default
0x25	BUCK_BUCK1_5	0xA5	CH1_A_VOUT = 1.65 V
0x26	BUCK_BUCK1_6	0xA5	CH1_B_VOUT = 1.65 V

Table 6. Register Settings DA9217-17V72, CONF = Hi-Z (I2C slave address is 0x60 (7-bits))

Register Address	Register Name	Default Value	Description
0x07	SYS_MASK_0	0x07	nIRQ interrupt, all masked
0x08	SYS_MASK_1	0xFF	nIRQ interrupt, all masked
0x09	SYS_MASK_2	0x07	nIRQ interrupt, all masked
0x0A	SYS_MASK_3	0x0F	nIRQ interrupt, all masked
0x0D	SYS_CONFIG_2	0x01	Over current latch-off function is disabled. PG is not masked during DVC. 1CH-2PH configuration
0x0E	SYS_CONFIG_3	0x02	Oscillator tuning (OSC_TUNE) is off. I2C_TIMEOUT is enabled
0x10	SYS_GPIO0_0	0x00	GPIO0 is set to CONF pin
0x20	BUCK_BUCK1_0	0x49	CH1 is enabled by default. DVC ramp-up and ramp-down slew rate is set to 20 mV/µs
0x21	BUCK_BUCK1_1	0x46	VOUT discharge resistor is enabled. Soft start slew rate is set to 10 mV/µs and shut-down slew rate is set to 20 mV/µs
0x22	BUCK_BUCK1_2	0x05	ILIM is set to 5.5 A/phase
0x23	BUCK_BUCK1_3	0xBE	Maximum output voltage is set to 1.9 V

Register Address	Register Name	Default Value	Description
0x24	BUCK_BUCK1_4	0x0F	Buck is set to auto mode (both CH1_A_MODE and CH1_B_MODE). CH1_A_VOUT is selected by default
0x25	BUCK_BUCK1_5	0xA5	CH1_A_VOUT = 1.65 V
0x26	BUCK_BUCK1_6	0xA5	CH1_B_VOUT = 1.65 V

7. Variant Table and Ordering Information

Table 7. Variant Table

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9080-66FCB2	32 UQFN	5.0 x 5.0 by 0.5 mm pitch	Tape & Reel	6000
DA9220-61V72	24 WLCSP	2.48 x 1.68 by 0.4 mm pitch	Tape & Reel	4500
DA9217-17V72	24 WSLCP	2.48 x 1.68 by 0.4 mm pitch	Tape & Reel	4500

Revision History

Revision	Date	Description
1.0	Feb 26, 2025	First version.

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(Rev.1.0 Mar 2020)

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