Smart Analog IC 300/301

Features and Usage Examples (Comparison with Smart Analog IC 500 Series)

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Introduction

This application note describes the differences between the Smart Analog IC 300 series and the Smart Analog IC 500 series, features of the Smart Analog IC 300 series, and its usage.

Operation Verified Devices

Smart Analog IC 300 (RAA730300) and Smart Analog IC 301 (RAA730301)

Contents

1. Overview

1.1 General

Smart Analog is a group of products whose circuits and characteristics can be reconfigured by using software to enable support of many different types of sensors and drivers.

There are two types of Smart Analog products: the Smart Analog IC 500 series that operates on 3.0 V to 5.5 V, and the Smart Analog IC 300 series that operates on 2.2 V to 3.6 V. For each series, Renesas provides devices whose analog circuit configuration differs depending on the Smart Analog IC incorporated.

This application note first describes the differences between Smart Analog IC 300 and Smart Analog IC 500, and Smart Analog IC 301 and Smart Analog IC 501, each of which pair has a similar analog circuit configuration, and then describes the features of Smart Analog IC 300 and Smart Analog IC 301 and their usage.

The following shows the major features of Smart Analog IC 300: For details, see *2.1*.

- Two D/A converter channels are incorporated per configurable amplifier channel
- The configurable amplifier can be used as a general amplifier.
- The input mode of the configurable amplifier, general amplifier, low-pass filter, and high-pass filter can be switched between rail-to-rail input and P-ch single-ended input.
- The operating mode of the configurable amplifier can be switched for each channel.

The following shows the major features of Smart Analog IC 301: For details, see *3.1*.

- The input mode of the instrumentation amplifier can be switched between rail-to-rail input and P-ch single-ended input.
- Switches for offset voltage measurement are incorporated.

1.2 Conditions under which operation has been verified

The operation of the hardware and software described in this application note has been verified under the conditions shown below.

Table 1.1 Conditions under which operation has been verified

Parameter	Description
Devices used	Smart Analog IC 300 (RAA730300) Smart Analog IC 301 (RAA730301) RL78/G1A (R5F10ELE)
Evaluation board used	TSA-IC300 or TSA-IC301
Software	Smart Analog Easy Starter Ver. 2.0

1.3 Related application notes

Also refer to these documents when using this application note.

- *Smart Analog Evaluating Sensors By Using Smart Analog Easy Starter (Ver. 2.0) (R02AN0017E) Application Note*
- *Smart Analog IC 300 Selecting Amplifiers Based on Sensor Type (R02AN0016E) Application Note*

2. Functional Differences in Smart Analog IC 300

2.1 Differences from Smart Analog IC 500

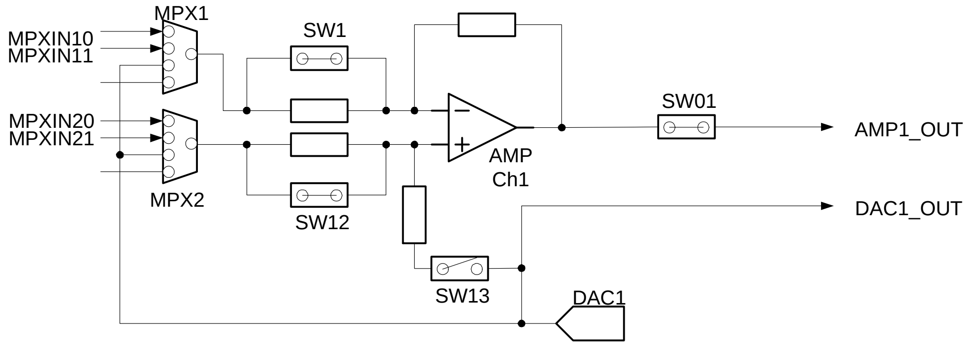
Table 2.1 shows the differences between Smart Analog IC 300 and Smart Analog IC 500. For details, see *RAA730300, Monolithic Programmable Analog IC Datasheet* and *RAA730500, Monolithic Programmable Analog IC Datasheet*.

Table 2.1 Differences between Smart Analog IC 300 and Smart Analog IC 500

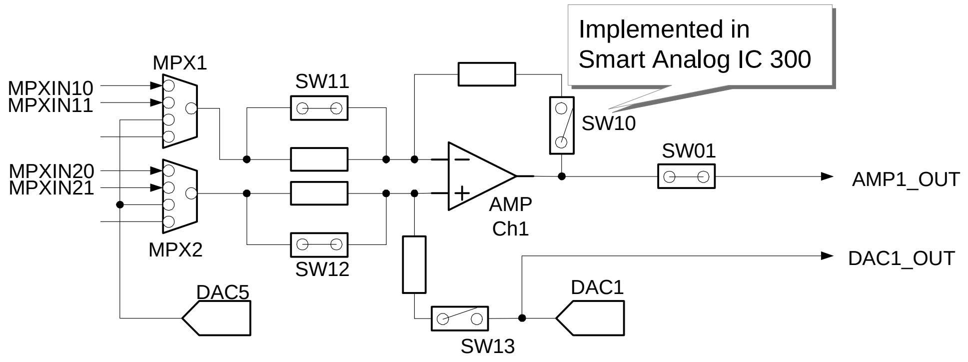
Description	Smart Analog IC 300	Smart Analog IC 500	Remark
Configuration of configurable amplifier	6 types (general amplifier configuration added)	5 types	See *2.2* for details.
General amplifier	2 channels	1 channel	See *2.3* for details.
Synchronous detection amplifier	Not available	1 channel	
D/A converter	7 channels	4 channels	See *2.4* for details.
Input mode setting	Configurable • Rail-to-rail input • P-ch single-ended input	Input mode is fixed. • P-ch single-ended input	See *2.5* for details.
Operating mode setting	Can be specified for each configurable amplifier	All amplifiers must be set to the same mode.	See *2.6* for details.
Gain when using instrumentation amplifier configuration	15.5 dB to 33.5 dB (Typ.)	20 dB to 54 dB (Typ.)	
Low-pass filter cutoff frequency	9 Hz to 900 Hz	9 Hz to 4.5 kHz	
Range of voltage output by variable output voltage regulator	1.8 V to 3.1 V (Typ.)	2.0 V to 3.3V (Typ.)	
Output voltage temperature coefficient for temperature sensor	–4 mV/°C (Typ.)	–5 mV/°C (Typ.)	
Operating voltage range	$2.2\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	$3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	

2.2 Configurable amplifier used as a general amplifier

The configurable amplifier incorporated in Smart Analog IC 300 can be used as a general amplifier by disabling all the related on-chip resistors. When the configurable amplifier is used as a general amplifier, various circuit configurations become possible by adding external components. On the other hand, the configurable amplifier incorporated in Smart Analog IC 500 cannot be used as a general amplifier because it does not have switches SWx0 (x = 1 to 3). Figure 2-1 shows a block diagram of configurable amplifier Ch1. Note that the direction of the switches in figure (b) applies to a general amplifier configuration.



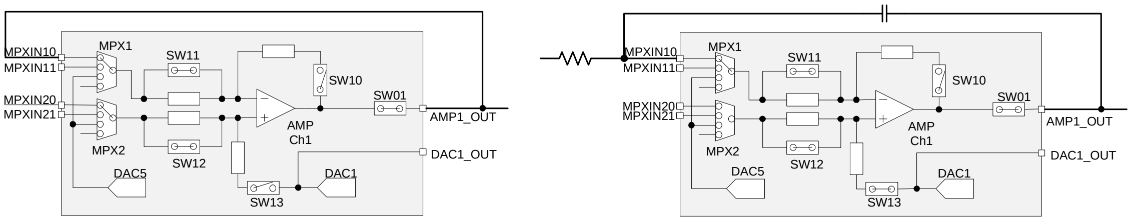
(a) Block Diagram of Configurable Amplifier Ch1 in Smart Analog IC 500



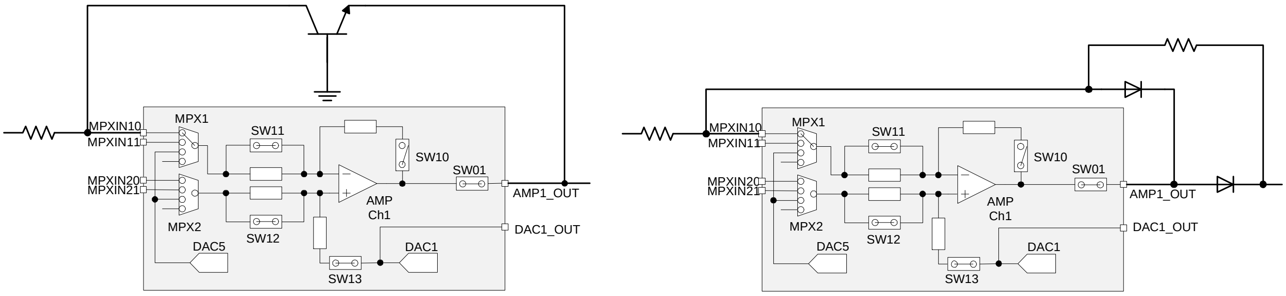
(b) Block Diagram of Configurable Amplifier Ch1 in Smart Analog IC 300

Figure 2-1 Block diagram of configurable amplifier Ch1

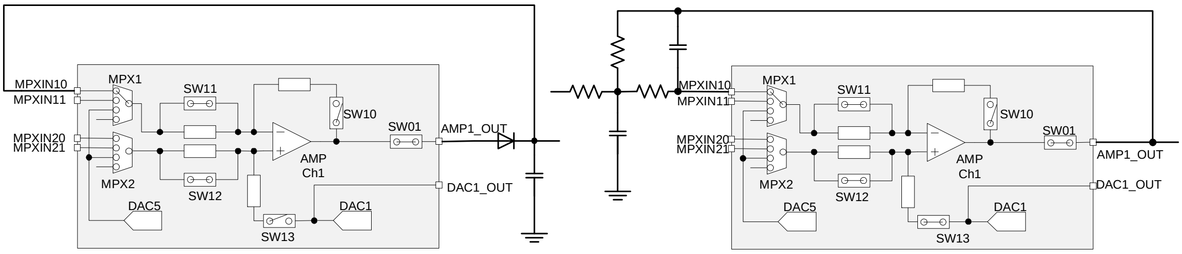
Figure 2-2 shows an example of a circuit configuration that can be achieved when using configurable amplifier Ch1 as a general amplifier.



(a) Buffer amplifier (b) Integrator



(c) Log amplifier (d) Half-wave rectifier



(e) Peak detector (f) Multiple feedback low-pass filter

Figure 2-2 Example uses of general amplifier

2.3 General amplifier (x 2 channels)

In addition to configuring the configurable amplifier as a general amplifier, Smart Analog IC 300 incorporates two general amplifier channels.

General amplifier Ch1 is provided to configure a standard general amplifier. On the other hand, general amplifier Ch2 can connect D/A converter Ch4 via its non-inverted input pin. By shorting SW53, the voltage output from D/A converter Ch4 can be used as the bias voltage for general amplifier Ch2. Because AMP5_OUT, the signal output from general amplifier Ch2, is connected to MPX8, it can be selected as the signal input to the low-pass and high-pass filters. Figure 2-3 shows a block diagram of the general amplifier.

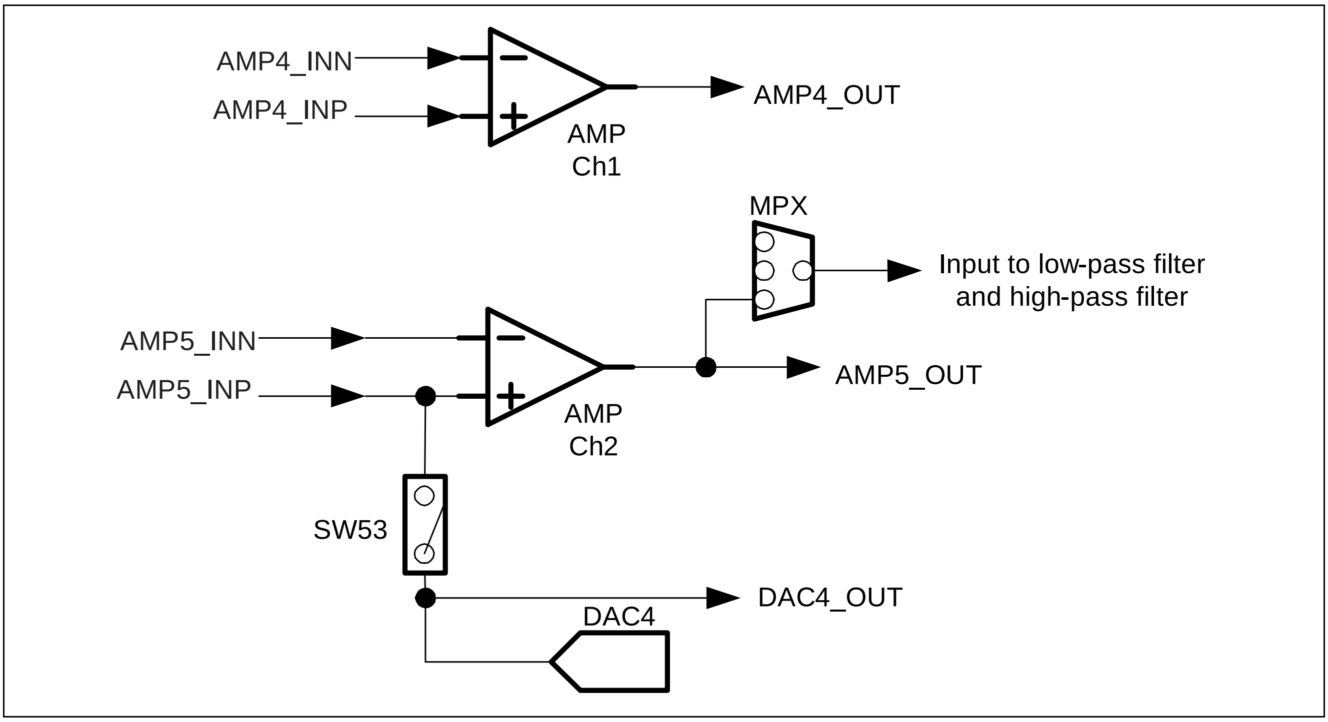


Figure 2-3 Block diagram of general amplifier

2.4 Example of using of two D/A converter channels

Smart Analog IC 500 incorporates one D/A converter channel per configurable amplifier channel. On the other hand, Smart Analog IC 300 incorporates two D/A converter channels per configurable amplifier channel. Due to this, the output voltage can be finely adjusted. Figure 2-4 shows a block diagram of configurable amplifier Ch1 of Smart Analog IC 300.

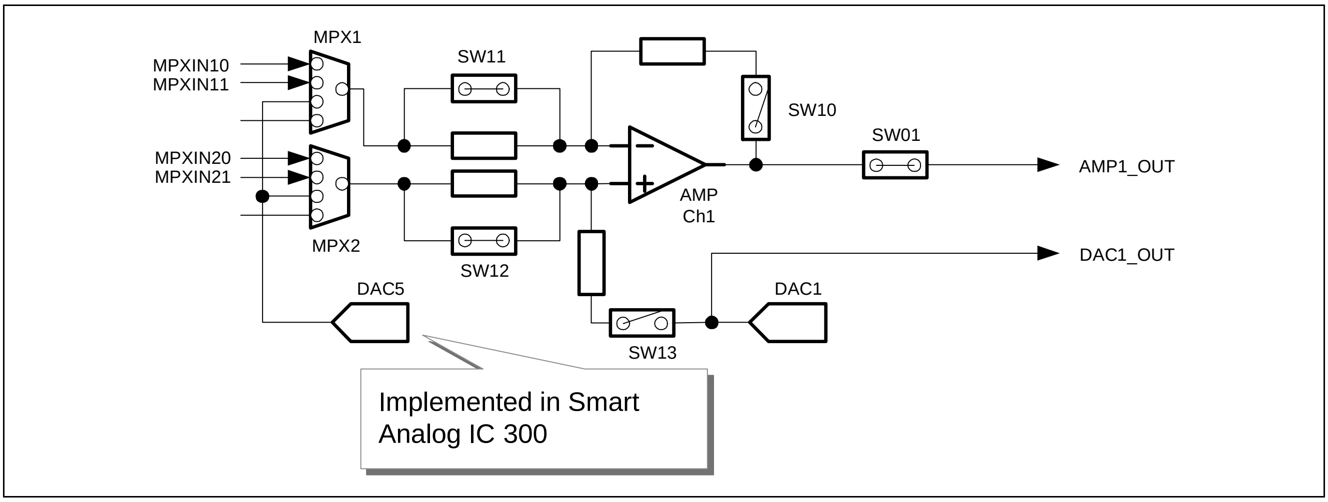


Figure 2-4 Block diagram of configurable amplifier Ch1

The differences in the output voltage adjustment step when using one D/A converter channel versus using two D/A converter channels are clear when amplifying a single-ended input signal with a high gain. These differences are described by using the examples below.

Generally, the voltage output from a D/A converter is used as the bias voltage of an amplifier. The D/A converter output voltage (V_{DAC}) can be expressed by using Formula 2-1.

$$V_{DAC} = \left\{ (\text{ref. voltage upper limit} - \text{ref. voltage } lower \text{ limit}) \times 2 \times \frac{1}{256} \right\} + 2 \times \text{ref. voltage } lower \text{ limit}$$

Formula 2-1

Here, if the upper and lower limits of the reference voltage for the D/A converter are set as VRB0 = VRB1 = VRT0 = VRT1 = 0, the upper limit of the reference voltage is $AV_{DD1}/2$, the lower limit of the reference voltage is AV_{SS}, and the minimum D/A converter step width ΔV_{DAC} can be expressed by using Formula 2-2.

$$\begin{aligned} \Delta V_{DAC} &= V_{DAC}(N+1) - V_{DAC}(N) \\ &= AV_{DD1} \times \frac{1}{256} \end{aligned}$$

Formula 2-2

When AV_{DD1} = 3.0 V, the adjustment width ΔV_{DAC} is approximately 11.7 mV.

Next, we will describe the output voltage adjustment step when using a non-inverting amplifier configuration and when using an inverting amplifier configuration.

The output voltage when using a non-inverting amplifier configuration, $V_{AMP\_OUTNonInvert}$, can be expressed by using Formula 2-3, with the sensor output voltage defined as V_{Sensor} and the gain of the non-inverting amplifier configuration defined as $G_{NonInvert}$. At this time, the D/A converter is connected to the inverted input pin of the amplifier.

$$V_{AMP\_OUT_{NonInvert}} = G_{NonInvert} \cdot V_{Sensor} - (G_{NonInvert} - 1) \cdot V_{DAC}$$

Formula 2-3

From Formula 2-3, the output voltage adjustment step when using a non-inverting amplifier configuration, $\Delta V_{AMP\_OUTNonInvert}$, can be expressed by using Formula 2-4.

$$\Delta V_{AMP\_OUT_{NonInvert}} = \left(G_{NonInvert} - 1\right) \cdot \Delta V_{DAC}$$ Formula 2-4

Similarly, the output voltage when using an inverting amplifier configuration, $V_{AMP\_OUTInvert}$, can be expressed by using Formula 2-5, specifying the sensor output voltage as V_{Sensor} and the gain of the inverting amplifier configuration as G_{Invert}. At this time, the D/A converter is connected to the non-inverted input pin of the amplifier.

$$V_{AMP\_OUT_{Invert}} = \left(1 + G_{Invert}\right) \cdot V_{DAC} - G_{Invert} \cdot V_{Sensor}$$ Formula 2-5

Formula 2-5From Formula 2-5, the output voltage adjustment step when using an inverting amplifier configuration, $\Delta V_{AMP\_OUTInvert}$, is Formula 2-6.

$$\Delta V_{AMP\_OUT_{Invert}} = \left(1 + G_{Invert}\right) \cdot \Delta V_{DAC}$$ Formula 2-6

In Formula 2-4 and Formula 2-6, the output voltage adjustment step of each inverter configuration, ΔV_{DAC}, is multiplied by a gain of -1 in the case of a non-inverting amplifier configuration, and by a gain of +1 in the case of an inverting amplifier configuration. Consequently, you can see that the output voltage adjustment step becomes larger as the gain increases.

Substituting real numbers into the calculation, the output voltage adjustment step when using a non-inverting amplifier configuration in which AV_{DD1} = 3.0 V and $G_{NonInvert}$ = 40.1 dB is approximately 1.17 V, and the output voltage adjustment step when using an inverting amplifier configuration in which AV_{DD1} = 3.0 V and G_{Invert} = 40 dB is approximately 1.18 V.

Using the above formulas, we can calculate that the output voltage adjustment step when using a non-inverting amplifier configuration or inverting amplifier configuration with a high gain will be at least 1 V, making adjustment difficult.

Next we will describe the bias adjustment width when using two D/A converter channels. A block diagram of a configuration in which configurable amplifier Ch1 and D/A converter channels Ch1 and Ch5 are used is shown in Figure 2-5 as an example.

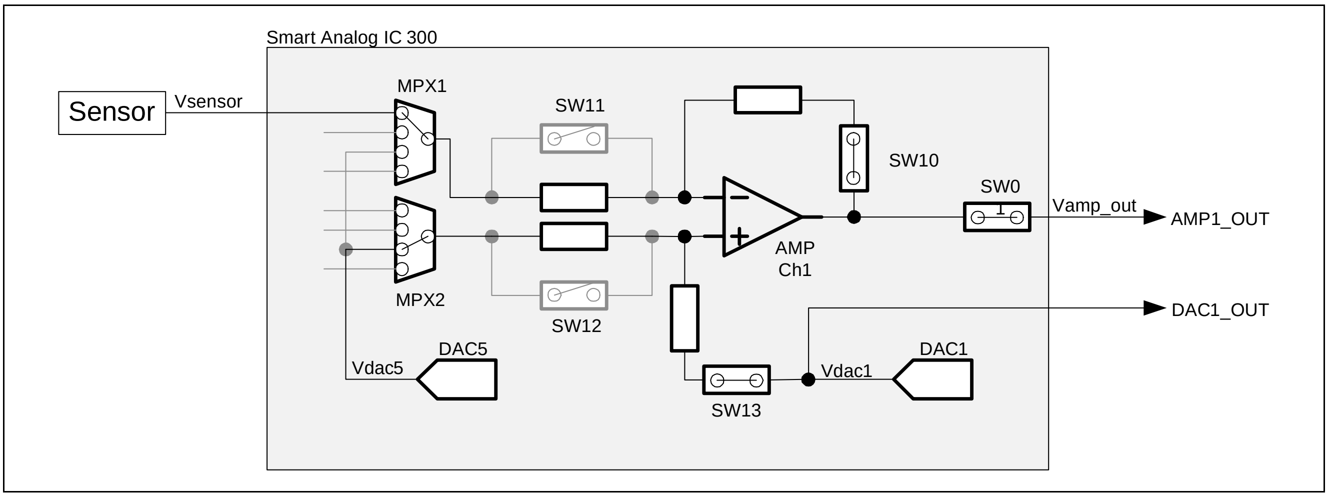


Figure 2-5 When two D/A converter channels are used

When Smart Analog IC 300 is configured as shown in Figure 2-5, its configuration is equivalent to the configuration of a differential amplifier. The amplifier output voltage V_{AMP_OUT} can be expressed by using Formula 2-7, with the gain defined as G_{Diff}, the voltage output from D/A converter Ch1 defined as V_{DAC1}, and the voltage output from D/A converter Ch5 defined as V_{DAC5}.

$$V_{AMP\_OUT} = G_{Diff} \cdot \left(V_{Sensor} - V_{DAC5}\right) + V_{DAC1}$$ Formula 2-7

From Formula 2-7, the variation width when the output voltage of D/A converter Ch1 is changed by 1 LSB (ΔV_{DAC1}), $\Delta V_{AMP\_OUT\_DAC1}$, and the variation width when the output voltage of D/A converter Ch5 is changed by 1 LSB (ΔV_{DAC5}), $\Delta V_{AMP\_OUT\_DAC5}$, is Formula 2-8 and Formula 2-9 respectively.

$$\Delta V_{AMP\_OUT\_DAC1} = \Delta V_{DAC1} \qquad \text{Formula 2-8}$$

$$\Delta V_{AMP\_OUT\_DAC5} = G_{Diff} \cdot \Delta V_{DAC5} \qquad \text{Formula 2-9}$$

Because ΔV_{DAC1} which equals $\Delta V_{AMP\_OUT\_DAC1}$ in Formula 2-8 is not multiplied by the gain of G_{Diff}, you can see that, unlike in Formula 2-4 and Formula 2-6, the offset output can be adjusted without being affected by amplifier gain.

Figure 2-6 shows an overview of how the bias voltage adjustment width changes according to the value set to the D/A converter.

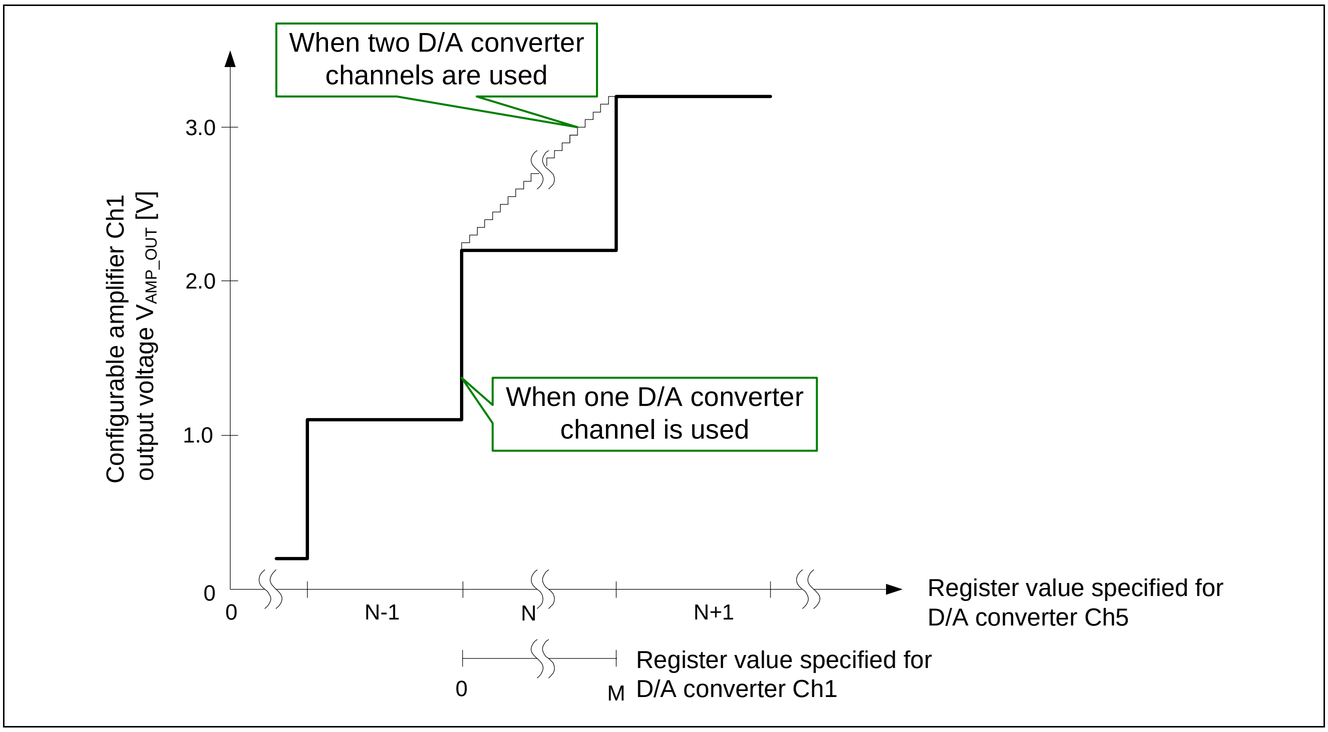


Figure 2-6 Overview of the bias voltage adjustment width when 40 dB is specified

When connecting a single-ended output sensor to an amplifier that uses two D/A converter channels, note the input impedance.

Because using two D/A converter channels configures a differential amplifier, the input impedance in the configurable amplifier becomes lower than that in non-inverting amplifiers. If the sensor incorporates an output impedance system, it might be affected by the input impedance of the differential amplifier. In this case, insert a non-inverting amplifier with a higher input impedance in the stage prior to the differential amplifier to avoid the effect of the impedance. Figure 2-7 shows an example of this kind of amplifier configuration. In Figure 2-7, configurable amplifier Ch1 is used as a buffer amplifier, and configurable amplifier Ch2 is used to amplify and adjust the bias voltage.

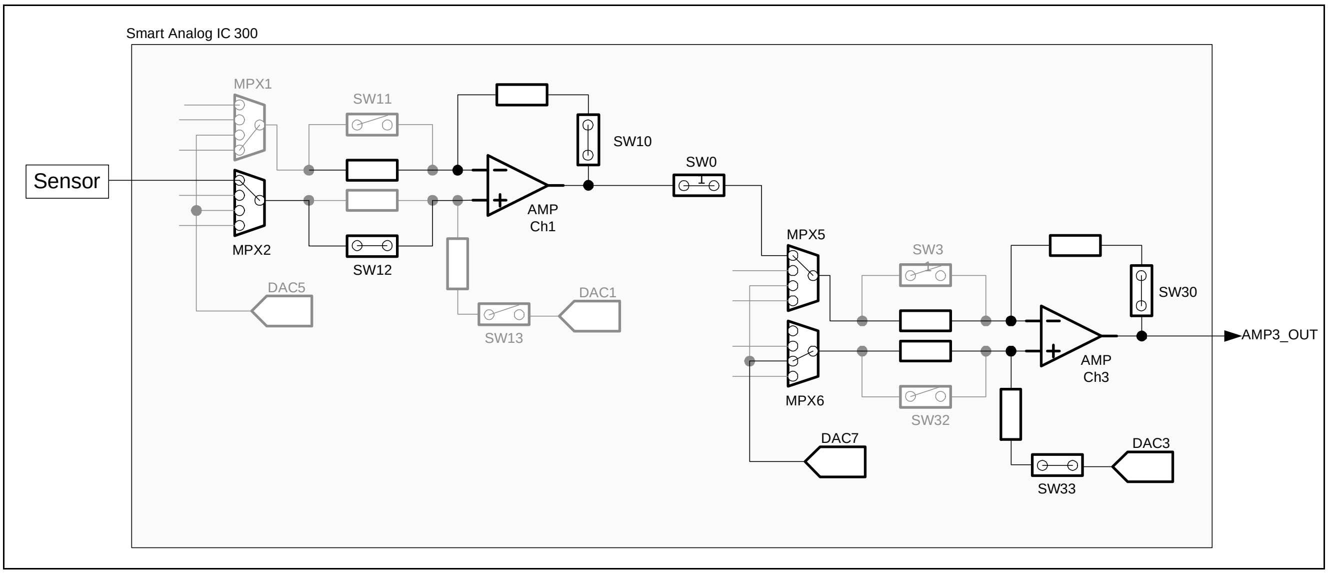


Figure 2-7 Example of amplifier configuration with high input impedance

2.5 Input modes

Smart Analog IC 300 incorporates an input mode control register. By using this register, the input mode of the configurable amplifier, general amplifier, low-pass filter, and high-pass filter can be selected from rail-to-rail input and P-ch single-ended input. Table 2.2 shows the characteristics of the input voltage for input mode. For details, see *RAA730300, Monolithic Programmable Analog IC Datasheet.*

Table 2.2 Input mode characteristics (excerpted from the datasheet)

Input voltage	Rail-to-rail input		P-ch single-ended input		Unit
	MIN	MAX	MIN	MAX	
Configurable amplifier channels Ch1 to Ch3 General amplifier	AGND1 – 0.05	AV$_{DD1}$ + 0.1	AGND1 – 0.05	AV$_{DD1}$ – 1.4	V
Low-pass filter High-pass filter	AGND3 + 0.2	AV$_{DD3}$ – 0.2	AGND3 + 0.2	AV$_{DD3}$ – 1.4	V

Figure 2-9 shows the actually measured waveforms. This figure shows the variation in the waveforms measured by applying a sine wave signal from a pulse generator and then using Smart Analog Easy Starter to change the input mode of configurable amplifier Ch1. Figure 2-8 shows the measurement scheme, and Table 2.3 shows the settings used for the measurement.

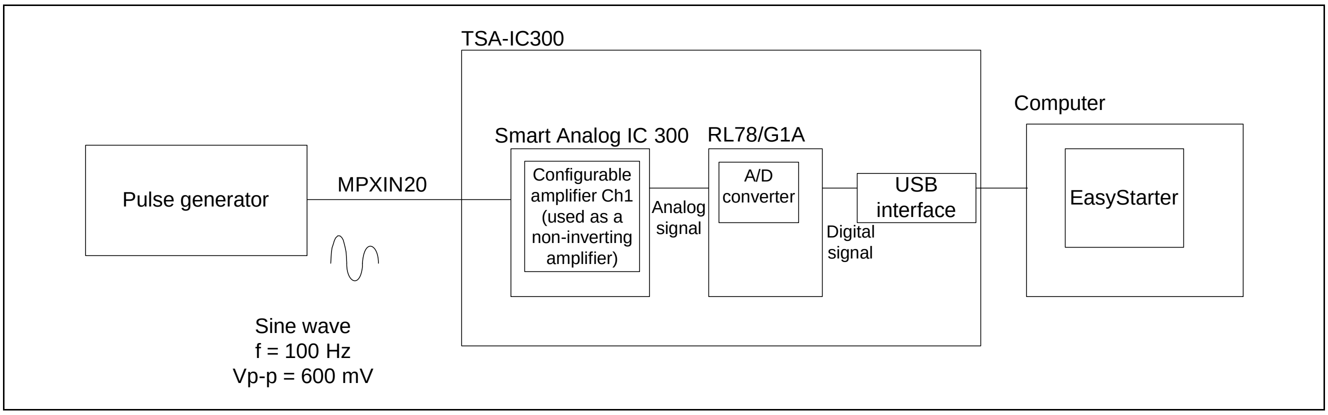


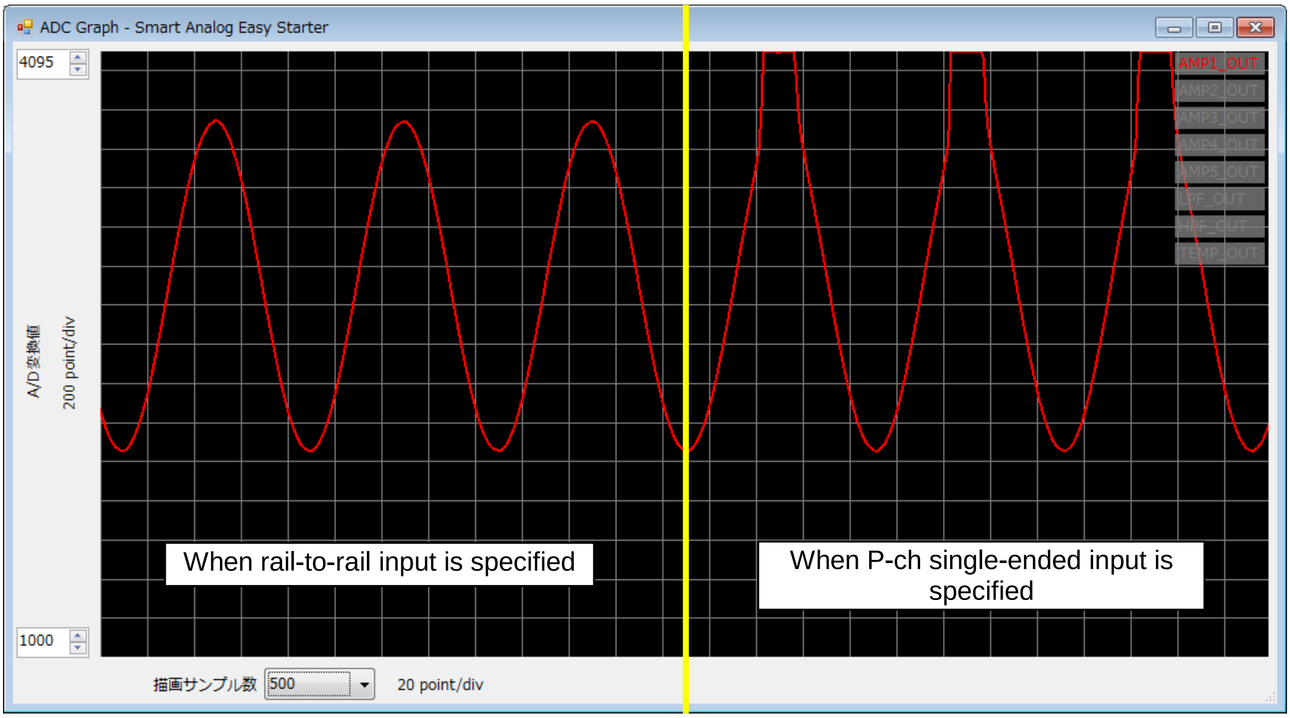
Figure 2-8 Measurement system diagram

Table 2.3 Settings for measurement in input mode

Settings specified in:	Description	Set value	
Pulse generator settings	Generating a sine wave signal	Signal	Sine wave
		Cycle	100 Hz
		DC offset	2.4 V
		Amplitude	600 mV$_{p-p}$
Easy Starter	Settings specified in Smart Analog IC 300	Amplifier used	Configurable amplifier Ch1
		Amplifier configuration	Non-inverting amplifier
		Signal input pin	MPXIN20
		Gain	9.5 dB
		D/A converter used	D/A converter Ch5
		D/A converter output voltage	193 (2.50 V)
		A/D conversion cycle	10 ms

If the input voltage exceeds the upper limit in P-ch single-ended input mode, the voltage output from the configurable amplifier is fixed at AV$_{DD}$.

Figure 2-9 shows an example of the measured waveforms. According to this figure, the amplifier output signal is measured as a sine wave in rail-to-rail input mode. In P-ch single-ended input mode, when the output voltage exceeds a specific voltage, the amplifier output signal is fixed at AVDD; that is, the upper limit of the input range is narrowed.



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When rail-to-rail input is specified

When P-ch single-ended input is specified

Figure 2-9 Waveforms of amplifier output voltage before and after input mode change

2.6 Operating modes

Power-saving operating modes can be selected for configurable amplifier channels Ch1 to Ch3. This setting can be changed by using the AMP operation mode control register, but it involves a trade-off between power saving and response speed.

In Smart Analog IC 500, the operating mode cannot be specified for each configurable amplifier channel. In Smart Analog IC 300, the operating mode can be specified for each configurable amplifier channel. Current consumption can be reduced by changing the operating mode from high-speed to low-speed, but this affects some of the electrical characteristics; for example, the gain band width is reduced and the slew rate is degraded. For details, see *RAA730300, Monolithic Programmable Analog IC Datasheet.*

Table 2.4 shows the current consumption and slew rate when configurable amplifier channels Ch1 to Ch3 are used as non-inverting amplifiers.

Table 2.4 Operating mode characteristics (excerpted from the datasheet)

Conditions	Current consumption				Slew rate	
	MIN	TYP	MAX	Unit	TYP	Unit
High-speed mode	–	330	500	μA	1.1	V/μs
Mid-speed mode 2	–	250	380	μA	0.8	V/μs
Mid-speed mode 1	–	170	260	μA	0.5	V/μs
Low-speed mode	–	90	150	μA	0.25	V/μs

Figure 2-11 shows the actually measured waveforms. This figure shows the variation in the slew rate measured by changing the operating mode for configurable amplifier Ch1 by using the TSA-IC300, a pulse generator, and an oscilloscope. Figure 2-10 shows the measurement scheme, and Table 2.5 shows the settings used for the measurement.

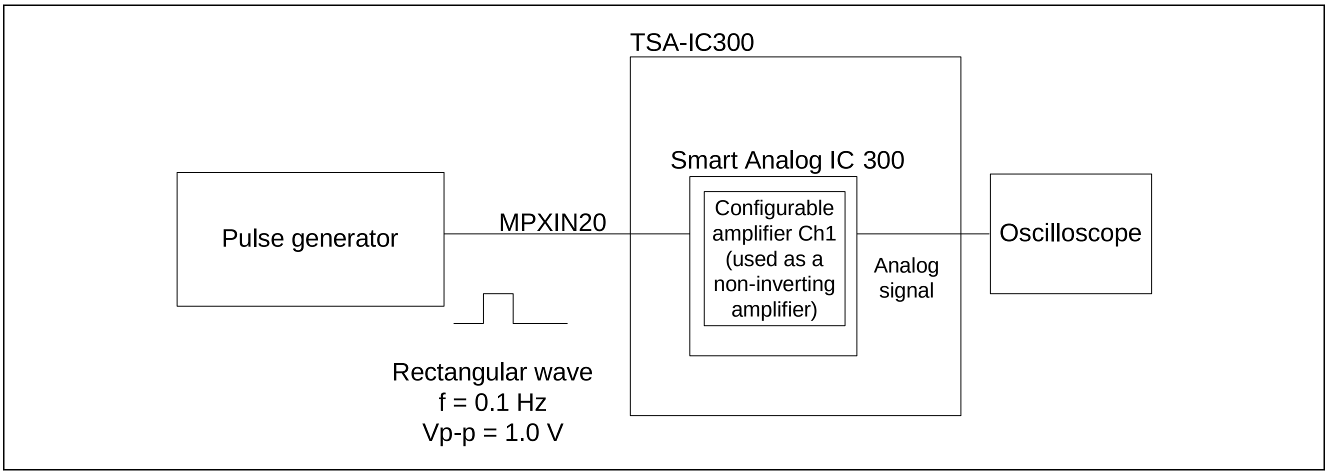
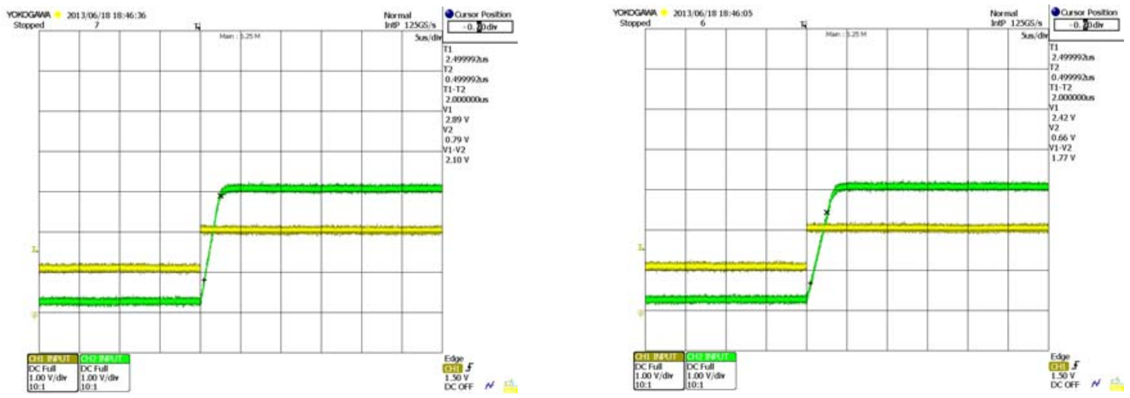


Figure 2-10 Slew rate measurement system diagram

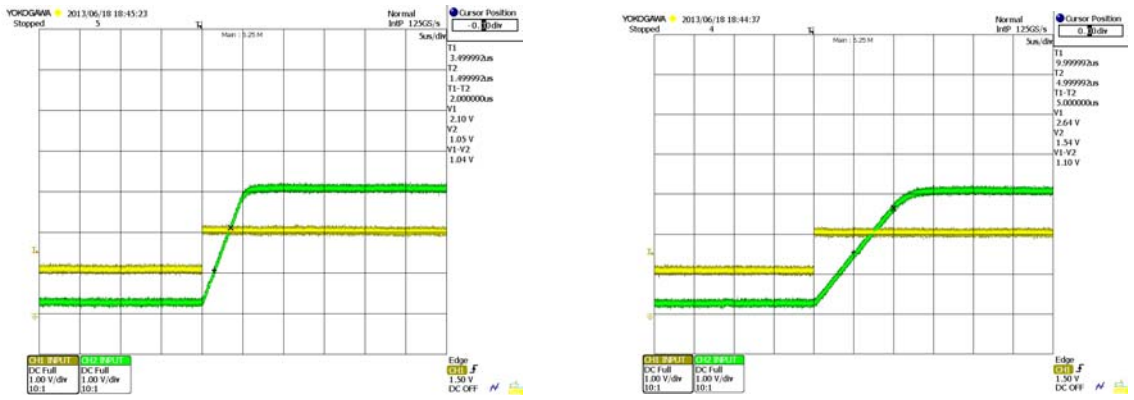
Table 2.5 Settings for measurement in operating mode

Settings specified in:	Description	Set value	
Pulse generator settings	Generating a sine wave signal	Signal	Rectangular wave
		Cycle	0.1 Hz
		DC offset	1.0 V
		Amplitude	1.0Vp-p
Easy Starter	Settings specified in Smart Analog IC 300	Amplifier used	Configurable amplifier Ch1
		Amplifier configuration	Non-inverting amplifier
		Signal input pin	MPXIN20
		Gain	9.5 dB
		D/A converter used	D/A converter Ch5
		D/A converter output voltage	116 (1.50 V)



(a) High-speed mode

(b) Mid-speed mode 2



(c) Mid-speed mode 1

(d) Low-speed mode

Figure 2-11 Slew rate measurement result

Table 2.6 shows the measured current consumption and slew rate values.

Table 2.6 Result of measurement in each operating mode

Operating modes	Current consumption		Slew rate	
	Measured value	Unit	Measured value	Unit
High-speed mode	260.0	μA	1.05	V/μs
Mid-speed mode 2	209.9	μA	0.89	V/μs
Mid-speed mode 1	134.8	μA	0.52	V/μs
Low-speed mode	71.2	μA	0.22	V/μs

Note The above values are obtained a result of measurement based on limited samples. Use these values for reference only.

As shown in Table 2.6, by lowering the operating speed, the current consumption can be reduced but the slew rate is degraded. In your actual system, thoroughly evaluate the performance and determine the settings according to the system specifications.

3. Functional Differences in Smart Analog IC 301

3.1 Differences from Smart Analog IC 501

Table 3.1 shows the differences between Smart Analog IC 301 and Smart Analog IC 501. For details, see *RAA730301, Monolithic Programmable Analog IC Datasheet* and *RAA730501, Monolithic Programmable Analog IC Datasheet.*

Table 3.1 Differences between Smart Analog IC 301 and Smart Analog IC 501

Description	Smart Analog IC 301	Smart Analog IC 501	Remark
Instrumentation amplifier input mode setting	Can be selected • Rail-to-rail input • P-ch single-ended input	Cannot be selected	See *3.2* for details.
Instrumentation amplifier gain setting	6 to 34 dB	20 to 60 dB	
Switches for offset voltage measurement	Available	Not available	See *3.3* for details.
Range of voltage output by variable output voltage regulator	1.8 V to 3.1 V (Typ.)	2.0 V to 3.3 V (Typ.)	
Output voltage temperature coefficient for temperature sensor	–4 mV/°C (Typ.)	–5 mV/°C (Typ.)	
Operating voltage range	$2.2\ V \leq V_{DD} \leq 3.6\ V$	$3.0\ V \leq V_{DD} \leq 5.5\ V$	

3.2 Input modes

In Smart Analog IC 301, an input mode bit (AIMS) is provided for the instrumentation amplifier. By using this bit, the input mode can be selected from rail-to-rail input and P-ch single-ended input. Table 3.2 shows the electrical characteristics for each input mode. For details see *RAA730301, Monolithic Programmable Analog IC Datasheet*.

Table 3.2 Input mode characteristics (excerpted from the datasheet)

Input voltage	Rail-to-rail input		P-ch single-ended input		Unit
	MIN	MAX	MIN	MAX	
Instrumentation amplifier	AGND1 – 0.05	AV_{DD1} + 0.1	AGND1 – 0.05	AV_{DD1} – 1.4	V

Figure 3-2 shows the actually measured waveforms. This figure shows the variation in the waveforms measured by applying a sine wave signal from a pulse generator and then using Smart Analog Easy Starter to change the input mode of the instrumentation amplifier. Figure 3-1 shows the measurement scheme, and Table 3.3 shows the settings used for the measurement.

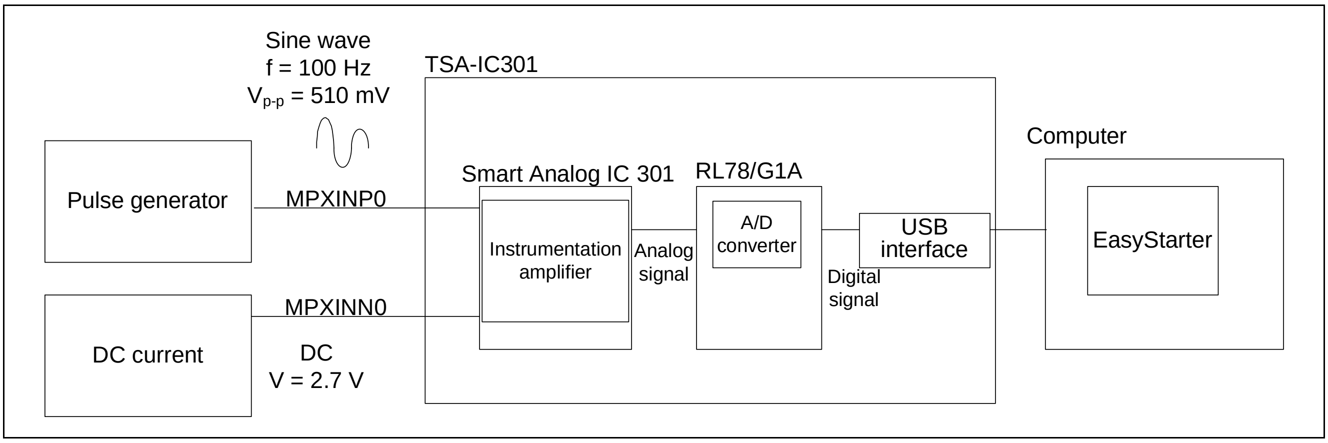
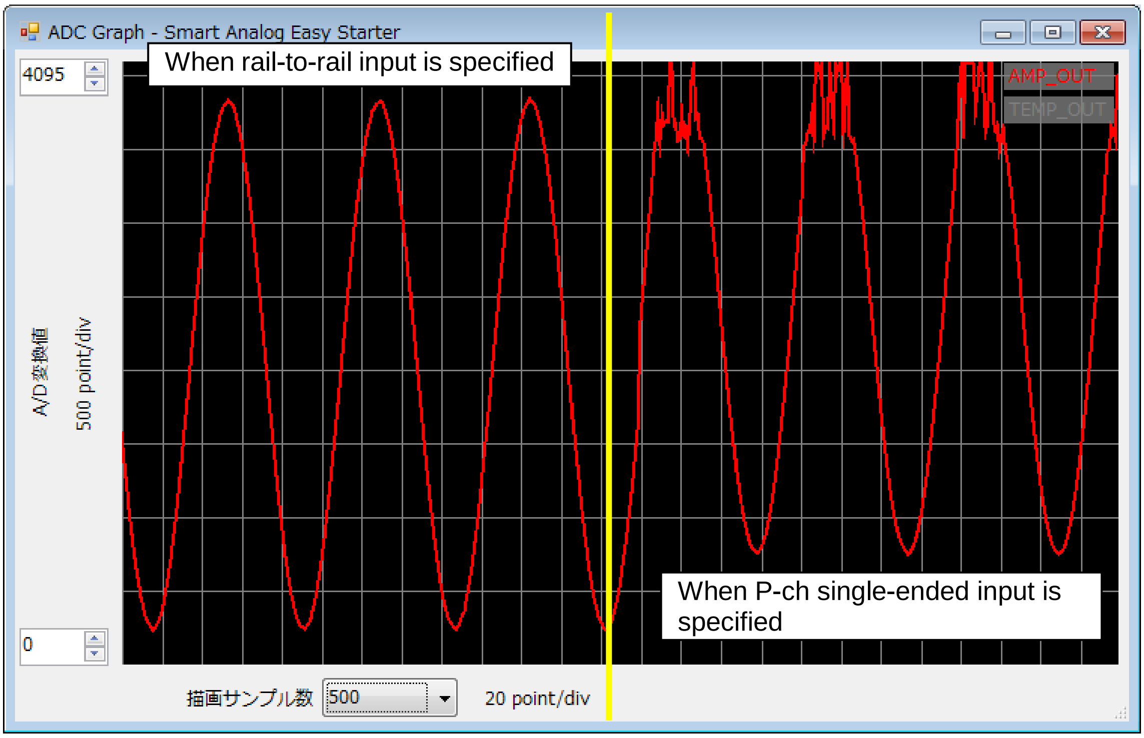


Figure 3-1 Measurement system diagram

Table 3.3 Settings for measurement in input mode

Settings specified in:	Description	Set value	
Pulse generator settings	Generating a sine wave signal	Signal	Sine wave
		Cycle	100 Hz
		DC offset	2.65 V
		Amplitude	510mVp-p
	Inputting a signal from the MPXINN0 pin in Smart Analog IC 301	Signal	DC
		Voltage	2.7 V
Easy Starter	Settings specified in Smart Analog IC 301	Instrumentation amplifier gain	16 dB
		D/A converter output voltage	162 (2.10 V)
		A/D conversion cycle	10 ms

If the input voltage exceeds the upper limit in P-ch single-ended input mode, the voltage output from the instrumentation amplifier is distorted. This means that the upper limit of the input range in P-ch single-ended input mode becomes narrower than that in rail-to-rail input mode.



When rail-to-rail input is specified

When P-ch single-ended input is specified

Figure 3-2 Waveforms of amplifier output voltage before and after input mode change

3.3 Switches for offset voltage measurement

Switches used for measuring the offset voltage, SW0 and SW1, are provided for Smart Analog IC 301. When both SW0 and SW1 are set to ON, the voltage at the non-inverted input pins and the inverted input pins becomes equal, thereby making it possible to measure the offset voltage that is generated in the amplifier.

The following shows how to calculate the offset voltage and the settings to be specified for Smart Analog IC 301 to measure the offset voltage.

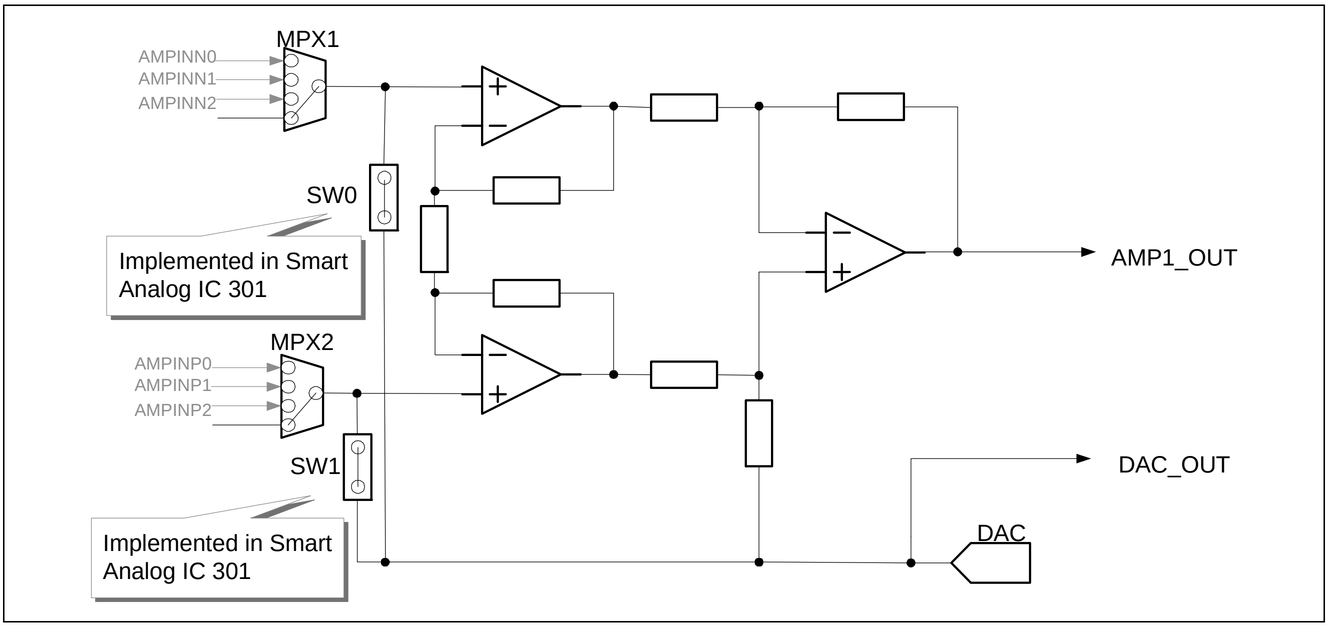


Figure 3-3 Offset voltage measurement

The desired instrumentation amplifier output voltage V_{AMP_OUT} can be expressed by using Formula 3-1, with the voltage at a non-inverted input pin defined as V_{MPXINP}, the voltage at an inverted input pin defined as V_{MPXINN}, the gain is defined as G, and the bias voltage defined as V_{DAC}.

$$V_{AMP\_OUT} = (V_{MPXINP} - V_{MPXINN}) \cdot G + V_{DAC}$$ Formula 3-1

If the instrumentation amplifier includes an offset difference, Formula 3-1 becomes Formula 3-2, with the input conversion offset voltage defined as V_{Offset}.

$$V_{AMP\_OUT} = (V_{MPXINP} - V_{MPXINN} + V_{Offset}) \cdot G + V_{DAC}$$ Formula 3-2

At this point, by setting both SW0 and SW1 to ON, V_{DAC} is supplied to the non-inverted input pin and the inverted input pin. Consequently, Formula 3-2 becomes Formula 3-3.

$$V_{AMP\_OUT} = V_{Offset} \cdot G + V_{DAC}$$ Formula 3-3

From Formula 3-3, if a voltage with the same potential is input to the non-inverted input pin and the inverted input pin, the offset voltage in the amplifier output can be calculated from the difference between V_{AMP_OUT} and V_{DAC}. The input conversion offset voltage is the offset voltage further divided by gain G.

For example, if V_{DAC} is set to 1.50 V, G to 34 dB, SW0 to ON, and SW1 to ON, the output voltage of the instrumentation amplifier when there is no offset voltage ($V_{Offset} = 0$), V_{AMP_OUT}, is 1.50 V, and the potential difference with V_{DAC} is 0 V.

However, if, with the above settings, a voltage of 1.60 V is measured at the V_{AMP_OUT} pin, we can calculate that the offset voltage in the amplifier output is 0.1 V from the 0.1 V difference between V_{AMP_OUT} and the D/A converter's output voltage V_{DAC}. Converting this to an input voltage, the offset voltage becomes approximately 2.0 mV.

To minimize the effect of the output offset voltage, it is necessary to adjust the bias voltage. As shown in Formula 3-3, because the D/A converter's output voltage is not multiplied by a gain value, there is no effect from gain. To ensure that the voltage actually output from the instrumentation amplifier is the same as the D/A converter voltage, V_{DAC}, before being adjusted, the D/A converter's output voltage can be adjusted ($V_{DAC} - \Delta V_{DAC}$) to cancel out the offset voltage generated by the amplifier (Formula 3-4).

$$V_{AMP\_OUT} = \left(V_{MPXINP} - V_{MPXINN} + V_{Offset}\right) \cdot G + V_{DAC} - \Delta V_{DAC} \qquad \text{Formula 3-4}$$

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep 30, 2013	—	First edition issued.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-ons
   The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to a product with a different type number, confirm that the change will not lead to problems.
   - The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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