DESIGNING WITH FIFOs

TECHNICAL NOTE TN-06

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FIFOs are First-In/First-Out buffers that act as elastic buffers between two synchronous or asynchronous systems. The IDT7201 (512 x 9), IDT7202 (1K x 9), IDT7203 (2K x 9) and IDT7204 (4K x 9) are high-speed FIFOs that can operate at frequencies greater than 20 MHz. Here are a few tips on designing with these FIFOs.

A generic block diagram of the FIFOs is shown in Figure 1. After power up, the FIFO must be reset. The reset operation requires that the read and write lines be HIGH for a time t_{RPW} or t_{WPW} (the read or write pulse width minimums) before the rising edge of $\overline{RS}$, and to be HIGH for a time t_{RSR} after the rising edge of $\overline{RS}$. These operating conditions are shown in Figure 2. It is important to observe the stipulated requirements on Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) during reset because they increment the read and write pointers and both edges of $\overline{R}$ and $\overline{W}$ also affect the empty and full counters. The Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$) counters have to be appropriately set after a reset operation.

The read and write pointers are high-speed counters that are incremented on every rising edge of read and write lines. These lines must be noise-free as in other high-speed counters like F161s and AS161s. This poses a common interface issue that users often encounter. False clocks can be caused by transmission line effects or crosstalk. Some of the symptoms of false clocking are flags asserted when they should not be, missing data or scrambled data order.

The Read or Write signals may be generated by a part that is physically placed far away from the FIFO on a PC board. This implies a propagation delay to and from the driver to the receiver that is greater than the rise and fall time of the driver. This causes reflections on the line. Also the driver that has a LOW impedance on the HIGH-to-LOW transition causes an impedance mismatch. The mismatch is apparent with an F-type device or a Schottky-TTL device as their HIGH-to-LOW impedance is fairly small (typically under 15 Ohms for F-type or FCT and under 10 Ohms for Schottky-TTL).

This translates to a signal that eventually settles near zero volts but, in the interim, has a "damping" effect; it may go through a –2.0 volt to +1.5 volt to –1.0 volt to +.7 volt to zero volts. This is shown in Figure 3. The FIFO devices can handle a negative voltage level of 1.5V for less than 10ns. If a positive 1.1 voltage level persists for a pulse width greater than 5ns, the corresponding read or write pointer may increment. Data is either written or read twice, or garbage is written to or read from one or more locations. This can cause the FIFO to be "out of sync" where the read or write (or both pointers) are at wrong locations. This problem is solved by keeping the parts creating the $\overline{R}$ and $\overline{W}$ signal as close to the FIFO as possible. If FAST™ or Schottky devices are used, and if ringing occurs, add a series resistor of 20 to 50 Ohms so the impedance of the driver in the HIGH-to-LOW transition, plus the series resistor, approximately equal the line impedance.

$\overline{R}$ and $\overline{W}$ should be HIGH if read and write operations are not occurring. Crosstalk causes noise on the read and write lines that may be 1.1 volts or greater for more than 5ns. However, if $\overline{R}$ and $\overline{W}$ are HIGH and noise appears on the line, the FIFO is more noise immune (as V_{OH} is higher on the driver when a CMOS device is being driven and the V_{CC} noise margin is greater than the ground noise margin). During a long clock LOW time of 150ns, for a clock cycle of 200ns, a spurious read or write can occur due to noise. If the system can handle it, a better recommended timing is a clock LOW time of 50ns and a clock HIGH time of 150ns, giving better noise immunity.

Unused data inputs should be tied to ground or V_{CC}. In the stand-alone mode or width expansion mode, $\overline{XI}$ must be grounded and $\overline{FL}/\overline{RT}$ should be tied HIGH, given the retransmit feature is unused. Good board design techniques must be practiced and a ground plane or power distribution element are highly recommended. Decoupling capacitors of 0.1µf disk capacitors should be used to decouple V_{CC} and ground.

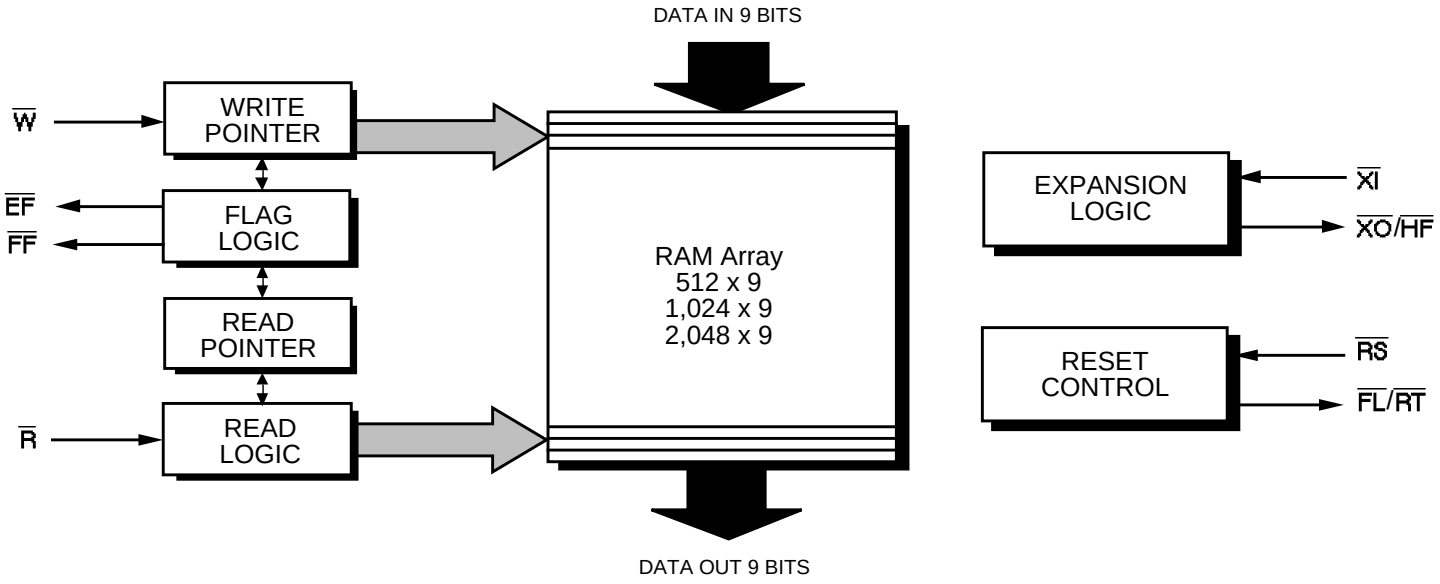

Figure 1. FIFO Block Diagram

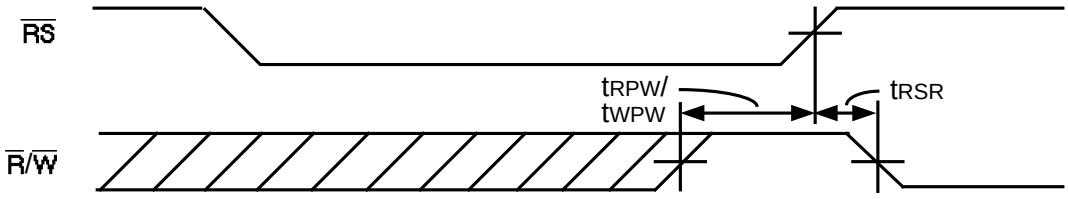

Figure 2. Reset Requirements

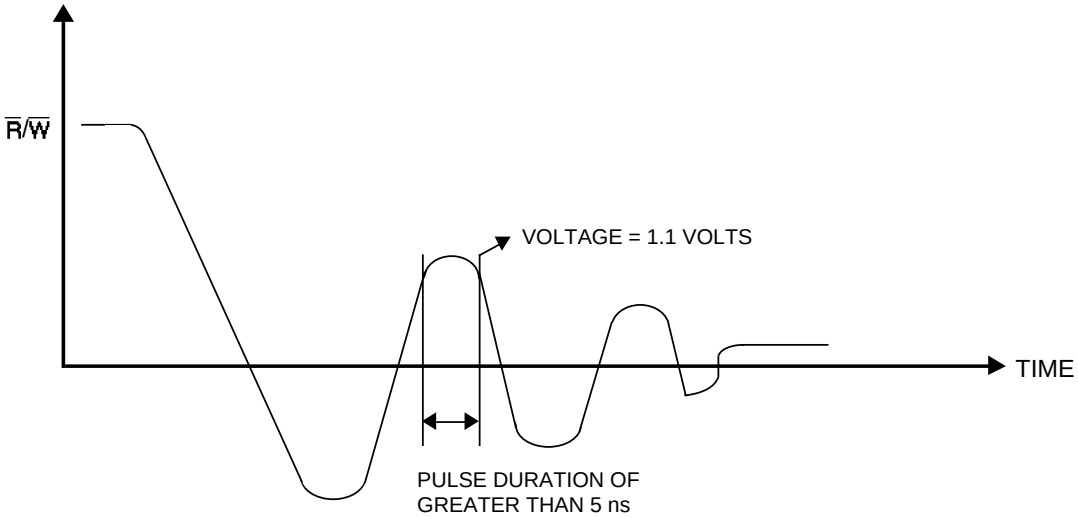

Figure 3. Reflections and Undershoot on the Read and Write lines that cause false increments on the Read and Write pointers

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