Cascading FIFOs or FIFO Modules

TECHNICAL NOTE TN-09

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The IDT7200/7201/7202/7203/7204/7205/7206/7207/7208 are high-speed 512 x 9, 1,024 x 9, 2,048 x 9, 4,096 x 9, 8,192 x 9, 16,384 x 9, 32,768 x 9 and 65,536 x 9 FIFOs, respectively, that can be cascaded to form even deeper FIFOs. This tech note explains how these FIFOs are cascaded.

A cascaded FIFO configuration of 512 x 9 FIFOs is shown in Figure 1. The $\overline{FL}$ pin (First Load) of the first FIFO to be loaded after a reset is tied to ground. The other FIFOs have their $\overline{FL}$ pin tied to VCC. After a reset operation, the first 512 writes occur in the first FIFO. During these write operations, the $\overline{XO}$ (Expansion Out) and $\overline{XI}$ (Expansion In) lines are high. On the 512th write, a pulse is created on the $\overline{XO}$ line following the Write ($\overline{W}$) line. The pulse informs the second FIFO that is going to receive the next word. It also informs the first FIFO that its write pointer will no longer increment due to an internal evaluation of the $\overline{XO}$ line. The $\overline{XO}$ line of the first FIFO is connected to the $\overline{XI}$ line of the second FIFO. The $\overline{XO}$ of the second FIFO is connected to the $\overline{XI}$ of the third, and so on. The $\overline{XO}$ of the last FIFO is connected to the $\overline{XI}$ of the first FIFO. A typical $\overline{XO}$ operation of 2,048 writes after a reset is shown in Figure 2.

The same procedure holds true for read operations. During the 512th read operation after a reset, another pulse will be created on the $\overline{XO}$ line following the Read ($\overline{R}$) line. This pulse will inform the second FIFO that it will be read from on the next cycle (provided it is n't empty). Also the first FIFO's read pointer will not increment until it receives a second pulse on its $\overline{XI}$ line.

Figure 3 shows the $\overline{XO}$ and $\overline{XI}$ relationship to read and write. The $\overline{XO}$ pulses are transferred to the $\overline{XI}$ of the next level of FIFO. The first pulse transfers write pointer control and the second transfers read pointer control. There is an important advantage to this method expansion. A word written to the FIFO after a master reset is immediately available at the FIFO output. A read cycle can be initiated as soon as the Empty Flag ($\overline{EF}$) is unasserted. This is called zero fall-through time. Earlier shift register-based FIFOs have a fall-through time in the µsec range.

To take full advantage of this unique expansion feature, some design precautions must be observed. Since a pulse on $\overline{XI}$ activates read or write operations of the FIFO, they must be relatively free from cross-talk noise. A long trace from the $\overline{XO}$ of the last FIFO to the $\overline{XI}$ of the first FIFO is a potential source of cross-talk noise. To prevent noise spikes from altering the $\overline{XI}$ input on this and other $\overline{XO}$ to $\overline{XI}$ interconnects, a small capacitor in the 22pF to 47pF range should be inserted between the $\overline{XI}$ inputs and ground.

Another important point is how to handle flags in the expansion mode. To create the composite Full Flag, tie the four individual FIFO Full Flags ($\overline{FF}$) to an OR gate. The composite $\overline{EF}$ is created similarly. This additional logic is shown in Figure 1.

To create intermediate flags using the individual Full and Empty Flags is more tricky, but can be done. For example, an attempt to create a composite Half-Full Flag ($\overline{HF}$) is described here. Let us define Flag f1 as when any two FIFOs are full and at last one other FIFO is not empty. Boolean Equation for f1:

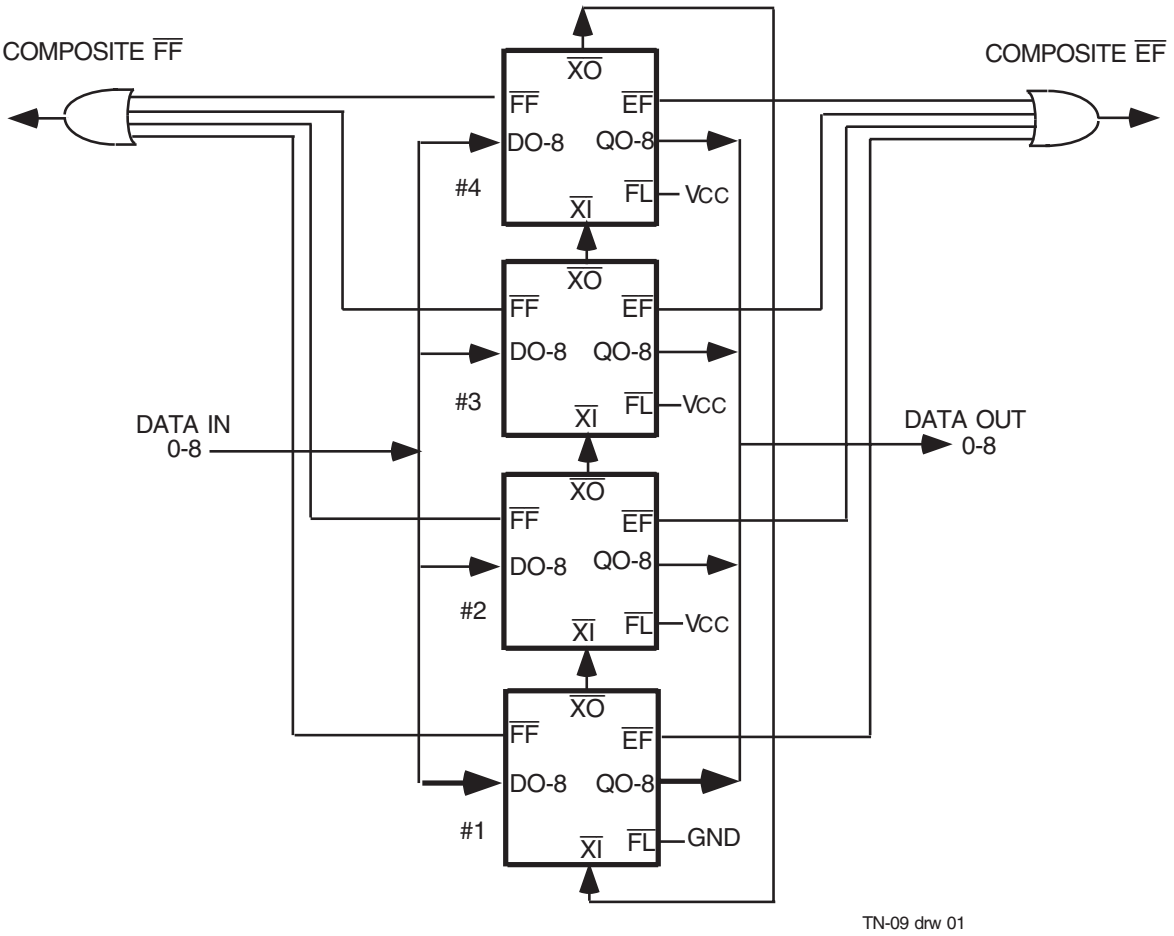
f1 = FF1.FF2($\overline{EF3}$ + $\overline{EF4}$) +
FF2.FF3($\overline{EF1}$ + $\overline{EF4}$) +
FF3.FF4($\overline{EF1}$ + $\overline{EF2}$)
FF4.FF1($\overline{EF2}$ + $\overline{EF3}$)

FFi = Full Flag of FIFOi

EFi = Empty Flag of FIFOi

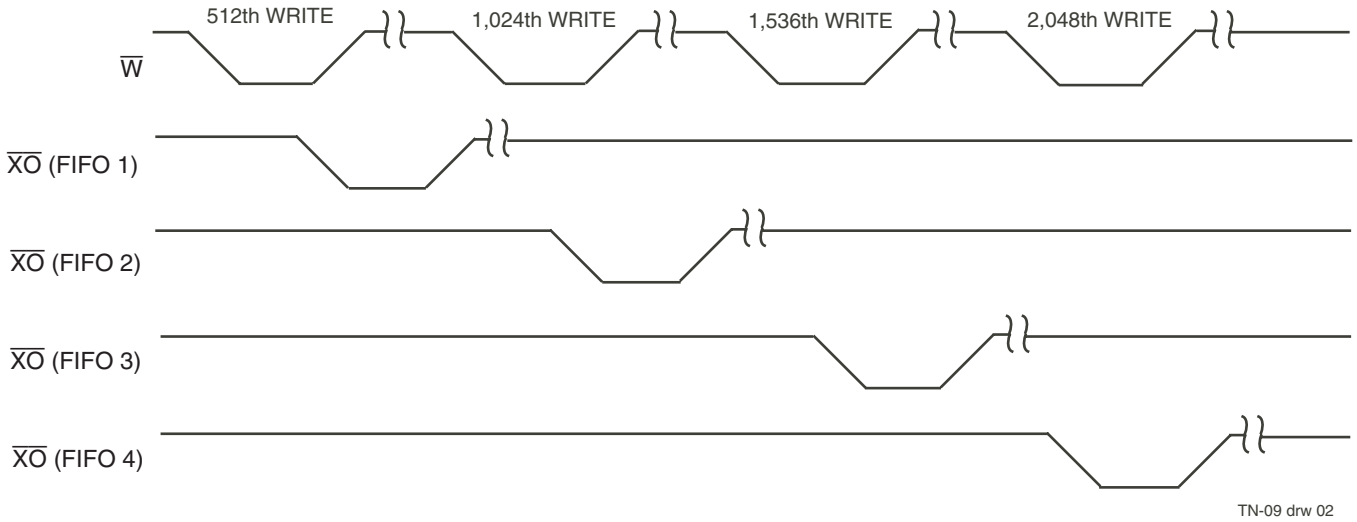
In one extreme case, f1 is asserted when there is 1,500-1 words in the FIFO array. The first two FIFOs are full, with 512 words in each, and the third FIFO has 511 words. Another extreme case is when two FIFOs are full and the third FIFO has only one word. Therefore, Flag f1 is only a range of words where the half-full condition exists, from 1,024+1 to 1,500-1 words in the array. It may not be used as a half-full indicator, because the FIFO array may be almost 3/4 full before Flag f1 is asserted.

As shown in Figure 4, an empty FIFO array has a word written to it and then read from it. Then, 1,500-1 words are written to the FIFO array. The write pointer is on the last word of the third FIFO. Only at this time is Flag f1 asserted, while the FIFO array has 1,500-1 words in it. Intermediate flags like f1, generated from Boolean Equations, can only provide a range of values when f1 is to be asserted. A precise position for f1 cannot be determined. If Boolean Equations are used to generate intermediate flags, consider all the different locations of the read and write pointers which may assert or deassert at a particular condition.



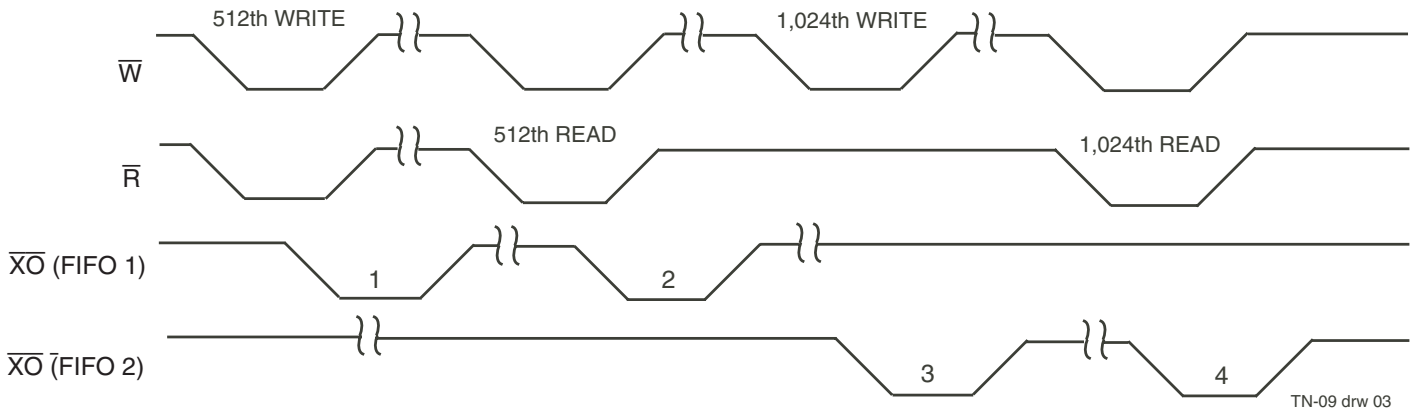
NOTE:
Read, Write and Reset controls go to all four FIFOs.

Figure 1. Four Cascaded 512 x 9 FIFOs



NOTE:
Read line is assumed to be HIGH in this example

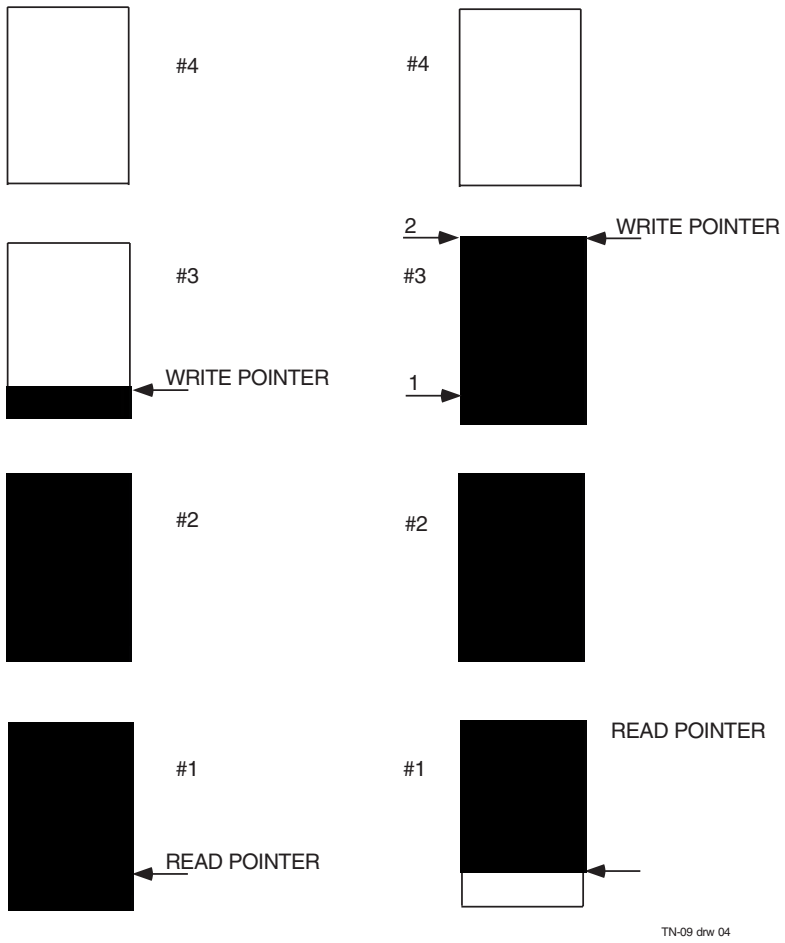
Figure 2. The XO/XI Timing Pulse for 2,048 Writes and Zero Reads



NOTES:

1. Pulse 1 is created by the 512th write pulse; it is a delayed write pulse.
2. Pulse 2 is created by the 512th read pulse.
3. Pulse 3 from FIFO 2 is created by the 1,024th write pulse.
4. Pulse 4 is created by the 1,024th read pulse.
5. $\overline{XO}$ (FIFO 3) and $\overline{XO}$ (FIFO 4) are not shown, but they follow the same pattern.
6. $\overline{XO}$ (FIFO 4) will be created by the 2,048th write pulse and later by the 2,048th read pulse, thereby transferring pointer control back to FIFO 1.

Figure 3. The $\overline{XO}$ and $\overline{XI}$ PulseTimings



Case 1: In the cascaded FIFO arrangement, the write pointer has just written to FIFO #3 and the flag defined by the f1 equation would be asserted at the half-full point.

Case 2: The FIFO array is half-full at arrow at Note 1, but f1 will not be asserted until the last write into FIFO #3 or until the FIFO array is almost 3/4 full or at arrow 2.

Figure 4. The Behavior of the f1 Flag for Different Cases