Transient SEE Test Method for Precision SAR ADCs

This application note discusses the test algorithm to characterize SEE (Single Event Effects) in low-speed precision Successive Approximation Register (SAR) ADCs specifically identifying SET (Single Event Transients) and SEFI (Single Event Functional Interrupts) to characterize the device for space applications. This test algorithm places the ADC into a set of real-world operating conditions to test the device in a manner in line with its actual usage. This algorithm applies to low-speed precision SAR ADCs that do not contain user programmable configuration registers. Such registers would require a separate algorithm for SEE detection.

To apply this algorithm, the test method requires that the ADC operates with an analog input in the middle of its input voltage range that equates to its reference voltage divided in half. This allows for the detection of transient events in both the positive and negative going directions. This contrasts with operating the ADC at an input level at or near the end points of its analog input range. In an ADC with bipolar (signed) data format, the operating point would be a zero-scale level (such as binary code near all 0s) rather than the positive or negative full-scale levels. In an ADC with unipolar (unsigned) data format, this would be at the mid-scale level (such as near the maximum binary code divided by two). Operating the device in the middle of its input voltage range is in line with normal operation of the part in a real-world application because most applications require maximum input signal range.

Observation of the ADC digital output codes can be performed by a logic analyzer or an FPGA (Field Programmable Gate Array). The algorithm detects any event where the digital output code(s) is/are beyond a specified threshold. Depending on the length of such an event, it can be determined if these events are SET or SEFI. The threshold used for event detection is device specific and is dependent on several factors. Some of these factors include resolution, inherent noise, and performance of the ADC as well as environmental noise factors. A calibration run must be performed at the SEE testing facility before exposing the device to heavy ions to determine the expected code and the appropriate detection threshold range.

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1. SEE Testing Facility

SEE testing should be performed at a facility such as the Texas A&M University (TAMU) Radiation Effects Facility of the Cyclotron Institute. This facility is coupled to a K500 super-conducting cyclotron, which can generate a wide range of particle beams with the various energy, flux, and fluence levels needed for advanced radiation testing. A facility such as this is necessary to provide various particle beams with different energy levels to allow for characterization of the ADC to enable the generation of Weibull fit curves, which may be subsequently input into CRÈME96 to statistically predict behavior in space applications. The Devices Under Test (DUT) should be delidded and located in air at 30mm to 50mm from the Aramica window for the ion beam. If the ADC is in a flip chip type package, the device should be delidded, and a backside grind performed to the appropriate thickness to allow for ion penetration into the active area of the die.

At a minimum, SEE testing should be performed using at least four heavy ions Au such as (gold), Ag (silver), Cu (copper), and Ar (argon) for LET values of 86, 43, 20, and 8.5MeV•cm^2/mg, respectively. Performing the testing using four heavy ions provides enough data points to generate a suitable Weibull fit curve. In some cases, it can be beneficial to test using lower energy ions such as Ne (neon), Nitrogen (N), and/or He (helium) for LET values of 2.7, 1.3, and 0.11MeV•cm^2/mg, respectively. Testing at these lower energy levels can provide further insight into the onset of SEE if there are a reasonably high number of SEE observed using the heavy ions Ar (argon) at 8.5 or Ne (neon) at 2.7MeV•cm^2/mg. At an LET value where no SEE is observed, there is no need to test at any lower LET values. The heavy ion LET values are quoted at the DUT surface.

2. Transient SEE Testing

This algorithm can be applied in multiple implementations. In this application note, the primary focus is on implementing the algorithm in a logic analyzer, but a brief discussion is included on its implementation in an FPGA. The output data from the ADC is input to a logic analyzer in parallel format. It is most efficient to handle the sample data in parallel format therefore observing the whole sample word each sample period.

Because most low-speed precision SAR ADCs use a SPI (Serial Peripheral Interface) bus for data output each data bit must be collected and assembled to form the sample word. A sample word could be anywhere from 14 to 20 bits or more; therefore, the device should be capable of handling the total number of bits. If the precision SAR ADC uses an SPI output, an on-board Complex Programmable Logic Device (CPLD) or similar programmable logic device can provide the conversion start signal and serial data clock to the ADC as well as perform the serial to parallel conversion of the data.

Most logic analyzers offer at least one or two parallel port input buses and some offer up to four. Logic analyzers with a higher number of input buses is required to support higher resolution ADCs. In this application note, the focus is on the test algorithm for a 14-bit precision SAR ADC. The logic analyzer referenced in this document is the Keysight 16861A Logic Analyzer. It offers two 16-bit parallel bus inputs each with a clock input. To enable SET detection with the fastest speed, data must be input to the logic analyzer as parallel data. In the implementation of this algorithm with the ISL73141SEH and ISL73148SEH, a CPLD collocated on the PCB with the ADC converts the serial data to parallel data for observation by the logic analyzer. The parallel digital output data from the CPLD is routed to the Keysight logic analyzer for SET detection.

The logic analyzer should be set up to detect ADC code deviations outside a specified window on a per sample basis. This allows for SET events to be detected even if only lasting for one ADC sample. This window is specific to a given ADC based on its resolution and performance. This SET detection algorithm detects single sample transients as well as records multiple sample transients if they are present because every sample is observed and, when an SET is detected, the sample is stored. Figure 1 shows the full output code range for an ADC with an example plot of output codes in green and an example SET threshold in blue. Example transient events are highlighted.

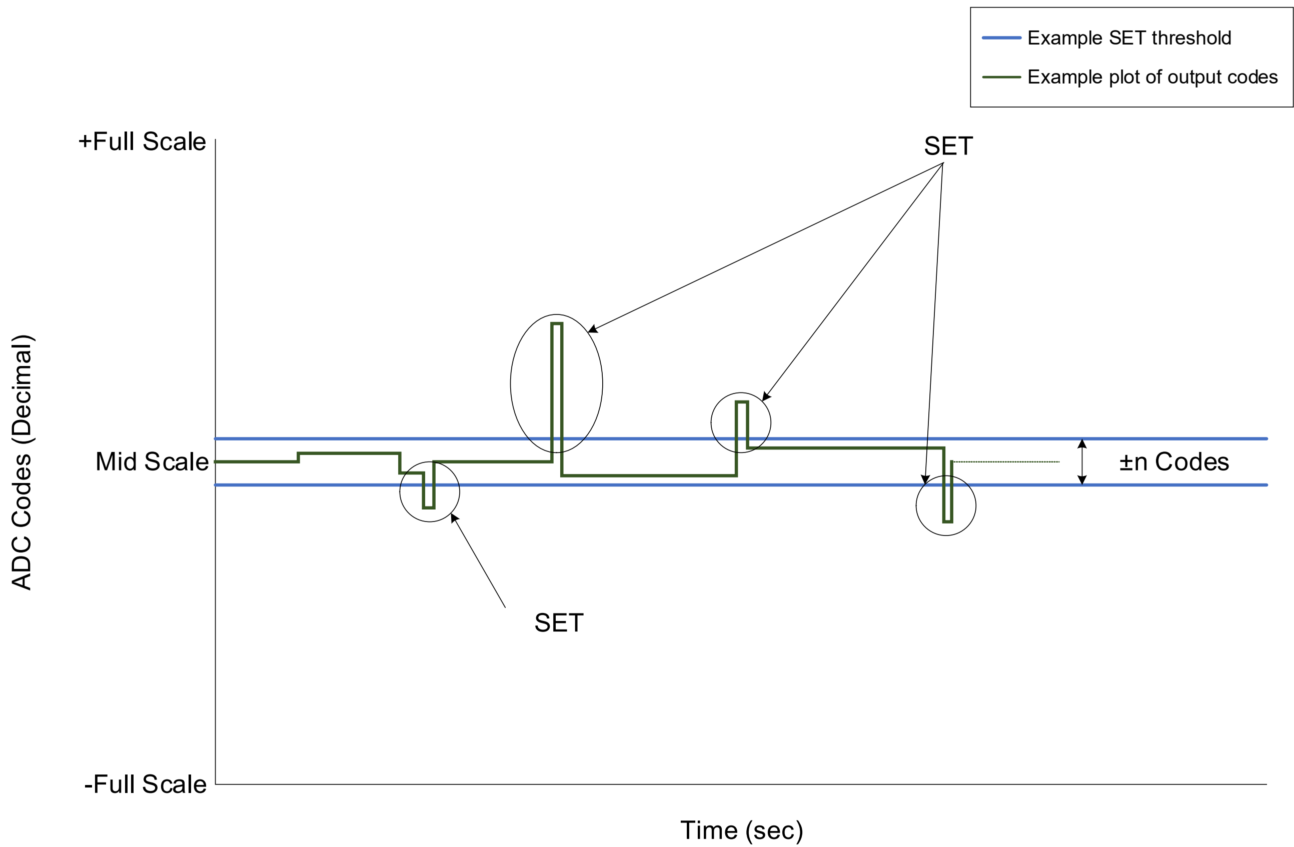

Figure 1. Expected ADC Output Code Range, SET Detection Threshold, and SET Events

The logic analyzer software can be set to automatically record the time if an SET event is detected. Additional separate software is required to perform post-processing of the data to determine the number and magnitude of single and multiple sample events. This processed data is then used to generate Weibull fit curves.

Before any SET run, each device should be observed in a radiation free environment to find the appropriate SET threshold. The threshold should be set such that it is just above the inherent noise level of the ADC and excludes any noise from the test environment. For the ISL73141SEH, this level was found to be ±8 codes centered at the average mid-scale code. To find the average mid-scale code a calibration run should be completed for each ADC before each SET run. In the case of a 14-bit ADC, the expected mid-scale output code in decimal should be approximately 8192 for unsigned (unipolar) data and 0 for signed (bipolar) data. Setting the ADC input to achieve this output code allows for transient excursions to be observed in either a positive or negative going direction. Achieving all these conditions effectively ensures that detected excursions beyond the threshold are because of heavy ion strikes.

The average mid-scale code is input in the logic analyzer to set the SET threshold to the appropriate number of codes around this value. To set up the logic analyzer appropriately, the advanced trigger feature of the Keysight 168161 Logic Analyzer is used and can be accessed as shown in Figure 2.

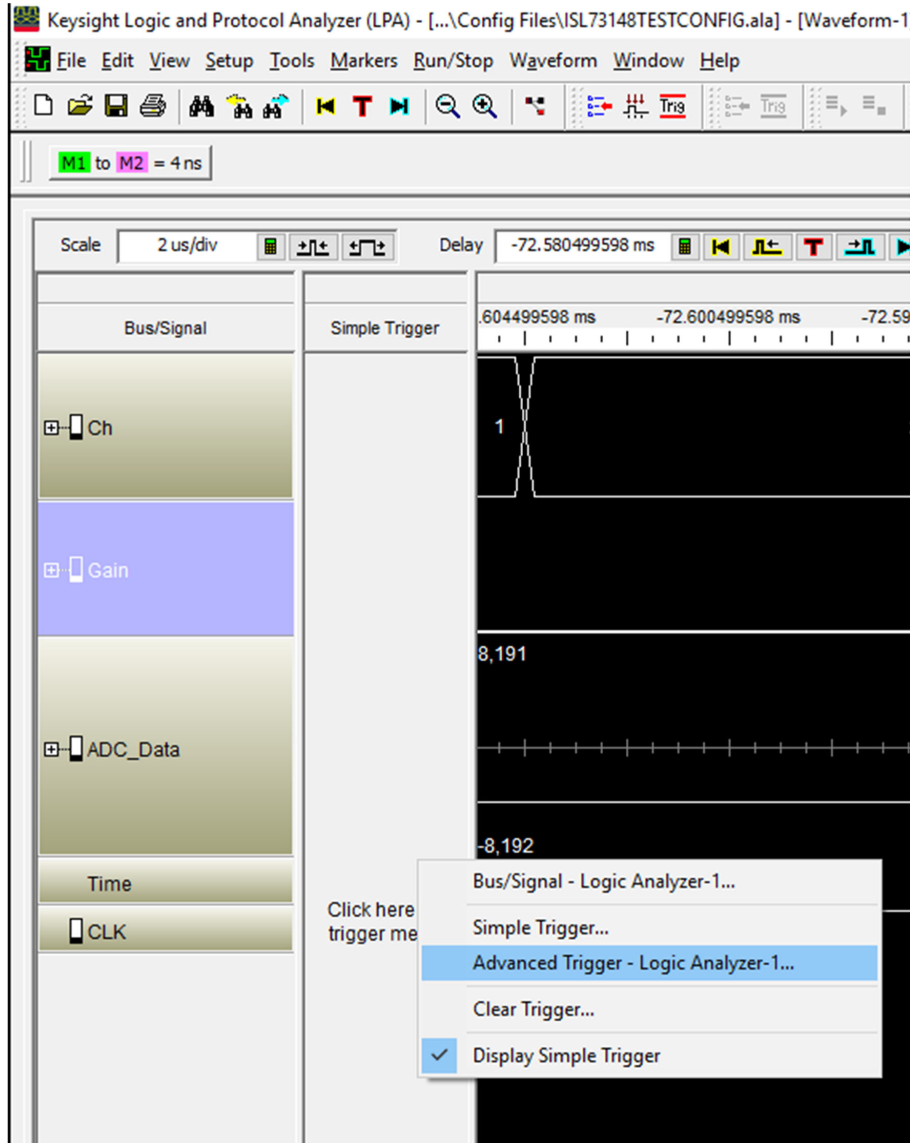

Figure 2. Access to the Advanced Trigger Menu on the Keysight 16861A

The advanced trigger allows the logic analyzer to trigger on specific events and has limited logic evaluation of such events. *IMPORTANT:* Each step number in the advanced trigger operation corresponds to one input clock cycle. When the Advanced Trigger menu is open, the functions available in the logic analyzer can be used to configure the algorithm to detect the digital output code excursions beyond the defined threshold.

Figure 3 shows how the Advanced Trigger menu is set up in the logic analyzer to detect any sampled digital code that violates a threshold of 8192 ±8 codes. This is defined by the statements in the section under Default Storage. This sets up the overall algorithm the conditions for when the logic analyzer capture stores a given sample. When a sample is within this specified range, the logic analyzer does not store the sample. The logic analyzer is set up to use a counter function that is programmed to the required maximum number of SET for the test run.

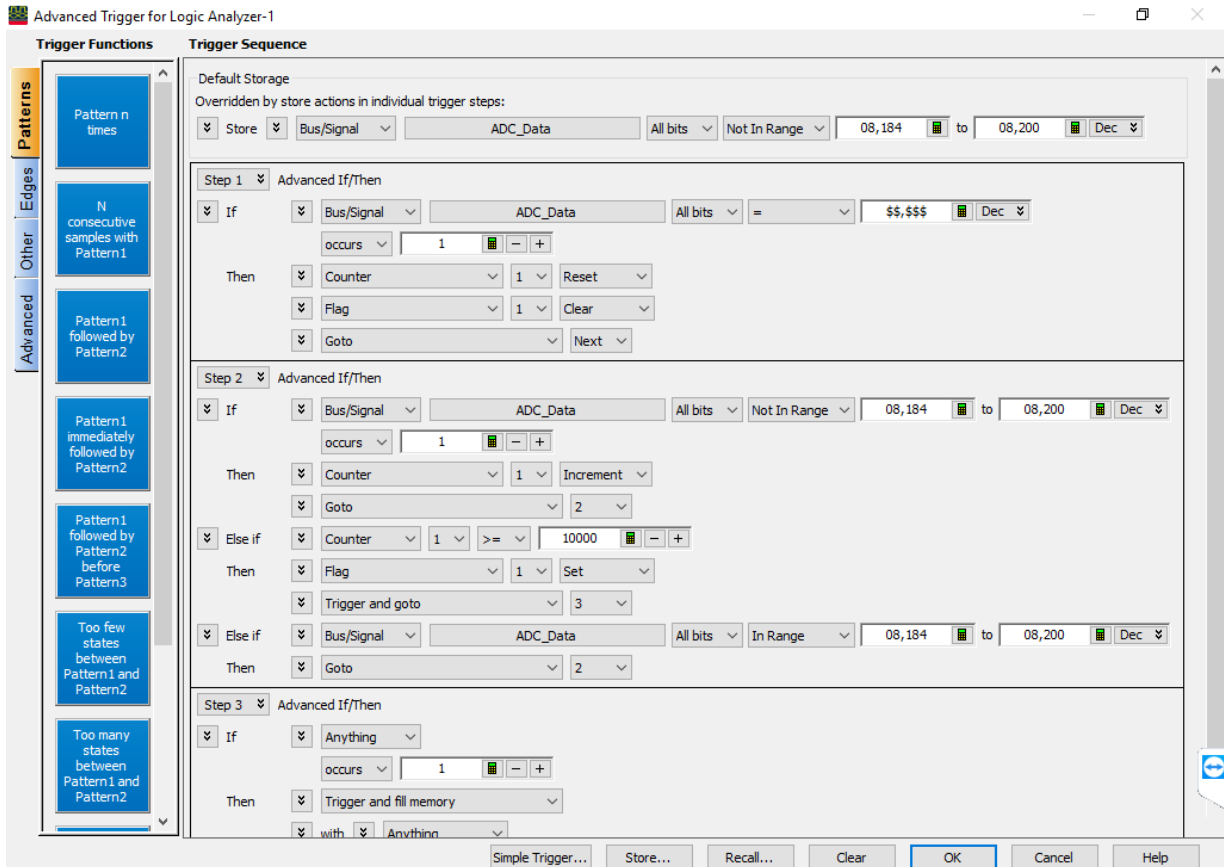

Figure 3. Advanced Trigger Menu Algorithm Setup on the Keysight 16861A

In this example, the maximum number for the counter is set to 10000 to have a high enough number that there is no concern of the algorithm stopping before maximum fluence is reached. This number can be adjusted depending on the performance of the ADC under test. At any point during the operation of the test, the execution of the algorithm in the logic analyzer can be stopped when the stored samples are saved to a file. This is accomplished by clicking on the red square stop button in the menu bar or by clicking **Stop** under the **Run/Stop** menu. The logic analyzer must be configured to capture the appropriate data and save it into a known location. This is selected under the **Run/Stop** menu as shown in Figure 4.

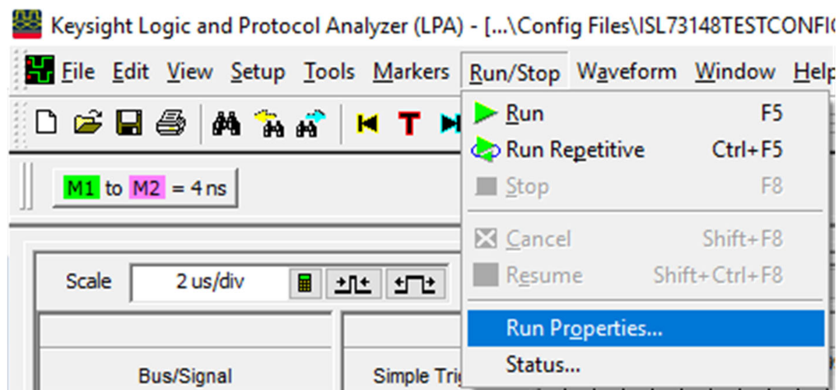

Figure 4. Run/Stop Menu Selection on the Keysight 16861A

From the **Run/Stop** menu the **Run Properties** selection is chosen to specify what is captured when the advanced trigger algorithm detects a sample outside the specified threshold. In this window (shown in Figure 5) the logic

analyzer is specified to save after every acquisition, to increment the file name between runs, and to stop running after 10 acquisitions (this stop is mostly just a precaution because one acquisition is all that is needed).

In addition, the file location and file type for the data is specified. In this example, a standard CSV file is specified. The data recorded includes all the data in the waveform so that the samples that violate the threshold along with the time stamps of each data point is recorded. Saving the time stamp along with the data allows the user to identify the length of each SET. This provides identification of single and multiple sample events by using software to calculate the time delta between time stamps to calculate the number of sample periods between recorded SET events.

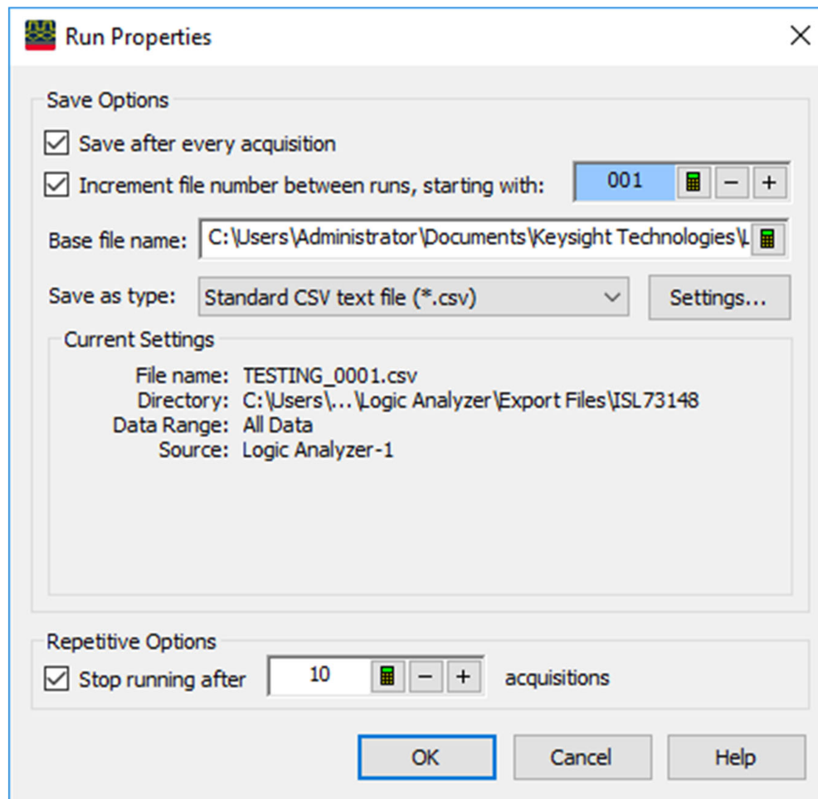

Figure 5. Run Properties Menu Selection

While performing a test run using this algorithm the logic analyzer continuously observes all ADC samples and only records samples to memory when a sample violates the specified threshold. When a sample is stored, the absolute time of that sample is also recorded, which gives the time since the start of the capture. The reported information from the logic analyzer provides the SET value in ADC codes. It can report several different data formats, but in this example decimal format is selected. To prevent runaway of the number of errors in this scenario, the detection algorithm increments a count each time an SET is detected and when a maximum user specified count (10000 in this example) is reached, the logic analyzer stops the test and saves the data to memory. A SEFI event can be identified if the counter reaches its maximum during the test. If the maximum is reached, a secondary read of the ADC output code is performed using a standard data capture in the logic analyzer. If the ADC output code remains at a value outside of the expected range, a SEFI may have occurred. If subsequent reads provide no change in the output code and an error remains, the next step is to issue a device reset if the device has one available. If not, a power cycle must be performed. If no operation short of a power cycle clears the SET, a SEFI has occurred. An example of this behavior might be if the ADC output code is constant at 16383, which would indicate a full scale short. When this condition is identified, a reset of the device if available should be performed. During reset, another standard ADC capture is performed to see if the condition has remedied, and the ADC output code has returned to within the expected range. If not, a power cycle should be performed followed by another standard ADC data capture. At this point, it would be expected that the ADC output

code should return to its expected range and the event can be recorded as a SEFI. If the ADC output code does not return to the expected range after these steps, the ADC may have permanent damage.

3. Alternate FPGA Method

Alternatively, an FPGA can be used to collect and observe the SAR ADC output data. While the exact implementation is a little different, the algorithm itself uses the same method to identify and collect the SET data. When using an FPGA, there is no need to have a CPLD to perform the serial to parallel conversion of the data. Instead, the serial data output from the ADC can be converted to parallel data within the FPGA where it can be analyzed for SET. In this case, the FPGA would need to monitor the sample data for SET and only push the samples exhibiting SET to an on-board memory such as a RAM (Random Access Memory). There should be a method to allow for time stamping the SET event so that consecutive SET events can be detected. This could be achieved using something such as an internal counter and recording the count value along with each SET event. Like the maximum count value in the logic analyzer, the FPGA can be programmed for a maximum number of SET. When the maximum number is reached, the FPGA would exit the test routine and push the SET data to a memory. The data from the memory could then be pushed to a computer where software can be used to process the data. This separate software would perform post-processing of the data to determine the number and magnitude of single and multiple sample events. At the completion of each test, the ADC should be read to detect any potential SEFIs in a similar manner to the logic analyzer method. The final data can then be used to generate Weibull fit curves.

4. Summary

A test algorithm has been presented that provides detection of SET and SEFI for precision SAR ADCs. This test algorithm offers the user detection of single sample transient events, multiple sample transient events, and SEFI. The ADC is operated in a manner during SEE test to allow for both positive and negative excursions of the digital output codes. This test method exercises and observes the full range of the ADC to mimic the experience of a real application. The results of testing with this method allow for the heavy ion performance of the ADC to be projected in an application by plotting the Weibull fit curves for the saturation cross section and using the CRÈME96 model for the appropriate orbit.

4.1 Next Steps

Visit the Rad Hard Data Converters page.

5. Revision History

Revision	Date	Description
1.00	Nov 4, 2022	Initial release.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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