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APPLICATION NOTE

Using Timer V Output to Drive a Buzzer

Introduction

The timer V output function is used to output, from the timer V output pin (TOMV), two-kHz pulses for switch-enabled driving of a buzzer.

Target Device

H8/300H Tiny Series H8/3664

Contents

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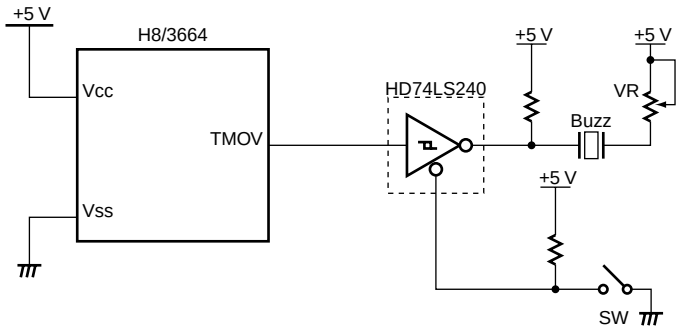
1. Specifications

1. The timer V output function is used to output, from the timer V output pin (TOMV), two-kHz pulses for switch-enabled driving of a buzzer.
2. Figure 1.1 shows the hardware configuration for connection of the timer V output to the buzzer. Turning on the switch sounds the buzzer.



Legend:
Buzz : Buzzer (PKM17EEP-2002-B0 from Murata Manufacturing Co., Ltd.)
SW : Push-button switch
VR : Variable resistor for turning up/down buzzer volume

Figure 1.1 Hardware Configuration

3. In this sample task, the H8/3664's operating voltage is 5.0 V and the frequency of oscillation of its system clock is 16 MHz.

2. Functional Description

1. In this sample task, driving of an output by the timer V compare-match function produces the 2-kHz pulses for the buzzer. Figure 2.1 shows the functional blocks used in the task. Table 2.1 describes the elements used and how they are specifically applied in this example.

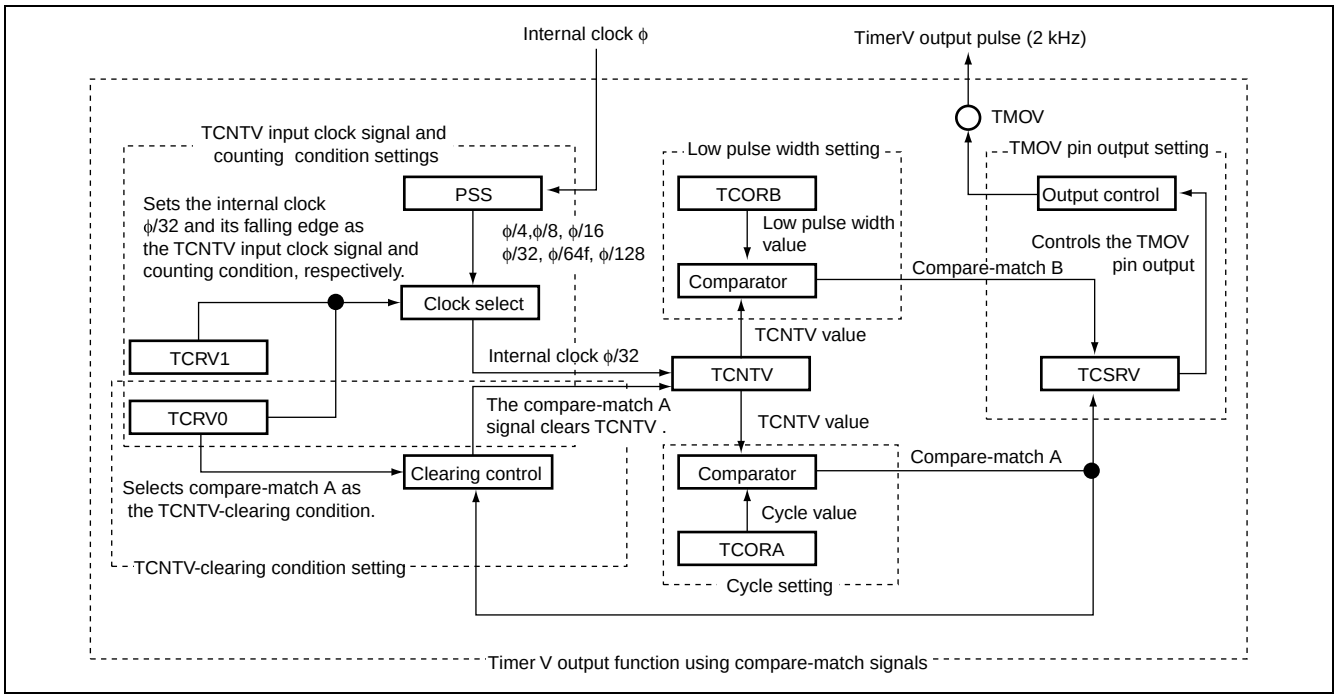
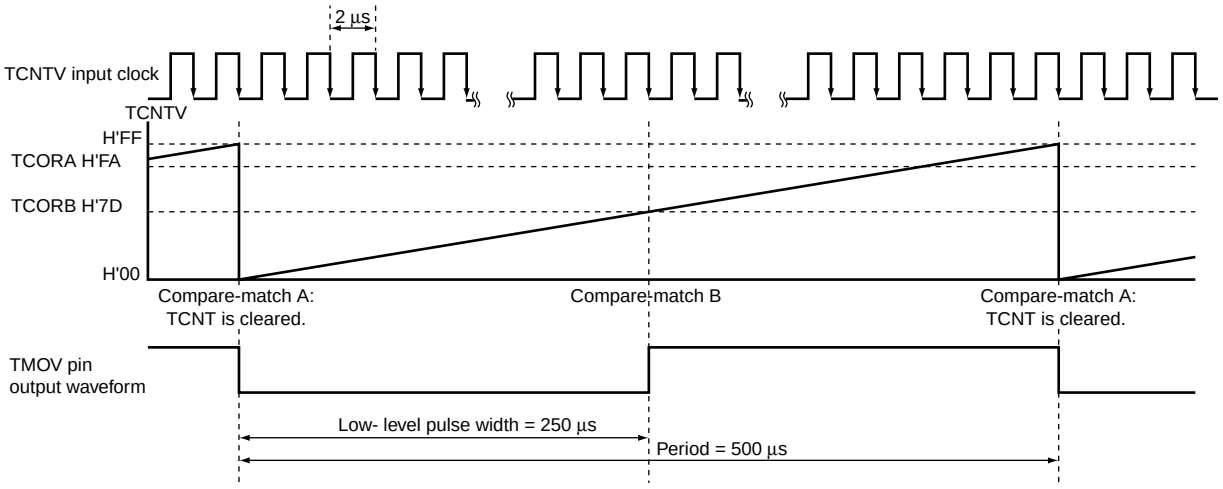


Figure 2.1 Using Timer V Compare-Match Signals to Drive an Output

Table 2.1 Function Assignment

Function	Function Assignment
TCORA	The TCORA value is constantly compared with the TCNTV value; when the values match, a compare-match A signal is generated. In this sample task, the signal is generated every 500 µs to set the timer V pulse-output period.
TCORB	The TCORB value is constantly compared with the TCNTV value; when the values match, a compare-match B signal is generated. In this sample task, the compare-match B signal B is generated 250 µs after the start of counting, to set the low-level period for the timer V output.
TCNTV	TCNTV selects the input clock signal and the signal condition to be counted, according to the combination of the values of CKS2 to CKS0 in the 8-bit counter control register TCRV0 and ICKS0 in TCRV1. The condition for clearing TCNTV is selected by the CCLR1 and CCLR0 bits of TCRV0.
TCSRV	TCSRV holds the status flags and controls the output on the TMOV pin for the respective compare-match signals. In this sample task, the compare-match B signal sets the output on the TMOV pin to 1 and the compare-match A signal sets the output on the TMOV pin to 0.
TCRV0	Settings in TCRV0 disable the applicable interrupt requests, and, in combination with the ICKS0 bit in TCRV1, the input clock signal for TCNTV and condition for the clearing of TCNTV. In this sample task, the internal clock ϕ/32 is selected as the input clock signal, with counting of the falling edge, and the compare-match A signal is selected as the TCNTV-clearing condition. All timer V interrupt requests are masked in this example.
TCRV1	Settings in TCRV1 disable TRGV input and select the input clock signal TCNTV. In this sample task, the internal clock ϕ/32 is selected as the input clock signal for TCNTV and the falling edge is selected as the condition to be counted; this is done in combination with the CKS2 to CKS0 values in TCRV0. Note that the TRGV input pin is not used in this task example.
TMOV	The TMOV pin outputs the timer V waveform. In this sample task, the value 1 is output on the TMOV pin by the active compare-match B signal, and the value 0 is output on the TMOV pin by the active compare-match A signal
PSS	This 13-bit counter receives the system clock signal (ϕ). The frequency-divided output from PSS is supplied to the on-chip peripheral modules as the internal clock signal. In this sample task, the system clock signal frequency-divided by 32 is supplied to TCNTV.

2. Figure 2.2 shows how the overall and low-level periods of the output waveform on the TMOV pin are set.



Notes: 1. Cycle = TCORA (H'FA) × 2 µs (prescaler S: 32 × system clock: 62.5 ns) = 500 µs
2. Low pulse width = TCORB (H'7D) × 2 µs (prescaler S: 32 × system clock: 62.5 ns) = 250 µs

Figure 2.2 Setting of the Overall and Low-Level Periods for the TMOV-Pin Output Waveform

3. Principles of Operation

1. Figure 3.1 shows the principle of operation for the TMOV-pin output. As the figure shows, pulses are output at 2 kHz from the pin through a combination of hardware and software processing.

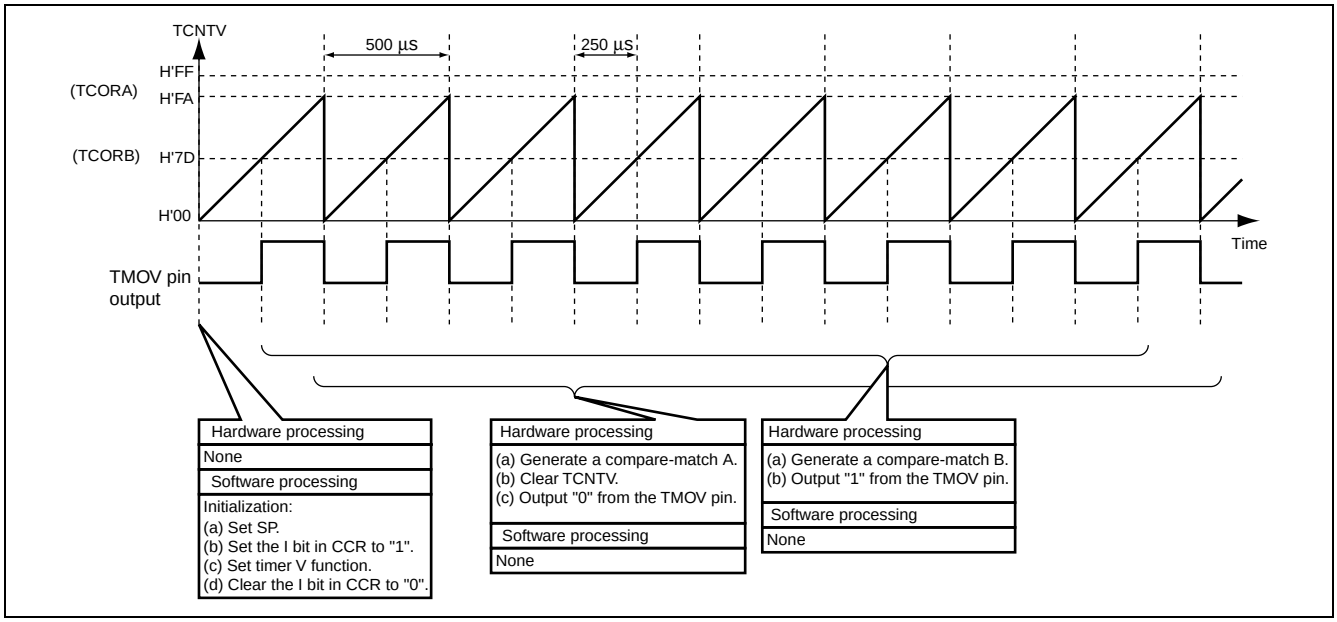


Figure 3.1 Operational Principle for TMOV Pin Output

2. Figure 3.2 shows the principle of operation for the buzzer-driving output. As shown in figure 3.2, turning on the switch enables the tri-state output inverter driver (HD74LS240) and produces a 2-kHz sound from the buzzer.

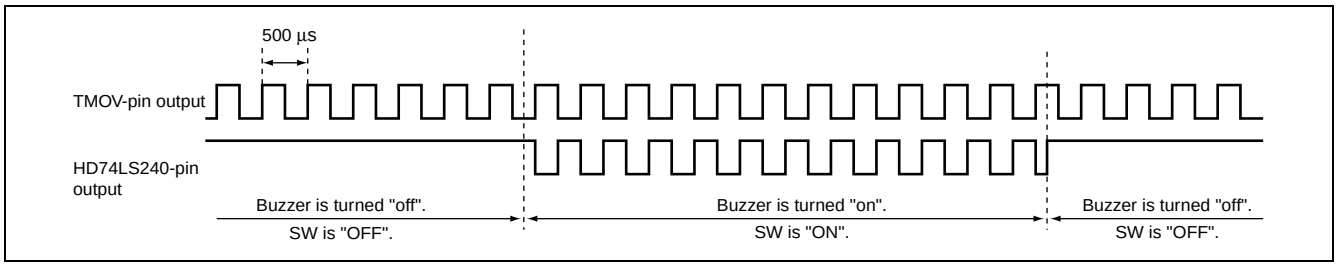


Figure 3.2 Operational Principle for Buzzer Output

4. Software Description

4.1 Module

Table 4.1 describes the single module of this task.

Table 4.1 Module descriptions

Module Name	Label Name	Function
Main routine	main	Initializes timer V and enables the applicable interrupt requests.

4.2 Arguments

No arguments are used in this task example.

4.3 Internal Registers Used

Table 4.2 describes the usage of internal registers in this task example.

Table 4.2 Internal Registers Used

Register Name		Function	Address	Setting
TCRV0		Timer control register V0: Selects the input clock signal and clearing condition for TCNTV, and enables/disables the applicable interrupt requests.	H'FFA0	H'0A
	CMIEB	Compare match interrupt enable B: When CMIEB = 0, interrupt requests from CMFB in TCSRV are disabled.	Bit 7	0
	CMIEA	Compare match interrupt enable A: When CMIEA = 0, interrupt requests from CMFA in TCSRV are disabled.	Bit 6	0
	OVIE	Timer overflow interrupt enable: When OVIE = 0, interrupt requests from OVF in TCSRV are disabled.	Bit 5	0
	CCLR1	Counter clear 1 and 0: Selects the condition for clearing of TCNTV. When CCLR1 = 0 and CCLR0 = 1, TCNTV is cleared on a match with the compare-match A value.	Bit 4	0
	CCLR0		Bit 3	1
	CKS2	Clock select 2 to 0: In combination with the ICKS0 value in TCRV1, selects the input clock signal for and condition to be counted by TCNTV. When CKS2 = 0, CKS1 = 1, CKS0 = 0, and ICKS0 = 1, TCNTV is incremented on falling edges of the internal clock signal ϕ/32.	Bit 2	0
	CKS1		Bit 1	1
	CKS0		Bit 0	0

Table 4.2 Internal Registers Used (ctd.)

Register Name		Function	Address	Setting
TCSRV		Timer control/status register V: Holds status flags and controls output in response to the compare-match signals.	H'FFA1	H'19
	CMFB	Compare match flag B: When the TCNTV and TCORB values match, CMFB is set to 1.	Bit 7	0
	CMFA	Compare match flag A: When the TCNTV and TCORA values match, CMFA is set to 1.	Bit 6	0
	OVF	Timer overflow flag: When the TCNTV value overflows, OVF is set to 1.	Bit 5	0
	OS3	Output select 3 and 2: Selects the level placed on the TMOV pin by activation of the compare-match B signal. OS3 = 1 and OS2 = 0 select the high level.	Bit 3 Bit 2	1 0
	OS2			
	OS1	Output select 1 and 0: Selects the level placed on the TMOV pin by activation of the compare-match A signal. OS1 = 0 and OS0 = 1 select the low level.	Bit 1 Bit 0	0 1
	OS0			
TCORA		Time constant register A: The TCORA value is constantly compared with the TCNTV value; when the values match, the compare-match A signal becomes active.	H'FFA2	H'FA
TCORB		Time constant register B: The TCORB value is constantly compared with the TCNTV value; when the values match, the compare-match B signal becomes active.	H'FFA3	H'7D
TCNTV		Timer counter V: An 8-bit up-counter, here incremented by the system clock signal frequency-divided by 32 and cleared by the compare-match A signal.	H'FFA4	H'00

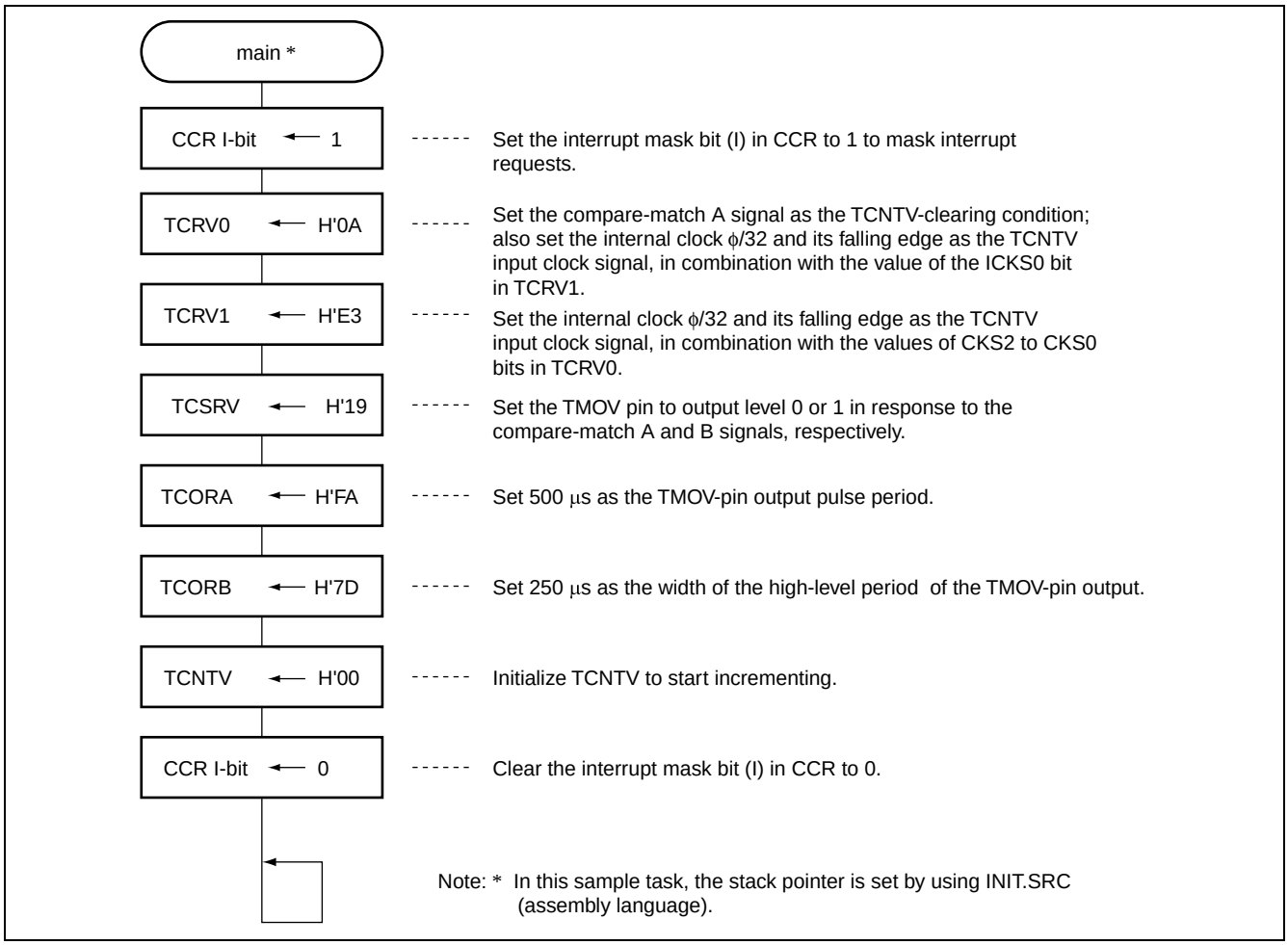
Table 4.2 Internal Registers Used (ctd.)

Register Name		Function	Address	Setting
TCRV1		Timer control register V1: Selects the valid TRGV pin edge, enables/disables TRGV input, and selects the input clock signal for TCNTV.	H'FFA5	H'E3
	TVEG1	TRGV input edge select 1 and 0:	Bit 4	0
	TVEG0	Selects the valid TRGV pin input edge. TVEG1 = 0 and TVEG0 = 0 disable the trigger input from the TRGV pin.	Bit 3	0
	TRGE	TRGV input enable: Enables/disables incrementing of TCNTV on input of the edge/edges selected by TVEG1 and TVEG0. TRGE = 0 disables starting and stopping of TCNTV incrementation on TRGV pin input and clearing of TCNTV by the compare-match signal, respectively.	Bit 2	0
	ICKS0	Internal clock select 0: In combination with the CKS2 to CKS0 values in TCRV0, selects the input clock signal and the condition for counting by TCNTV. When CKS2 = 0, CKS1 = 1, CKS0 = 0, and ICKS0 = 1, TCNTV is incremented on falling edges of the internal clock signal ϕ/32.	Bit 0	1

4.4 RAM Usage

No RAM is used in this task example.

5. Flowchart


main *
CCR I-bit ← 1
Set the interrupt mask bit (I) in CCR to 1 to mask interrupt requests.
TCRV0 ← H'0A
Set the compare-match A signal as the TCNTV-clearing condition; also set the internal clock ϕ/32 and its falling edge as the TCNTV input clock signal, in combination with the value of the ICKS0 bit in TCRV1.
TCRV1 ← H'E3
Set the internal clock ϕ/32 and its falling edge as the TCNTV input clock signal, in combination with the values of CKS2 to CKS0 bits in TCRV0.
TCSRV ← H'19
Set the TMOV pin to output level 0 or 1 in response to the compare-match A and B signals, respectively.
TCORA ← H'FA
Set 500 μs as the TMOV-pin output pulse period.
TCORB ← H'7D
Set 250 μs as the width of the high-level period of the TMOV-pin output.
TCNTV ← H'00
Initialize TCNTV to start incrementing.
CCR I-bit ← 0
Clear the interrupt mask bit (I) in CCR to 0.
Note: * In this sample task, the stack pointer is set by using INIT.SRC (assembly language).

6. Program Listing

INIT.SRC (program listing)

```
      .EXPORT  _INIT
      .IMPORT  _main
 ;
      .SECTION    P,CODE
 _INIT:
      MOV.W    #H'FF80,R7
      LDC.B    #B'10000000,CCR
      JMP      @_main
 ;
      .END
```

```
/* H8/300H Tiny Series -H8/3664- Application Note     */
/* Advanced 1                                        */
/* ~ Driving of a Buzzer by Timer V Output           */

#include   <machine.h>

/* Symbol definition                                 */
#define TCRV0 *(volatile unsigned char *)0xFFA0       /* Timer control register V0                    */
#define TCSRV *(volatile unsigned char *)0xFFA1       /* Timer control/status register V              */
#define TCORA *(volatile unsigned char *)0xFFA2       /* Time constant register A                     */
#define TCORB *(volatile unsigned char *)0xFFA3       /* Time constant register B                     */
#define TCNTV *(volatile unsigned char *)0xFFA4       /* Timer counter V                              */
#define TCRV1 *(volatile unsigned char *)0xFFA5       /* Timer control register V1                    */

/* Function definition                               */
extern void INIT(void);                               /* Set stack pointer                            */
void main(void);                                      /* Main routine                                 */

/* Vector address */
#pragma section V1                                    /* Vector-setting section                       */
void (*const VEC_TBL1[])(void) = {
    INIT                                              /* H'0000 Reset vector                          */
};
#pragma section                                       /* P                                            */
/* Main program                                      */
void main(void)
{
```

```
    set_imask_ccr(1);                       /* CCR I-bit = 1                    */

TCRV0 = 0x0a;                               /* Initialize Timer V               */
    TCRV1 = 0xe3;
    TCSRV = 0x19;
    TCORA = 0xfa;                           /* Compare match A period = 500us   */
    TCORB = 0x7d;                           /* Compare match B period = 250us   */
    TCNTV = 0x00;

    set_imask_ccr(0);                       /* CCR I-bit = 0                    */

    while(1);
}
```

Link addresses:

Section Name	Address
CV1	H'0000
P	H'0100