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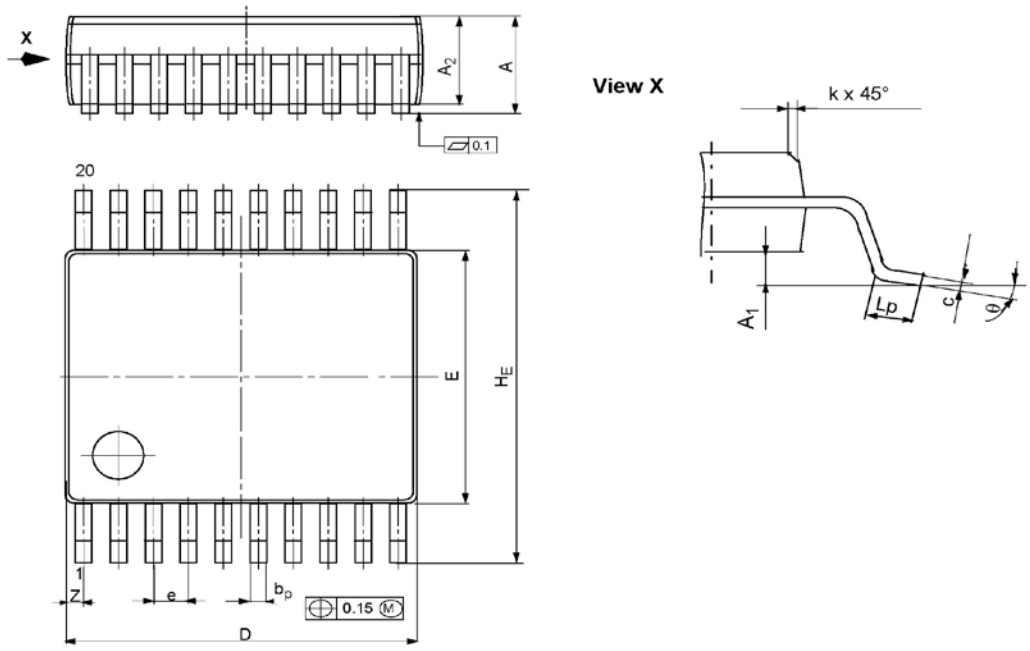
1 ZSSC3170 SSOP20 Package

The SSOP20 package is RoHS-compliant and based on JEDEC JEP95: MO-150. Package dimensions are given in millimeters in Figure 1.1.

1.1. SSOP20 Package Dimensions

Figure 1.1 Package View and Dimensions



Dimensions of Sub-Group B1	
A_{max}	1.99
b_{Pmin}	0.25
b_{Pmax}	0.38
e_{nom}	0.65
H_{Emin}	7.65
H_{Emax}	7.90
L_{Pmin}	0.63
Z_{max}	0.74

2	**Weight**	≤ 0.3 g
3	**Package Body Material**	Low Stress Epoxy
4	**Lead Material**	FeNi-Alloy or Cu-Alloy
5	**Lead Finish**	solder plating
6	**Lead Form**	Z-bends

Dimensions of Sub-Group C1	
A_{min}	1.73
A_{1min}	0.05
A_{1max}	0.21
A_{2min}	1.68
A_{2max}	1.78
c_{min}	0.09
c_{max}	0.20
D_{min}*	7.07
D_{max}*	7.33
E_{min}*	5.20
E_{max}*	5.38
k_{min}	0.25
θ_{min}	0°
θ_{max}	10°

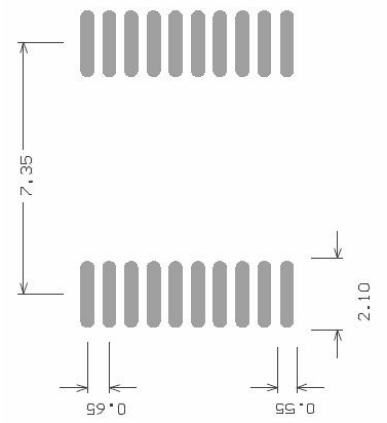
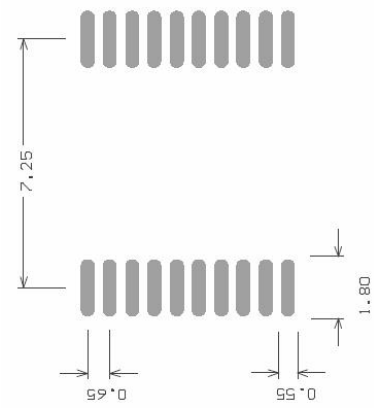
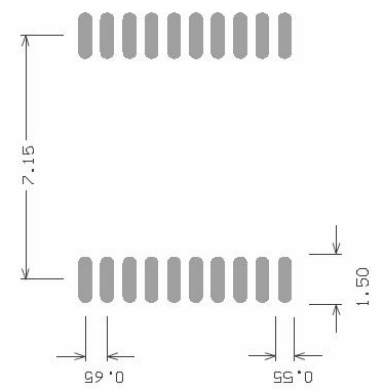
* without mold-flash

Note: Drawing is not true to scale.

1.2. Recommended Printed Circuit Board Layout – SSOP20 Package

The recommended printed circuit board layout for the SSOP20 package depends on the board density.

Figure 1.2 Recommended Printed Circuit Board Layout – SSOP20 Package

SSOP20 Layout for Low Density	SSOP20 Layout for Medium Density	SSOP20 Layout for High Density
		

1.3. SSOP20 Package Marking and Pin Assignments

Table 1.1 SSOP20 Package Marking

Top Side		Comments
1st Line	ZSSC	
2nd Line	3170EA or 3170EE	3170 = Product name; E = Revision Identifier; A= Temperature Range Identifier or 3170 = Product name; E = Revision Identifier; E = Temperature Range Identifier
3rd Line	XXXXXXXX	Lot number
4th Line	YYWW	YY = Year (e.g., 14 for 2014, 15 for 2015, ...); WW = Workweek (e.g., 15)

Table 1.2 Pin Assignments

SSOP20 Pin	Name	Description	Remarks
1	n.c.	No connection	
2	VDDA	Positive Analog Supply Voltage	Power supply
3	VSSA	Negative Analog Supply Voltage	Ground
4	SDA	I²C™* Data I/O	Analog I/O, internal pull-up
5	SCL	I²C™ Clock	Analog input, internal pull-up
6	VDD	Positive Digital Supply Voltage	Power supply
7	HOUT	PWM High-Side Switch	High voltage I/O
8	VB	Positive External Supply Voltage	High voltage I/O
9	VSSE	External Ground (PWM Modes)	High voltage I/O
10	VSS	Ground (LIN Mode)	Ground
11	LIN	LIN	LIN high voltage I/O
12	LOUT	PWM Low-Side Switch	High voltage I/O
14	VBN	Negative Input Sensor Bridge	Analog input
15	VBR_B	Negative (Bottom) Bridge Supply Voltage	Analog I/O
16	VBP	Positive Input Sensor Bridge	Analog input
17	VTN1	Temperature Sensor 1	Analog I/O
18	VBR_T	Positive (Top) Bridge Supply Voltage	Analog I/O
19	VTN2	Temperature Sensor 2	Analog I/O
20	n.c.	No connection	

* I^2C™ is a trademark of NXP.

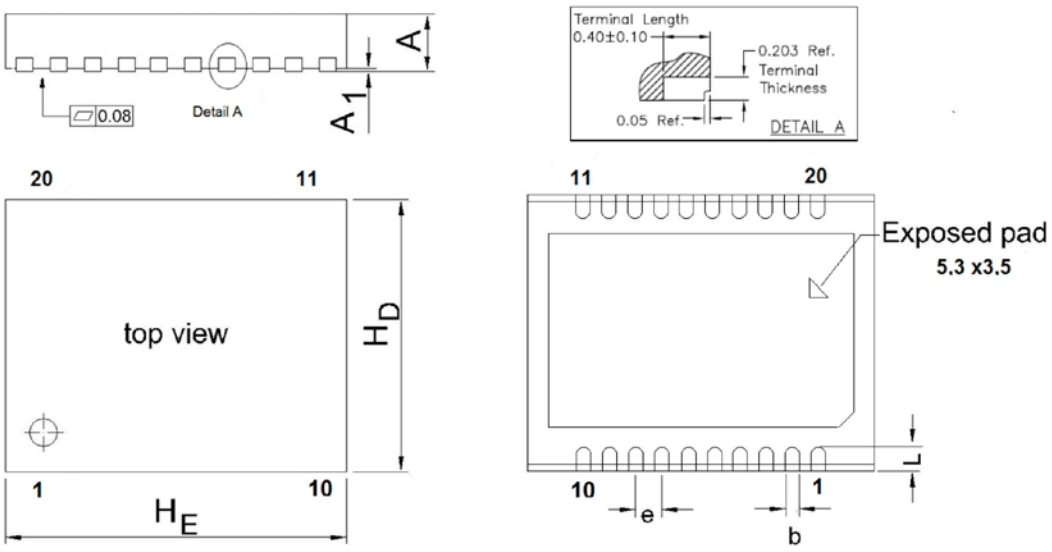
2 DFN20 Package

The ZSSC3170 is also available assembled in a DFN20 package (sales codes ZSSC3170EE3R and ZSSC3170EA3R) with wettable flanks. For this package option, the pin assignments are the same as for the SSOP20 package. The DFN20 package is RoHS-compliant.

2.1. DFN20 Package Dimensions

The figure below provides the dimensions in mm for the DFN20 package, which are based on JEDEC MO-229.

Figure 2.1 Outline Drawing for DFN20 Package with Wettable Flanks



Dimensions	min	max
A	0.8	0.9
A_1	0	0.05
b	0.2	0.3
e	0.5 nom	
H_D	4.9	5.1
H_E	5.9	6.1
L	0.3	0.5

Weight	≤ 0.05 g
Package Body Material	Low Stress Epoxy
Lead Material	Cu-Alloy
Lead Finish	solder plating

2.2. Footprint and Wettable Flank Description

Figure 2.2 Recommended Printed Circuit Board Footprint – DFN20

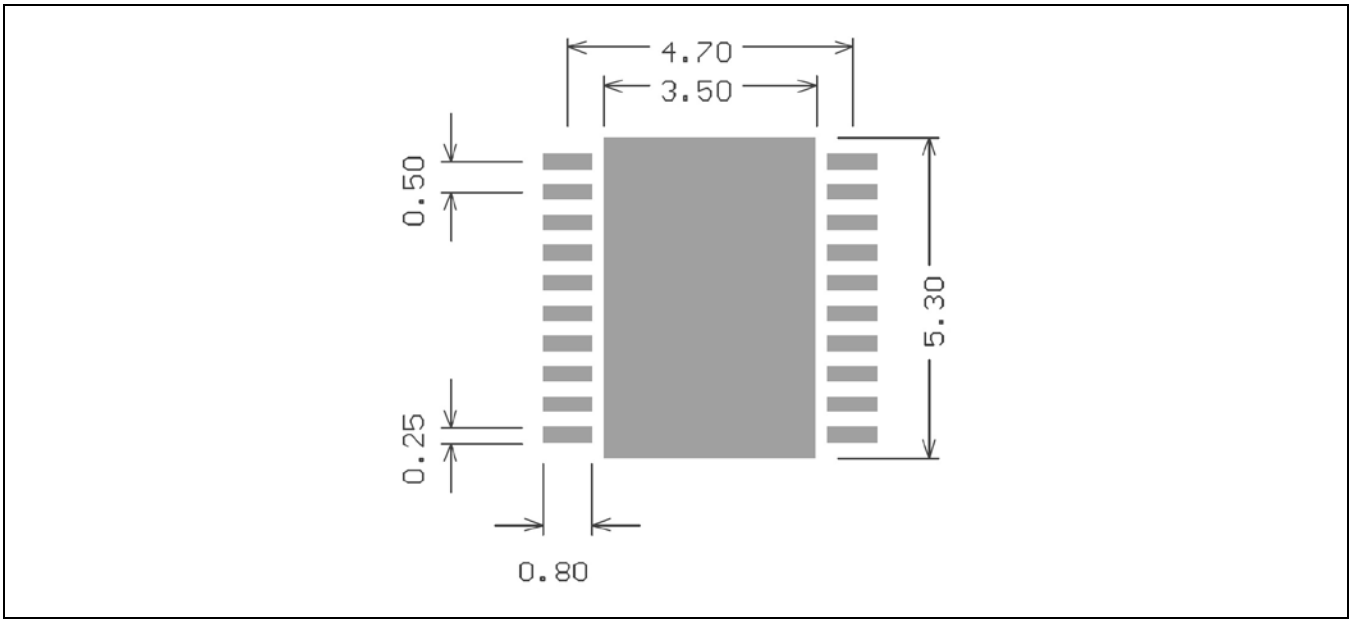


Figure 2.3 illustrates the general concept of the wettable flank (side plating), which allows automatic optical inspection.

Figure 2.3 Wettable Flank General Concept

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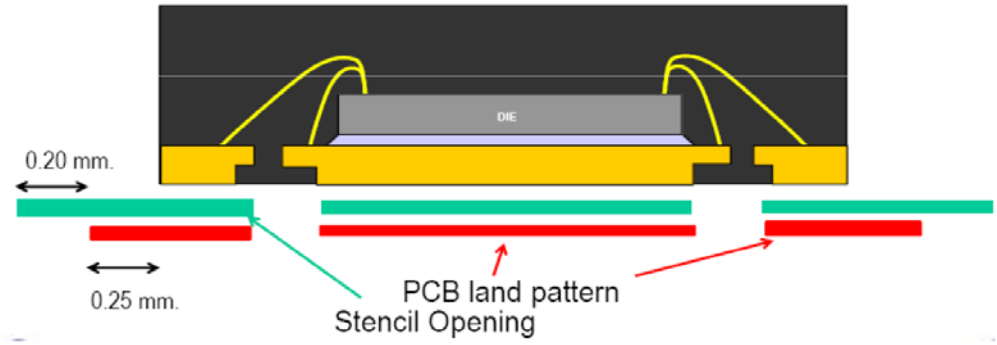
Figure 2.4 illustrates a suggested footprint for printed circuit board (PCB) designs using the ZSSC3170 DFN20.

- The exposed area of the landing pattern is 0.25mm for the unit edge.
- The stencil opening excess is about 0.2mm from the landing pattern.

Figure 2.4 Footprint Dimensions for DFN20 with Wettable Flanks



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2.3. DFN20 Package Marking

Table 2.1 DFN20 Package Marking

Top Side		Comments
1st Line	3170EA or 3170EE	3170 = Product name; E = Revision Identifier; A= Temperature Range Identifier or 3170 = Product name; E = Revision Identifier; E = Temperature Range Identifier
2nd Line	XXXXX	Last five digits of IDT lot number
3rd Line	YYWW	YY = Year (e.g., 14 for 2014, 15 for 2015, ...); WW = Workweek (e.g., 15)

3 Storage Conditions

For detailed information about storage conditions requirements, refer to the document *IDT Storage Conditions*. This document is included in all deliveries of packaged parts. It is also available upon request (see contact information on page 8).

4 Related Documents

Document
ZSSC3170 Data Sheet
ZSSC3170 Functional Description
IDT Storage Conditions

Visit the ZSSC3170 product page (www.IDT.com/ZSSC3170) or contact your nearest sales office for the latest version of these documents.

5 Document Revision History

Revision	Date	Description
1.00	April 5, 2009	First release.
2.00	March 31, 2010	Update for revision C.
2.10	July 19, 2010	Change of product name to ZSSC3170. Change to IDT's new documentation template. Completely revised version.
2.20	September 14, 2010	Update for revision D of the ZSSC3170
2.30	April 11, 2013	Update for revision E of the ZSSC3170. Pad layout and SSOP20 drawings added.
2.40	February 12, 2014	Added wafer drawing and defined scribe line.
2.50	December 3, 2014	DFN20 package added. Update for contact information.
2.51	December 10, 2014	Correction for definitions of SDA and SCL in Table 1.2. Update for e-mail contact.
2.60	December 8, 2015	Separation of document into separate technical notes for die dimensions and for package dimensions. Addition of land patterns. Updates for related documents.
	April 1, 2016	Changed to IDT branding.

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