ZSSC3286 + RH4Z2501 Reference Designs

QFN/DFN and WLCS Packages

This application note presents two reference designs for an IO-Link device sensing solution featuring the ZSSC3286 and RH4Z2501. It highlights essential design elements in both the circuit diagram and PCB layout, with a focus on optimizing EMC performance and thermal considerations.

Target devices:

- RH4Z2501 single channel IO-Link physical layer transceiver with integrated protection
- ZSSC3286 IO-Link Ready Dual Channel Resistive Sensor Signal Conditioner IC

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1. Introduction

IO-Link devices must be qualified at system level in accordance with the *IO-Link Interface and System Specification*. The success of passing the environmental tests largely depends on the device's design. Some tests like Burst, EMC and ESD tests are mandatory, while others like Surge test are recommended. To minimize the risk of design errors and to ease the design effort for the device manufacturer, this application note presents two reference designs (different IC packages) of an IO-Link sensing solution, which consists of the combination of ZSSC3286 and RH4Z2501. It covers general best practices and design guidelines, as well as the reference solutions in detail. Both the circuitry and the board layout are considered.

Note: The reference designs shown in this document serve as a guideline. Any adjustments and/or modifications made by the customer to create a comprehensive sensor product are not guaranteed to ensure a product that passes the tests.

Reference documents:

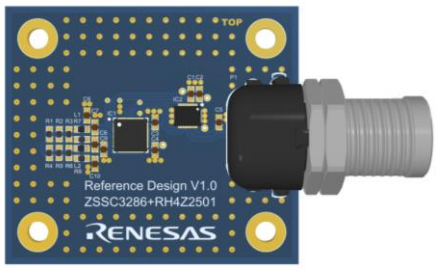
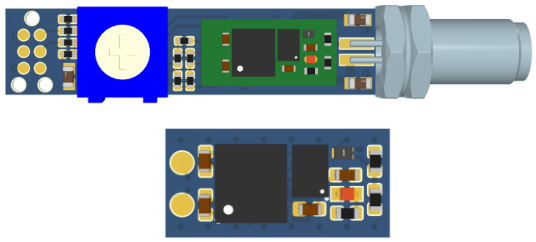
- ZSSC3286 Datasheet document (Reference 1)
- RH4Z2501 Datasheet document (Reference 2)
- ZSSC324x EMC document (Reference 3)

2. Reference Designs

2.1 Overview

Table 1 gives an overview of the two different reference design solutions, both realizing a single channel IO-link device.

Table 1. Reference Designs Overview

Criteria	Reference Design 1: QFN / DFN	Reference Design 2: WLCSP
Picture		
IC package	ZSSC3286: QFN RH4Z2501: DFN	ZSSC3286: WLCSP RH4Z2501: WLCSP
IO-Link connector	M12-4	M5-4
PCB technology	4 layers, 1.6mm Min. width / spacing: 0.15mm / 0.2mm	BGA; two-board solution Baseboard: 4 layers, 1.6mm Min. width / spacing: 0.2mm / 0.15mm Mini Module: 6 layers, 1.6mm Min. width / spacing: 0.1mm / 0.1mm
Use case	Robust and high functional design	Space-critical, high-integrity applications

Both designs passed the IO-Link conformance testing according to IO-Link Interface Specification V1.1.3:

- Functional Tests
  - Physical Layer Test — IO-Link Test Specification V1.1.3
  - Protocol Tests — IO-Link Test Specification V1.1.3
- Environmental Tests
  - Electrostatic Discharge (ESD) — IEC 61000-4-2
  - Electromagnetic field (HF) — IEC 61000-4-3
  - Fast Transient (Burst) ±2kV — IEC 61000-4-4
  - Surge (±1.25kV/2.5A 8/20µs pulse 500Ω) — IEC 61000-4-5 (DIN EN 60947-2)
  - Conducted radio frequency (CRF) — IEC 61000-4-6
  - Radiated emissions — EN 55011

2.2 General Recommendations

The following general design guidelines shall be considered when working with ZSSC3286 and RH4Z2501 to ensure compliance and optimal performance:

- Short tracks of communication signals between ZSSC3286 and RH4Z2501 (low exposure to noise)
- Separated board areas for
  - high voltage (IO-Link: 24V) and low voltage (3.3V / 5V) power and signals
  - analog (ZSSC3286 front end) and digital (IO-Link, OWI) signals
- Grouping / separating signals, e.g. according to EMC sensitivity and emission
- Solid, uninterrupted GND and VDD planes
- Via stitching for GND layers, enforced around PCB edge (low impedance return path, shielding around PCB edge)
- Place decoupling / stabilization capacitors close to the corresponding supply or signal pins; routing signal tracks directly via capacitor pad
- Optimized exposed pads, especially on RH4Z2501 for improved thermal conductivity
  - Multiple vias for better heat conduction
  - Large, continuous copper planes for effective heat dissipation

2.3 Reference Design 1: QFN (ZSSC3286) / DFN (RH4Z2501) Packages

2.3.1. Schematic Reference Design 1

Figure 1 illustrates the reference design schematic using QFN (ZSSC3286) / DFN (RH4Z2501) packages. It realizes a single channel sensing solution: The raw sensor signal from the sensor element (resistor bridge) is measured and corrected by the ZSSC3286. The digitalized data is then transmitted via UART interface to the RH4Z2501 IO-Link transceiver that converts it into IO-Link format. The ZSSC3286 configures the RH4Z2501 via OWI. The analog frontend consists of six resistors representing a resistive bridge sensor element. The simulated sensor element is connected to an EMC filter network consisting of L1 L2, C6-C10 and R7, R8 (Reference 3).

Both ZSSC3286 and RH4Z2501 use 5V logic power supply. This requires that the 5V and 3V3 pins on RH4Z2501 are connected. The exposed pads of the ICs are connected to GND. Capacitors C1-C4 are implemented according to IC's datasheets. The 100nF blocking capacitor C5 is connected to L+. A commonly used M12-4 connector is chosen for IO-Link interface.

Note: During surge event, the capacitance on L+ causes longer discharge current through internal TVS diodes of RH4Z2501 when internal surge protection is enabled. The RH4Z2501 successfully passed testing with 100nF capacitor at L+. If higher capacitances are necessary, especially when placed close to VDD pin, external surge protection using TVS diodes should be considered.

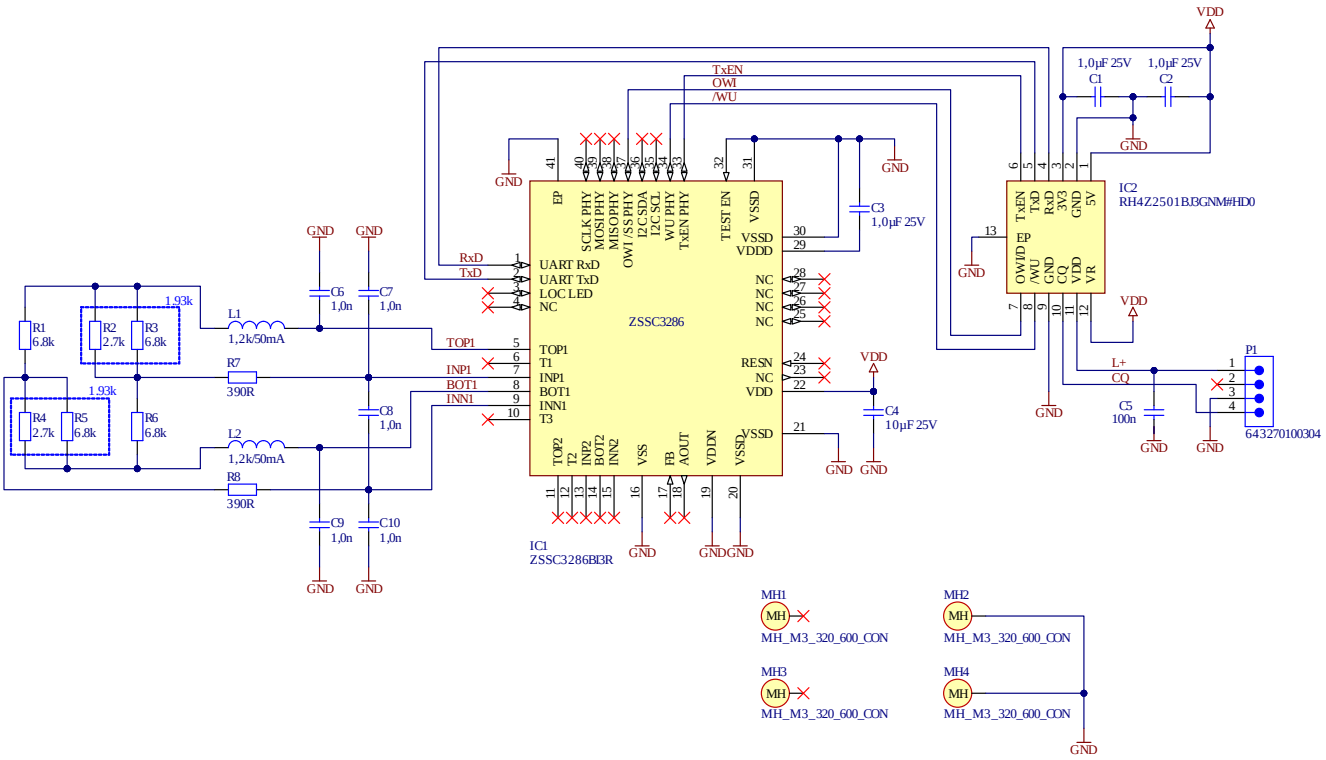


Figure 1. Schematic Reference Design 1

2.3.2. PCB Reference Design 1

Table 2 presents the PCB stack-up used for this design. Figure 2 to Figure 5 show the copper layer layouts.

Table 2. PCB stack-up Reference Design 1

Layer	Signals	Function	Drawing
TOP	Most signals, flooded with GND	Primary routing	Figure 2
Layer 2	GND	Reference GND plane for TOP Layer and Inner Layer 3	Figure 3
Layer 3	VDD 5V, Remaining misc. signals	Low impedance power plane, Secondary routing	Figure 4
BOT	GND	Reference plane for Inner Layer 3 / Shielding	Figure 5

Although 4-layer stack-up is recommended, a 2-layer design can be cheaper and simpler:

- TOP Layer: All signals, VDD, flooded with GND
- BOT Layer: GND

Figure 6 illustrates the TOP layer layout / component placement of the board. Areas marked with rectangular boxes are representing functional blocks classified by signal type:

1. Low voltage (<2V), analog
2. Low voltage (5V), digital
3. High voltage (24V), digital

These blocks should be kept separated from each other, avoiding intra-PCB EMC problems such as crosstalk.

Decoupling capacitors C1, C2, C3 and C4 are kept close to the respective pin, and tracks are routed directly via the pads. C5 is placed close to the M12-4 IO-Link connector to block noise entering the circuit on L+ line.

The shield of the M12-4 connector is not connected to GND of the PCB to avoid noise coupling into the GND plane.

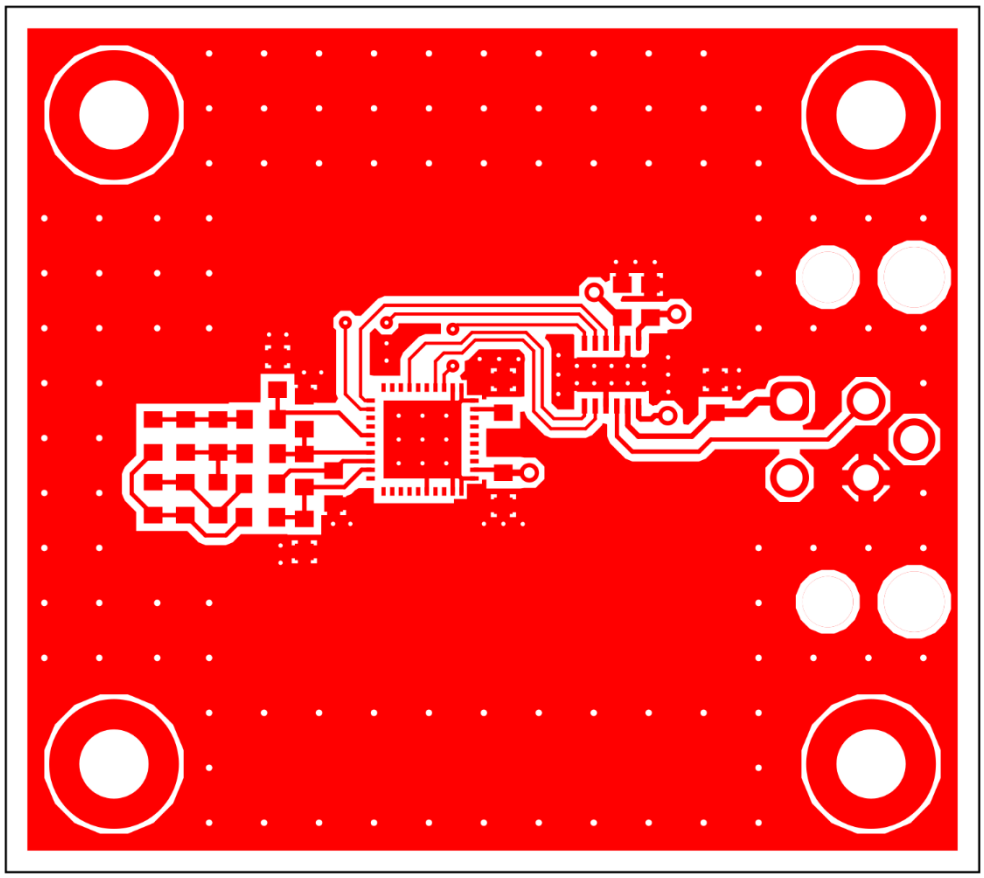


Figure 2. Reference Design 1 - TOP Layer

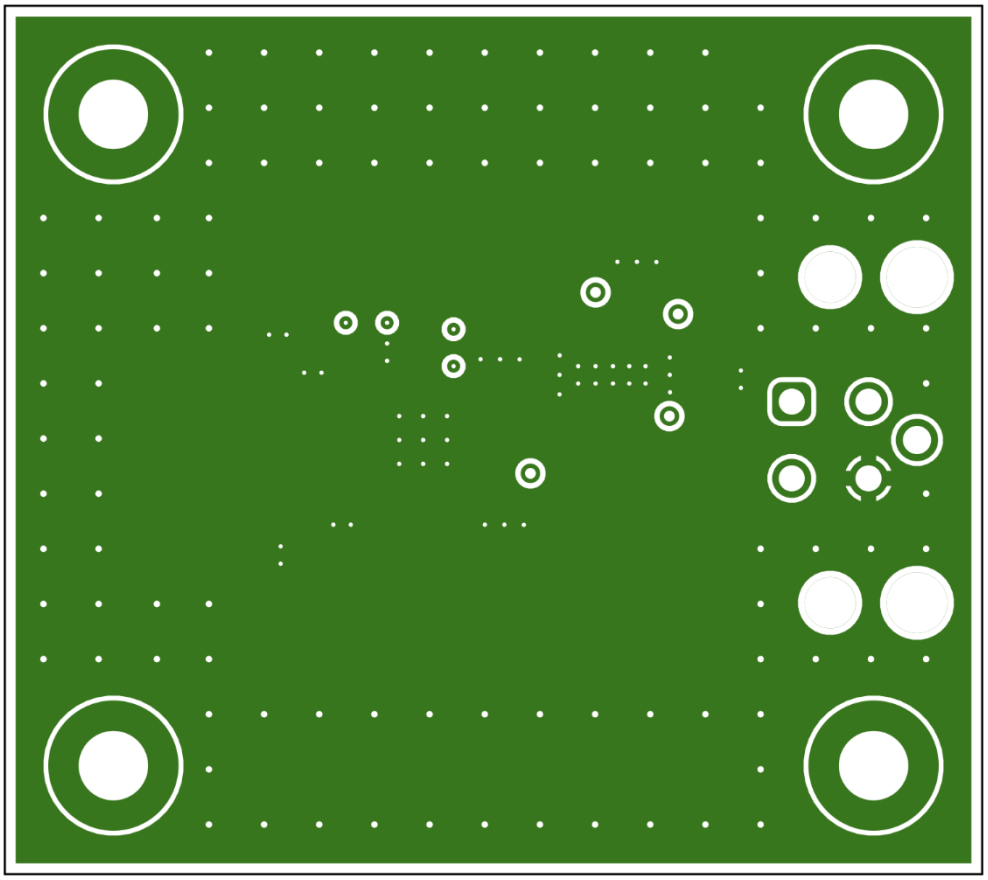


Figure 3. Reference Design 1 - Layer 2

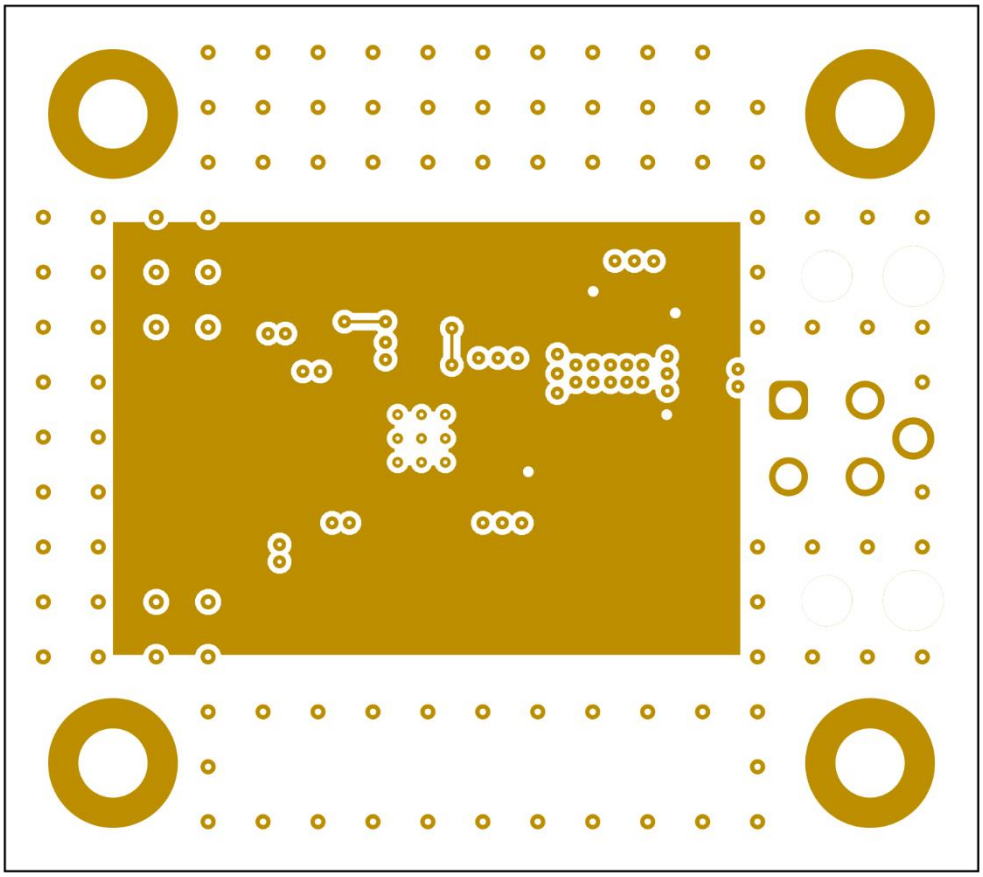


Figure 4. Reference Design 1 - Layer 3

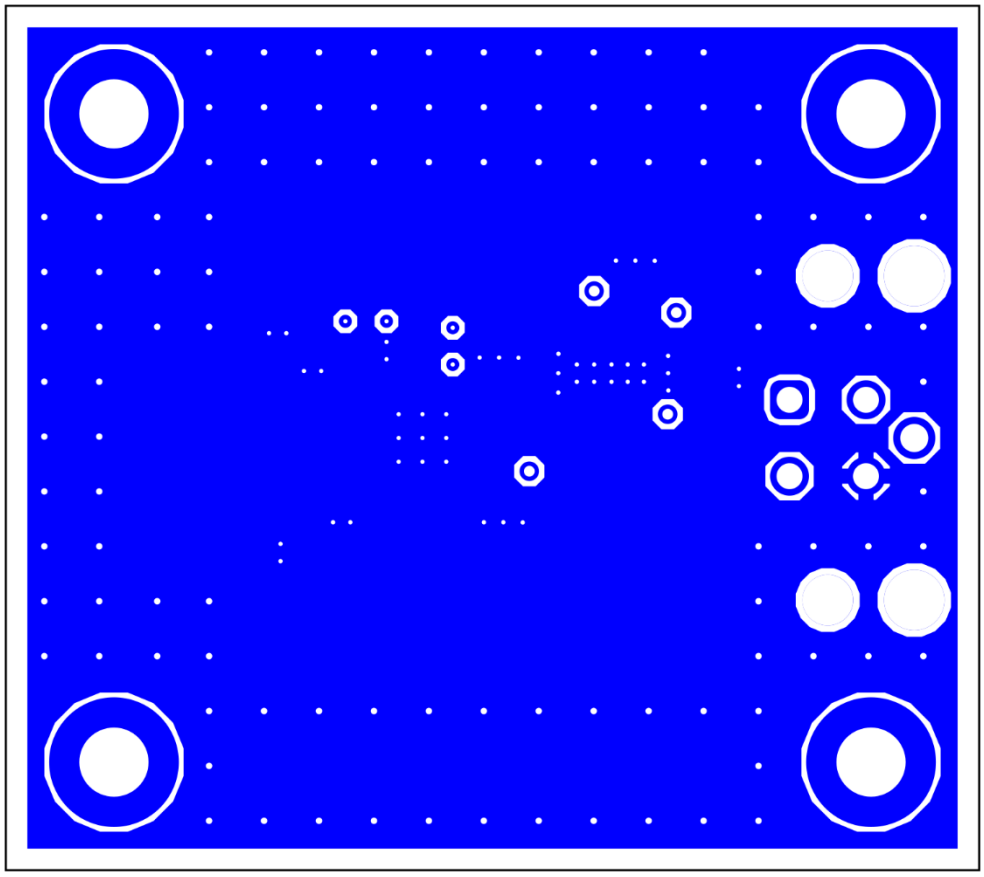


Figure 5. Reference Design 1 - BOT Layer

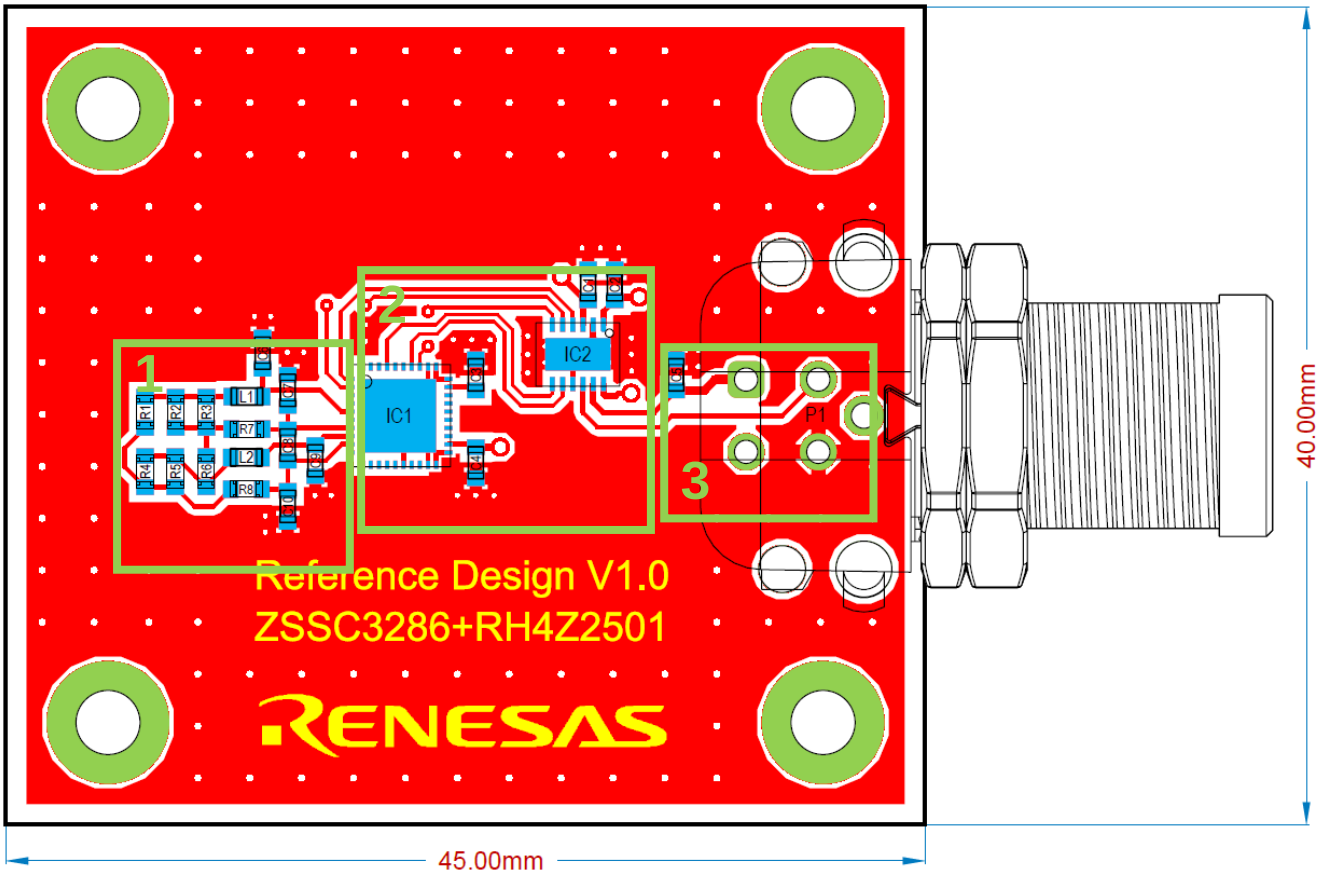


Figure 6. Reference Design 1 - Assembly View TOP

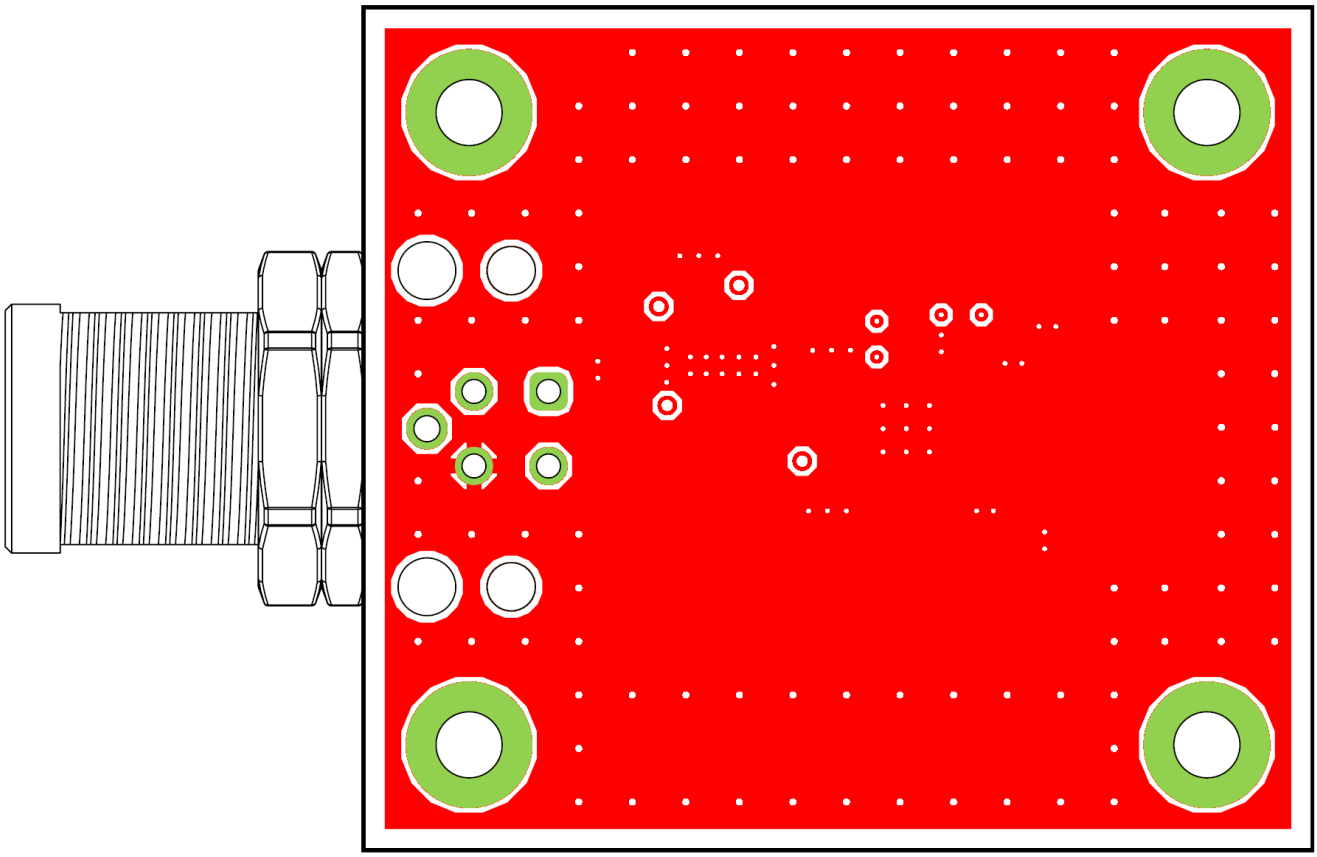


Figure 7. Reference Design 1 - Assembly View BOT

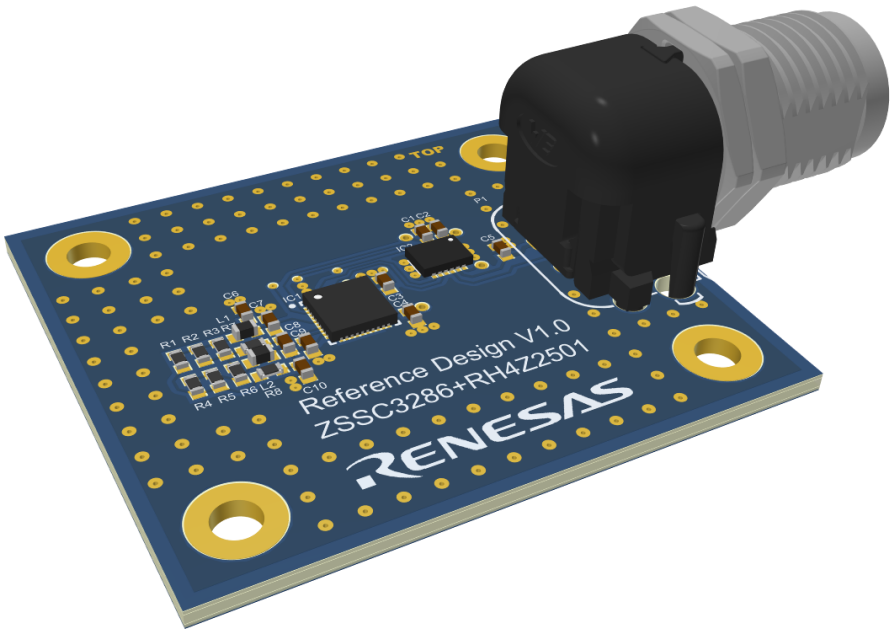


Figure 8. Reference Design 1 - 3D View

2.4 Reference Design 2: WLCSPs

Reference Design 2 realizes an ultra-small formfactor sensing solution using a two-board approach: The Base Board and the Mini Module. The Base Board carries the Mini Module as an LGA PCB, connecting it to a simulated sensor element (resistor bridge and potentiometer) and to an M5-4 IO-Link connector. The focus of the Reference Design 2 is clearly on the Mini Module. It puts both ZSSC3286 and RH4Z2501 as WLCSPs in a high-integrity form factor smaller than the size of a thumbnail, ideal for high-integrity sensor applications. The Mini Module should be seen as a cutout from a commercial sensor PCB, not as a stand-alone module to be placed on a final product.

2.4.1. Schematic Reference Design 2

Like Reference Design 1, the Mini Module represents a single channel sensor. Both ZSSC3286 and RH4Z2501 work with 3.3V logic natively but can be set to 5V by connecting 3V3 and 5V externally. Capacitors C1-C4 are selected according to IC's datasheets. As in Reference Design 1, a 100nF blocking capacitor (C1) is placed at L+. The pins AOUT and FB are connected, not using the internal connection setting of ZSSC3286. An LED (D1) is connected to GPIO1 to enable IO-Link Locator functionality. GPIO15 controls an open collector digital output, used as a binary output signal. RESN, TEST_EN, MOD1 and MOD2 signals are routed out for debug purposes. Due to the closeness of both ICs, they share one 1µF capacitor on 3V3 supply. The exposed pad of the Mini Module facilitates heat to the Base Board.

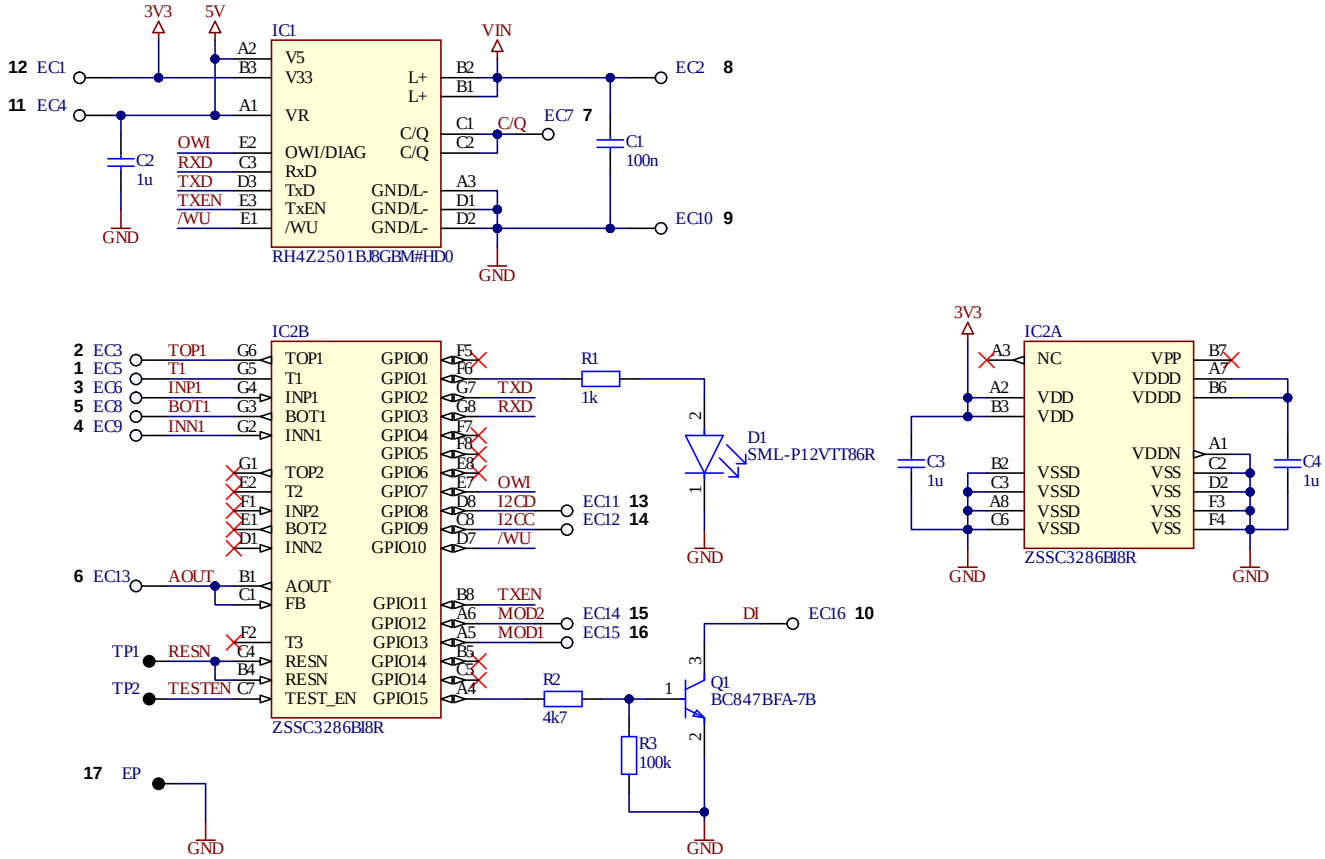


Figure 9. Schematic Reference Design 2: Mini Module

The Base Board works as a carrier to connect the Mini Module to a resistor bridge (sensor replacement) and an IO-Link connector (M5-4). Connector J2 with resistors R5-R8 is used for debug purposes and is not applicable to a sensor product. AOUT and I2C signals are not routed on the Base Board.

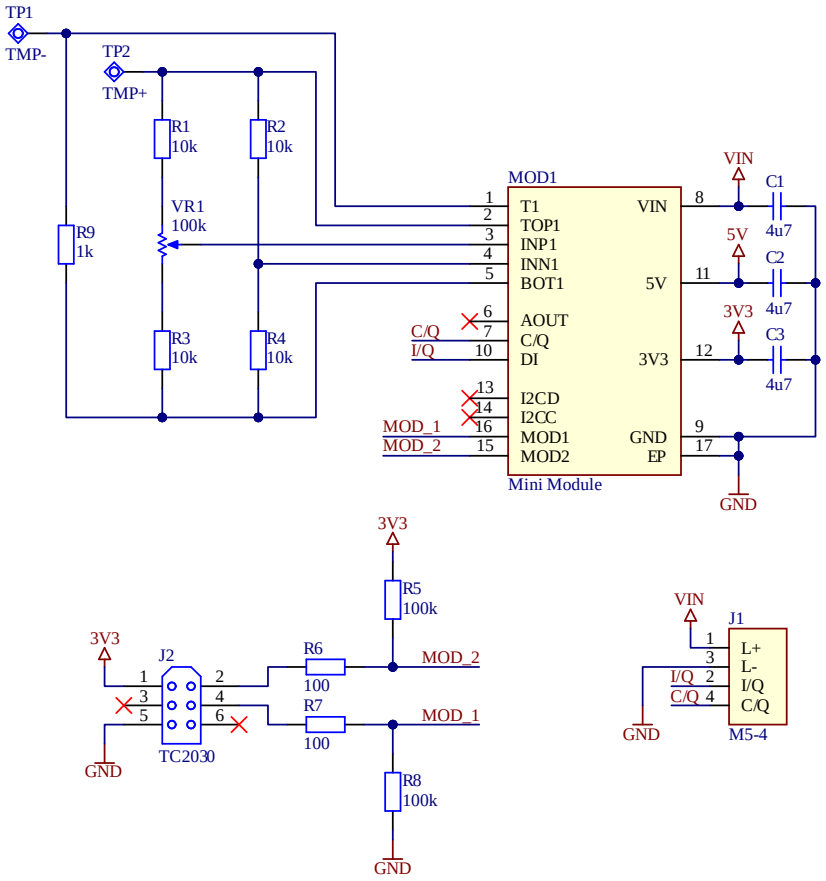


Figure 10. Schematic Reference Design 2: Base Board

2.4.2. PCB Reference Design 2

Table 3 presents the PCB stack-up for the Base Board. Figure 11 to Figure 14 show the copper layer layouts.

Table 3. PCB stack-up Reference Design 2: Base Board

Layer	Signals	Function	Drawing
TOP	All signals	Primary routing	Figure 11
Layer 2	GND	Reference GND plane for TOP Layer	Figure 12
Layer 3	VDD 3.3V	Low impedance power plane	Figure 13
BOT	GND	Low impedance GND plane / Shielding,	Figure 14

There are three main areas of the base board (disregarding debug connector), marked with rectangular boxes:

1. Sensor replacement area
2. Mini Module
3. M5-4 IO-Link connector

A large, dedicated GND pad stitched with vias (Figure 11) ensures improved heat dissipation from the mini module into the GND layers of the Base Board.

Pads for J2 and the test points on BOT layer (Figure 16) are not needed for a commercial sensor design.

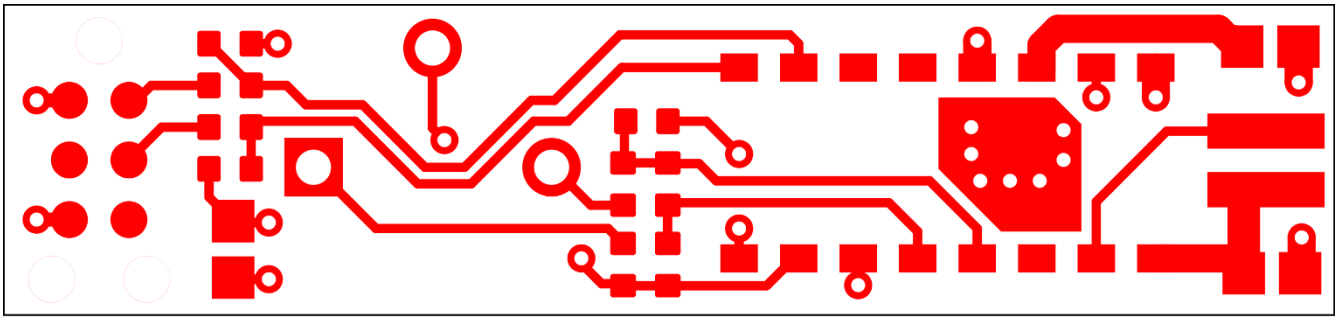


Figure 11. Reference Design 2: Base Board - TOP Layer

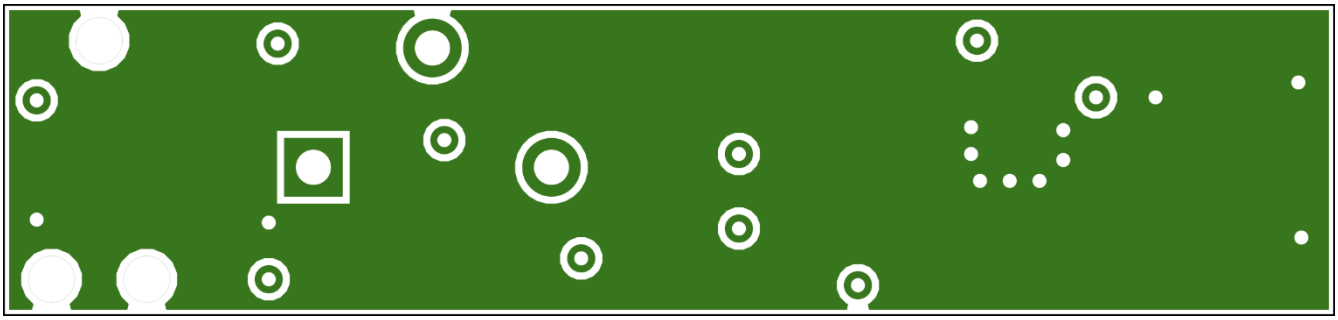


Figure 12. Reference Design 2: Base Board - Layer 2

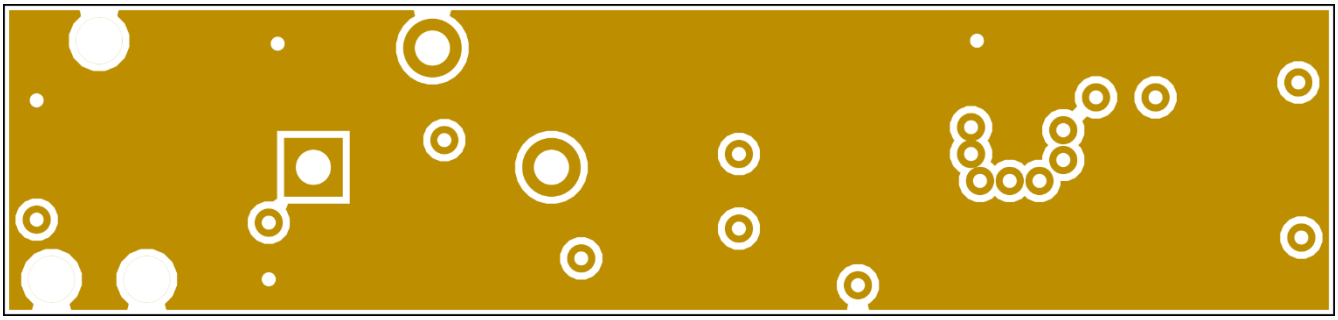


Figure 13. Reference Design 2: Base Board - Layer 3

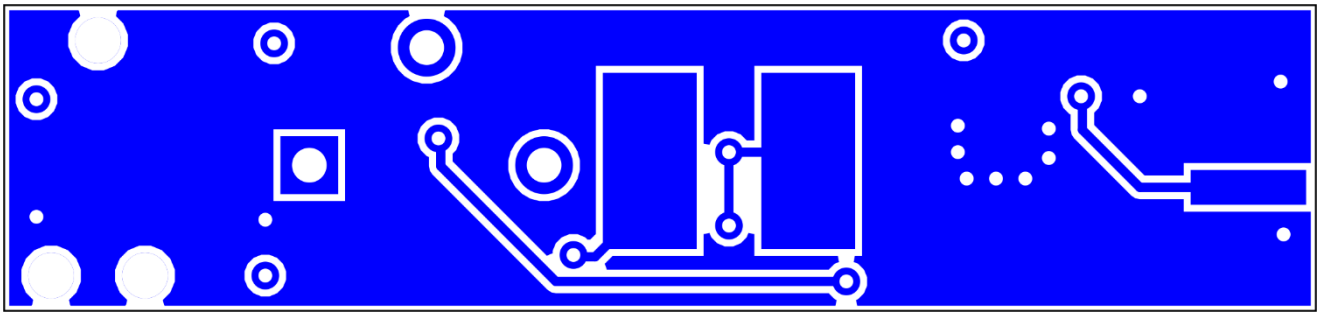


Figure 14. Reference Design 2: Base Board - BOT Layer

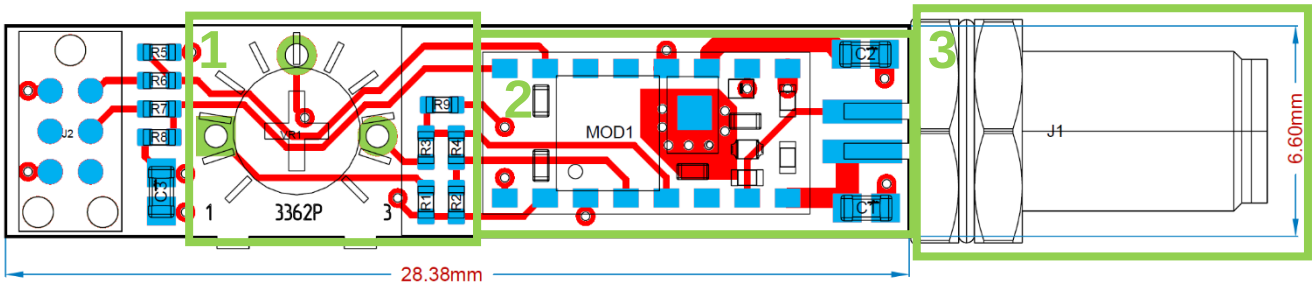


Figure 15. Reference Design 2: Base Board - Assembly View TOP

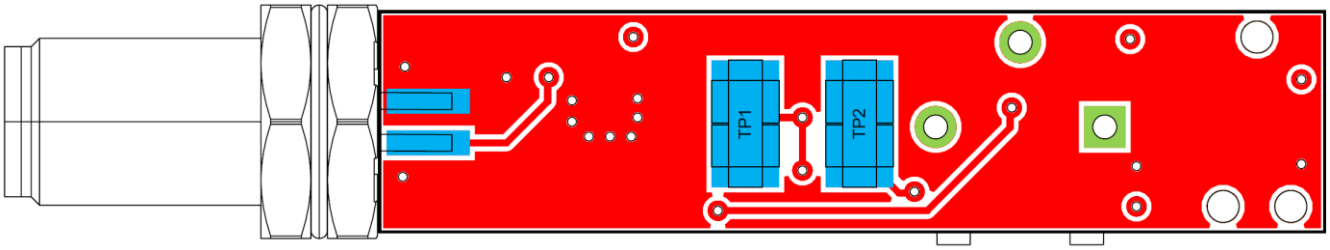


Figure 16. Reference Design 2: Base Board - Assembly View BOT

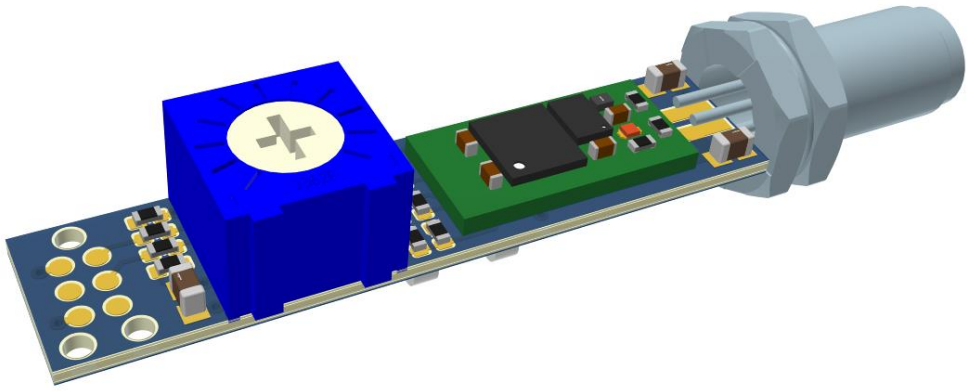


Figure 17. Reference Design 2: Base Board - 3D View

Table 4 explains the PCB stack-up for the Mini Module. Figure 18 to Figure 23 show the copper layer layouts.

Table 4. PCB stack-up Reference Design 2: Mini Module

Layer	Signals	Function	Drawing
TOP	Miscellaneous	Routing Layer 1 (primary)	Figure 18
Layer 2	GND	Reference GND plane for TOP Layer	Figure 19
Layer 3	Miscellaneous	Routing Layer 2 (primary)	Figure 20
Layer 4	Miscellaneous	Routing Layer 3 (secondary)	Figure 21
Layer 5	VDD 3.3V	Low impedance power plane	Figure 22
BOT	GND	Low impedance GND plane, LGA pads	Figure 23

The BOT layer carries LGA pads and thus works as a contact plane for the two-board PCB solution. A commercial sensor product would consist of a single PCB solution with a continuous GND plane without the need for LGA pads. Similarly, the test pads on the TOP layer are not needed.

The WLCSPs with high density BGA (0.4mm pitch) require via-in-pad technology. Thus, all vias are filled and capped, though showed as holes in the layer views.

Layout and component placement (also refer Figure 24) is oriented at keeping high voltage signals on the right side of the board, whereas digital interfaces are routed out on top left side and analog signals to the bottom left side.

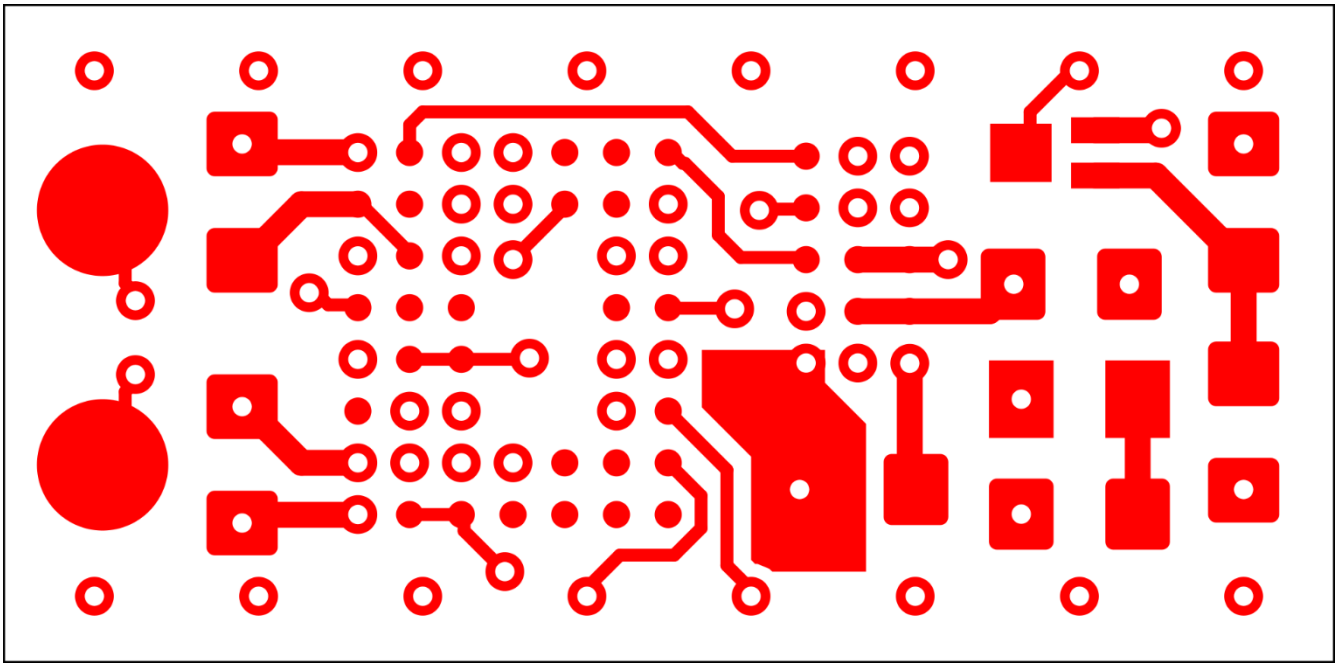


Figure 18. Reference Design 2: Mini Module - TOP Layer

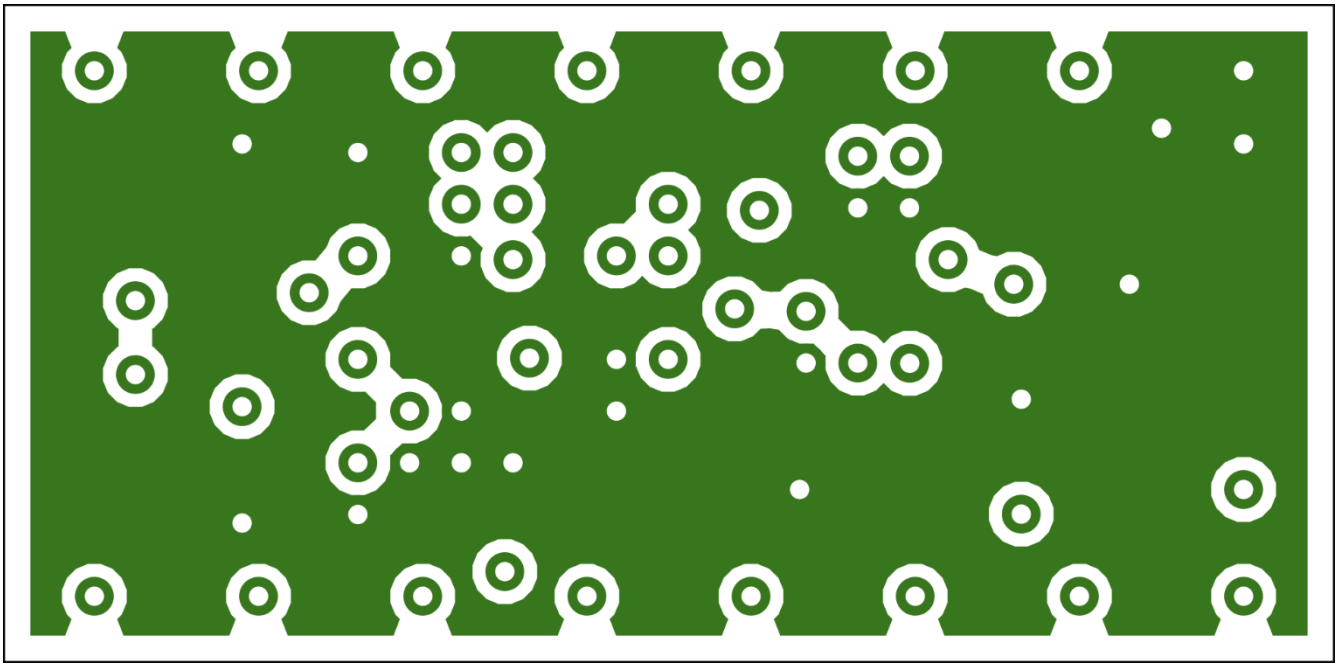


Figure 19. Reference Design 2: Mini Module - Layer 2

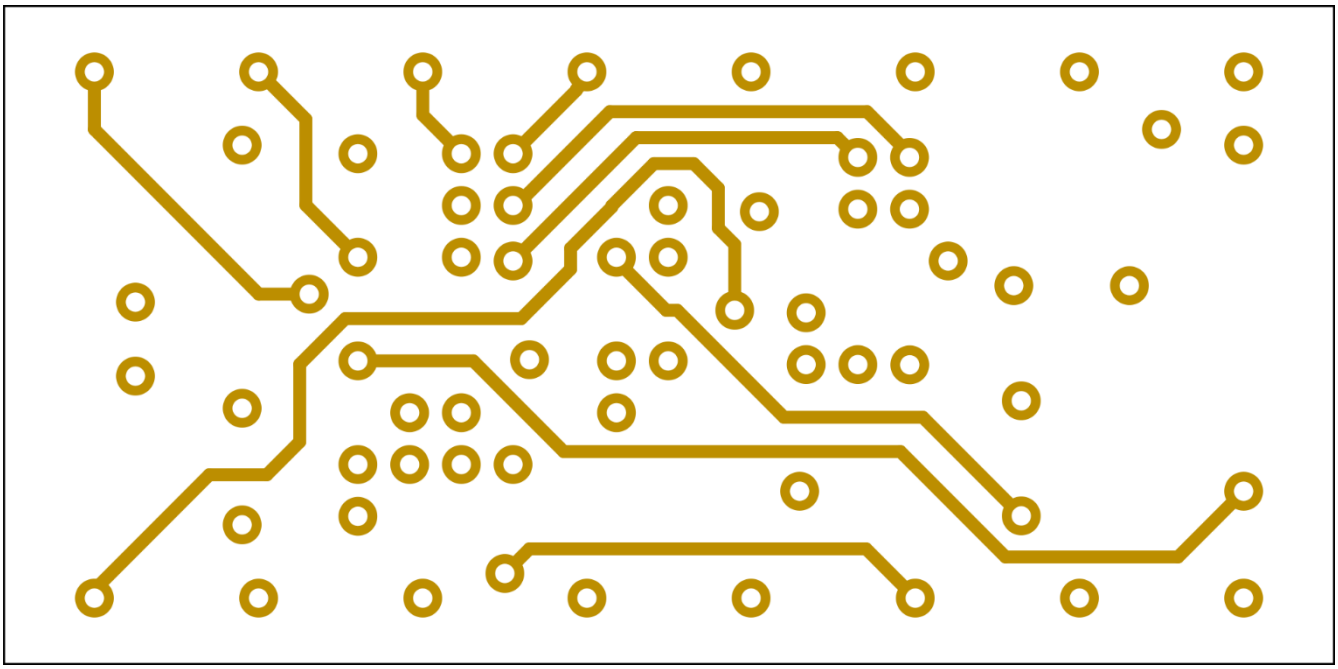


Figure 20. Reference Design 2: Mini Module - Layer 3

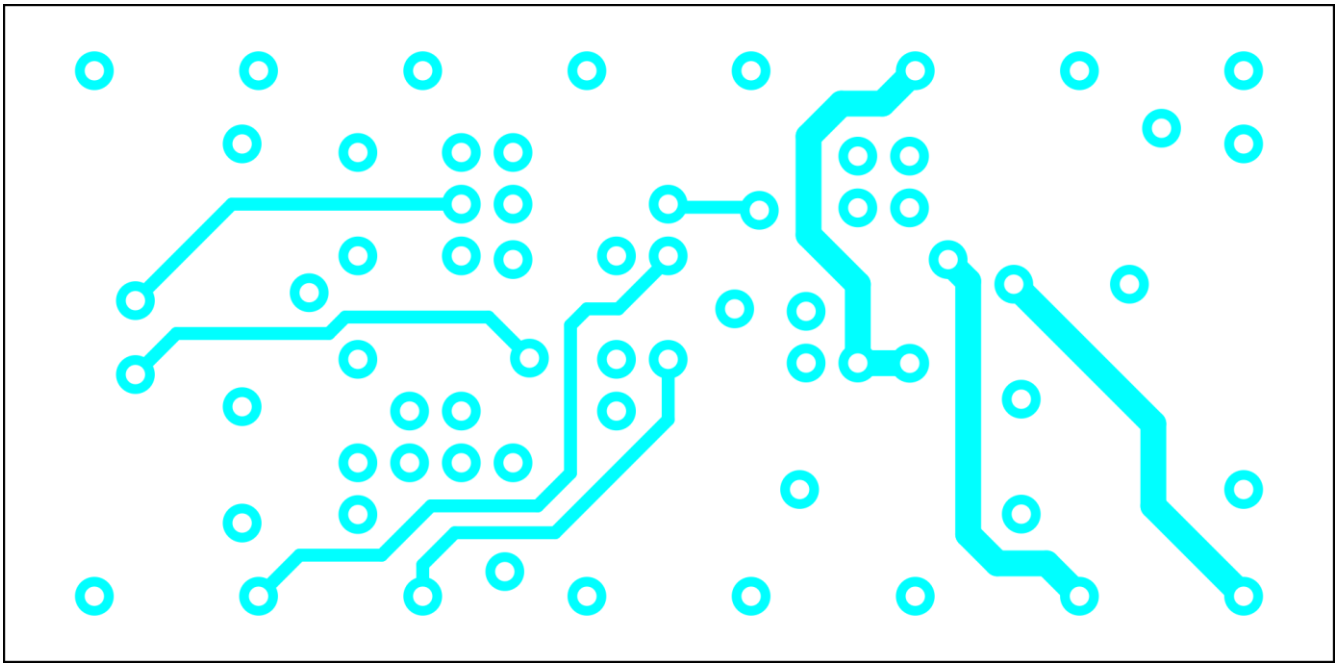


Figure 21. Reference Design 2: Mini Module - Layer 4

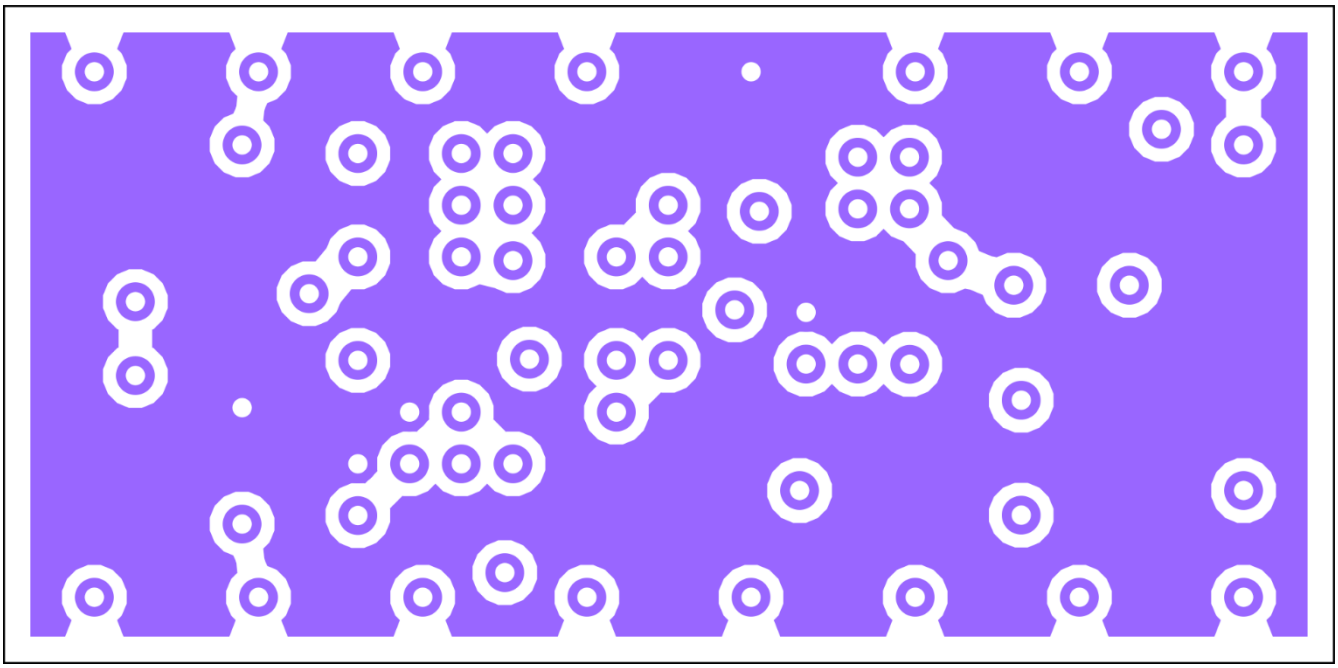


Figure 22. Reference Design 2: Mini Module - Layer 5

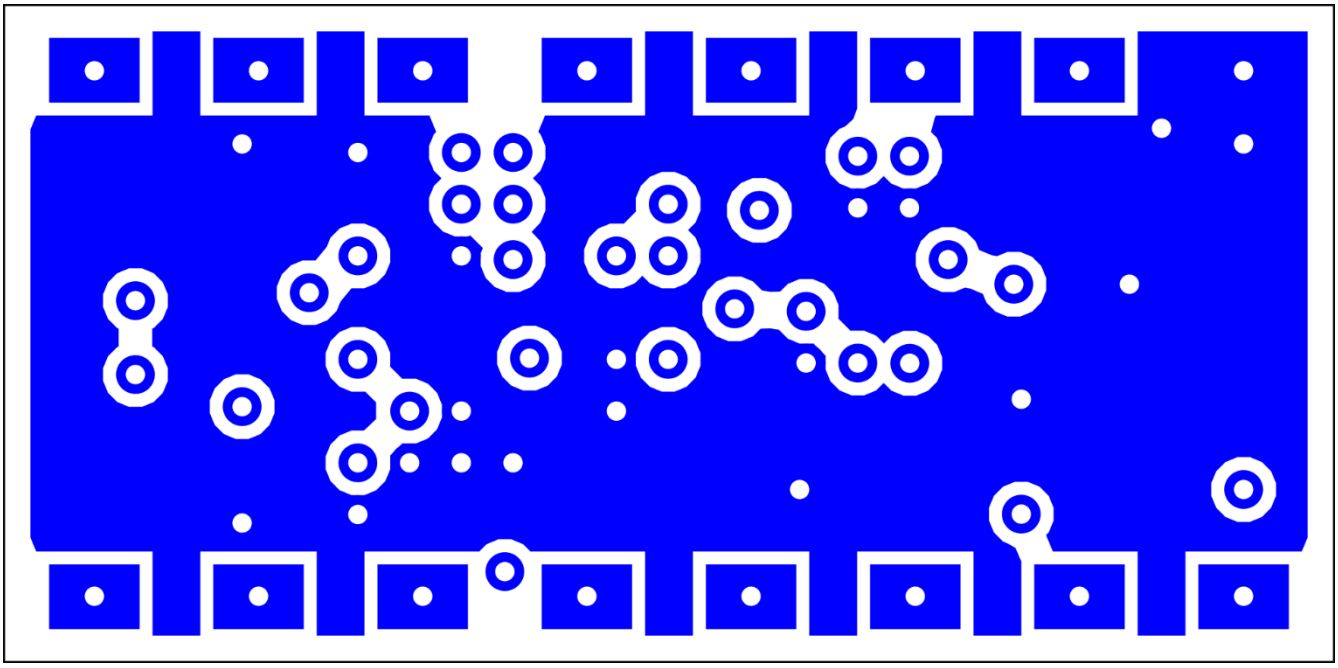


Figure 23. Reference Design 2: Mini Module - BOT Layer

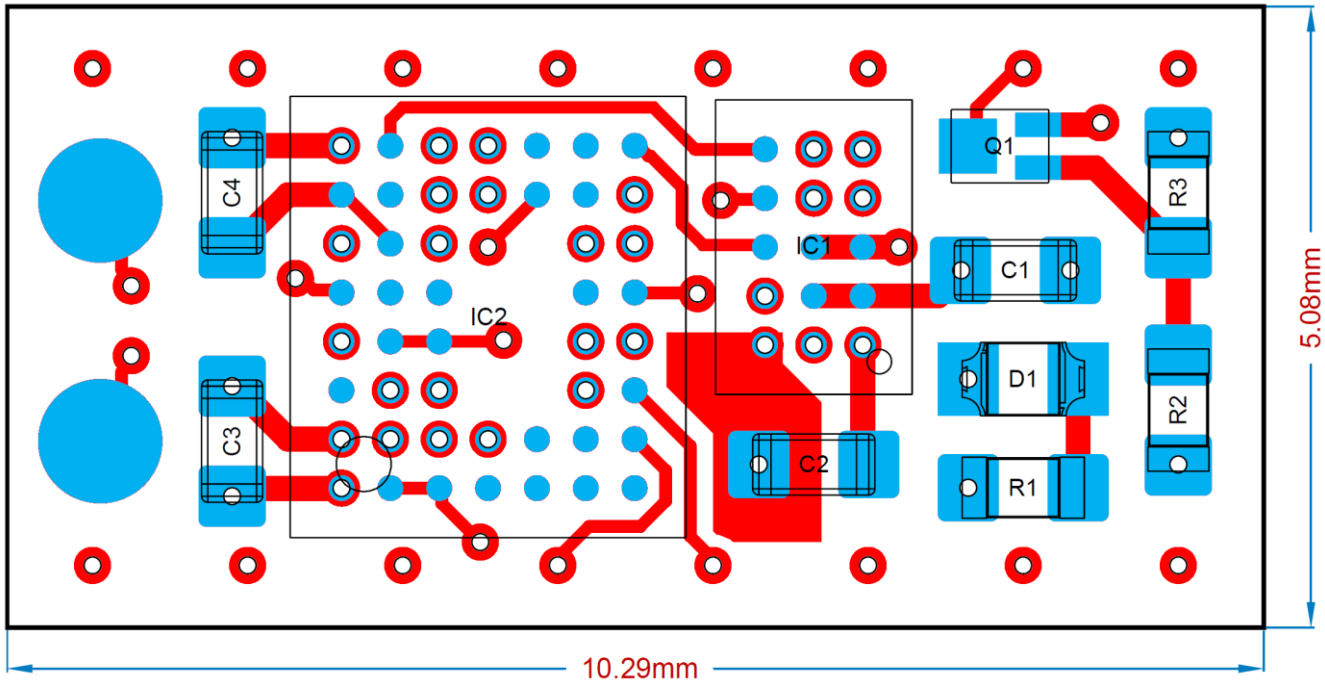


Figure 24. Reference Design 2: Mini Module - Assembly View TOP

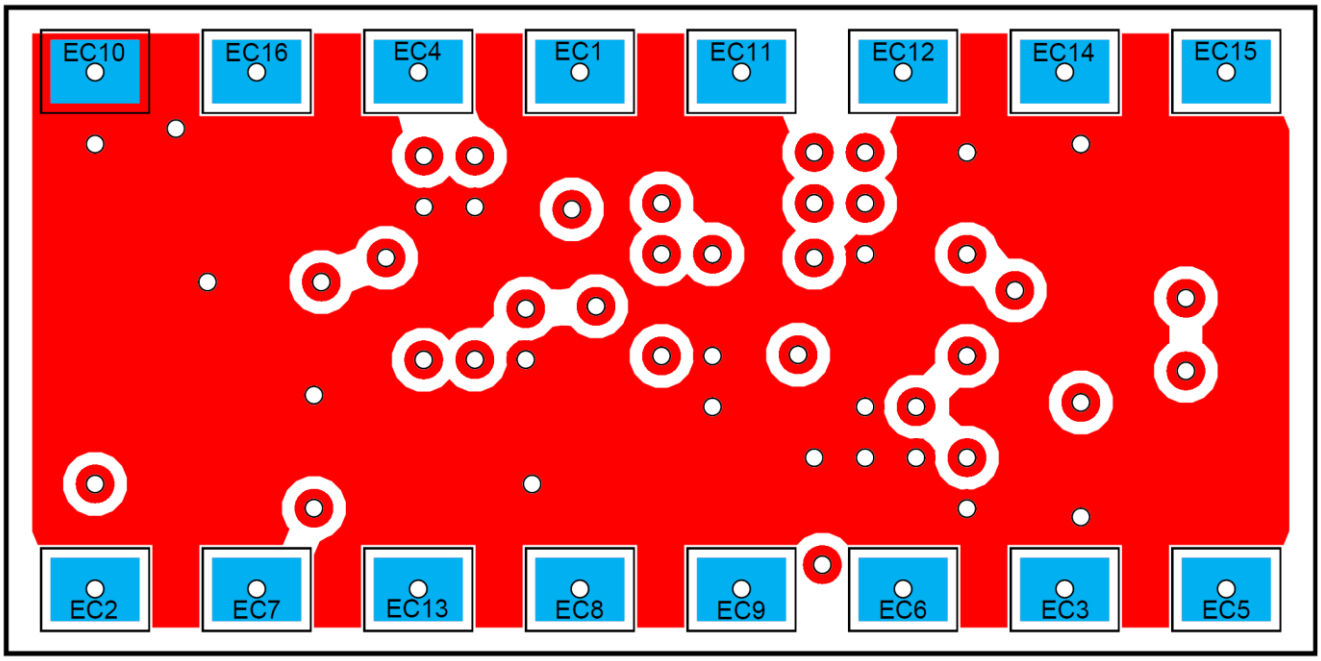


Figure 25. Reference Design 2: Mini Module - Assembly View BOT

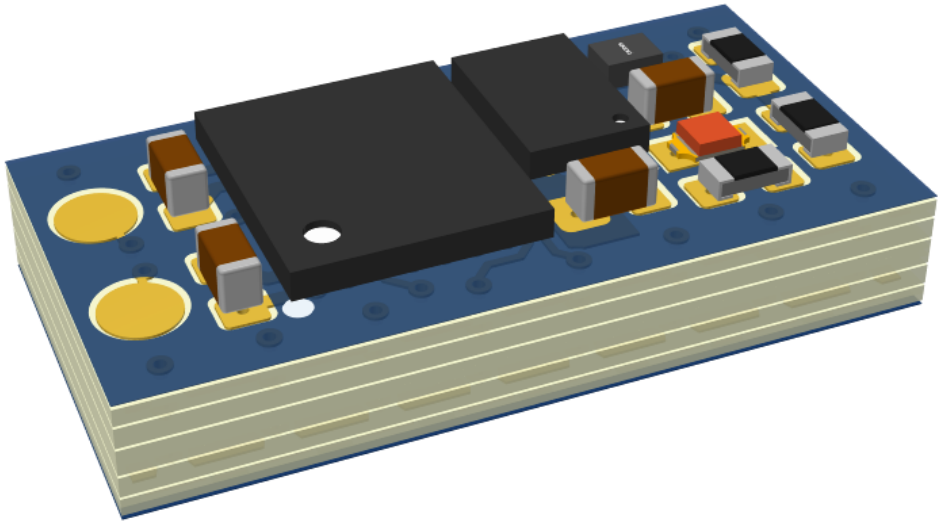


Figure 26. Reference Design 2: Mini Module - 3D View

3. References

Reference Number	Title
1	ZSSC3286 Datasheet available at: https://www.renesas.com/ZSSC3286
2	RH4Z2501 Datasheet available at: https://www.renesas.com/RH4Z2501
3	ZSSC324x Electromagnetic Compatibility Technical Note available at: https://www.renesas.com/en/document/tcb/zssc324x-electromagnetic-compatibility

4. Glossary

Term	Description
AOUT	Analog Output
BGA	Ball Grid Array
BOT	Bottom PCB Layer
C/Q	C/Q line of IO-Link interface. Connection for communication (C) or switching (Q) signal.
DFN	Dual-Flat No-Leads
EP	Exposed Pad
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
GND	Ground
GPIO	General Purpose Input/Output
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
LED	Light Emitting Diode
LGA	Land Grid Array
misc.	miscellaneous
OWI	One Wire Interface
PCB	Printed Circuit Board
PHY	Physical Layer
QFN	Quad-Flat No-Leads
TOP	Top PCB Layer
TVS	Transient Voltage Surpressor
WLCSP	Wafer Level Chip Scale Package

5. Revision History

Revision	Date	Description
1.0	Apr.15.24	Initial release.