Interface IP

USB2.0 FS Transceiver

Overview

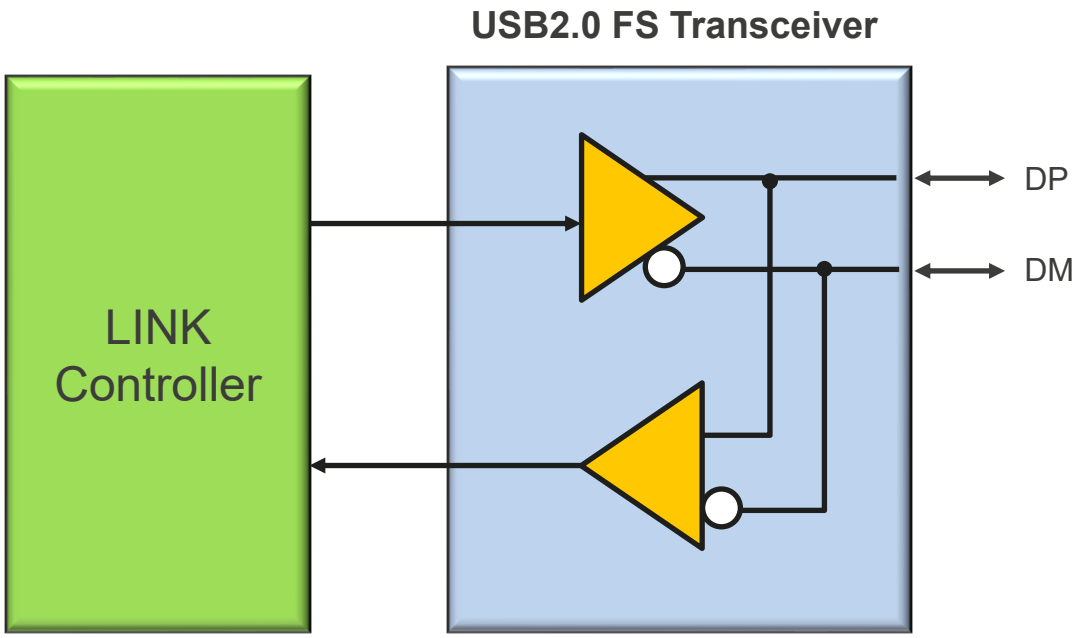
The Renesas USB2.0 FS Transceiver is useful analog 1port transceiver hard macro for TSMC 40nm LP process. This macro can be configured to operate as a USB2.0 Full/Low Speed peripheral or host controller.

For this IP, only the parts required for FullSpeed(FS:12Mbps) and LowSpeed(LS:1.5Mbps) are cut out from the USB2.0 PHY IP.
When HighSpeed(HS:480Mbps) is not required, we can provide the optimum solution in terms of area and power consumption.

Key Features

- Renesas USB2.0 FS Transceiver can be used for analog transceiver of following interface .
  - Universal Serial Bus Specification Revision 2.0 Full/Low Speed
- Technology is TSMC 40nm LP 1p6M.
- Supply voltage can be applied 1.1V for core voltage and 3.3V for IO voltage.
- USB transfer mode is full-speed (12 Mbps), and low-speed (1.5 Mbps) modes.
- A terminal resistance, pull-up resistor, and pull-down resistor are included.

Block Diagram



CTPD-24-119
R06PF0011EJ0101

2024.09