To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS FIELD EFFECT TRANSISTOR

Phase-out/Discontinued

2SJ448

SWITCHING
P-CHANNEL POWER MOS FET

DESCRIPTION

The 2SJ448 is P-channel MOS Field Effect Transistor designed for high voltage switching applications.

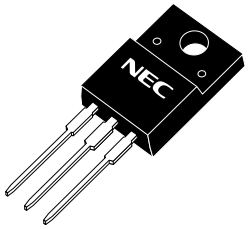
ORDERING INFORMATION

PART NUMBER	PACKAGE
2SJ448	Isolated TO-220

FEATURES

- 250 V rating high withstand voltage
- Low on-state resistance:
  $R_{DS(on)}$ = 2.0 Ω MAX. (V_{GS} = –10 V, I_D = –2.0 A)
- Low input capacitance:
  C_{iss} = 470 pF TYP.
- Narrow gate cut-off voltage width:
  $V_{GS(off)}$ = –5.5 to –4.0 V
- Built-in gate protection diode
- Full-mold package for easy mounting

★ (Isolated TO-220)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

	Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	–250	V
★	Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	∓30	V
	Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	∓4.0	A
	Drain Current (pulse) Note1	$I_{D(pulse)}$	∓16	A
	Total Power Dissipation (T_C = 25°C)	P_{T1}	30	W
	Total Power Dissipation (T_A = 25°C)	P_{T2}	2.0	W
	Channel Temperature	T_{ch}	150	°C
	Storage Temperature	T_{stg}	–55 to +150	°C
	Single Avalanche Current Note2	I_{AS}	–4.0	A
	Single Avalanche Energy Note2	E_{AS}	80	mJ

Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = –125 V, R_G = 25 Ω, V_{GS} = –20 → 0 V

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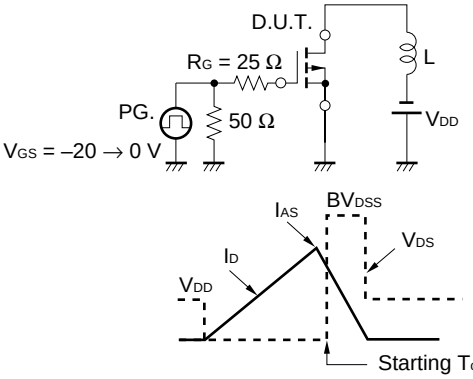
Printed in Japan

The mark ★ shows major revised points.

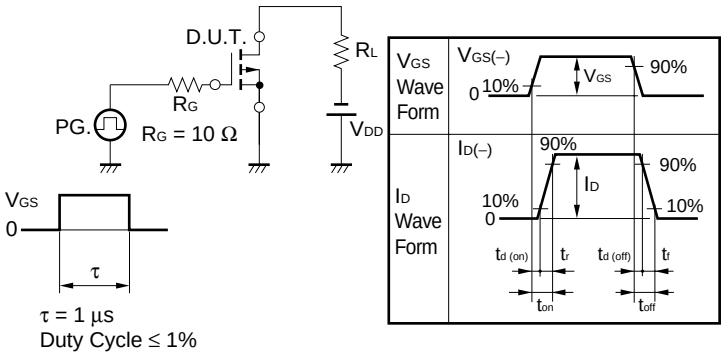
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –250 V, V_{GS} = 0 V			–100	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓25 V, V_{DS} = 0 V			∓10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–4.0	–4.8	–5.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = –10 V, I_D = –2.0 A	1.0	2.3		S
Drain to Source On-state Resistance	$R_{DS(on)}$	V_{GS} = –10 V, I_D = –2.0 A		1.5	2.0	Ω
Input Capacitance	C_{iss}	V_{DS} = –10 V		470		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		200		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		70		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –125 V, I_D = –2.0 A		13		ns
Rise Time	t_r	V_{GS} = –10 V		7		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		34		ns
Fall Time	t_f			10		ns
Total Gate Charge	Q_G	V_{DD}= –200 V		15		nC
Gate to Source Charge	Q_{GS}	V_{GS} = –10 V		4		nC
Gate to Drain Charge	Q_{GD}	I_D = –4.0 A		9		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 4.0 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 4.0 A, V_{GS} = 0 V		195		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 50 A/μs		760		nC

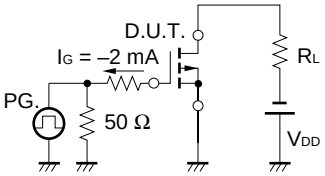
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

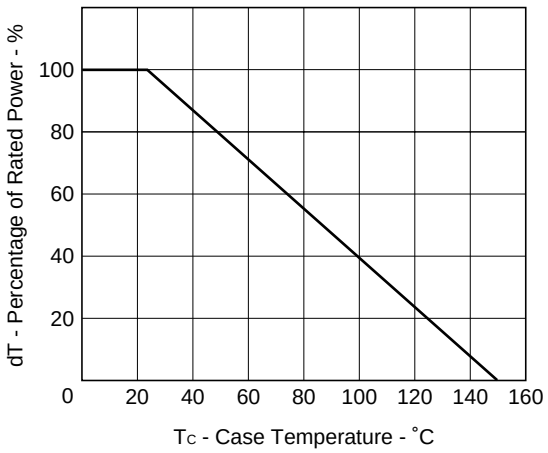


TEST CIRCUIT 3 GATE CHARGE

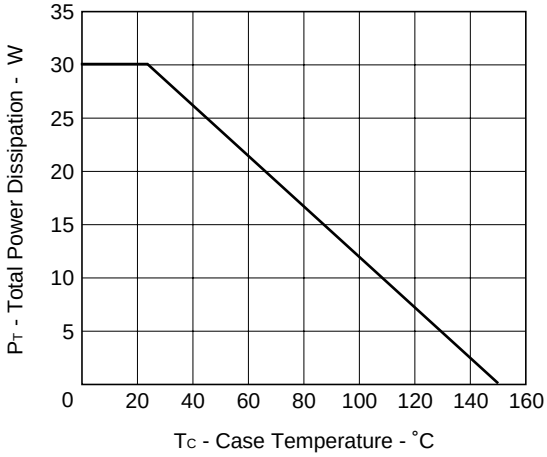


TYPICAL CHARACTERISTICS (T_A = 25°C)

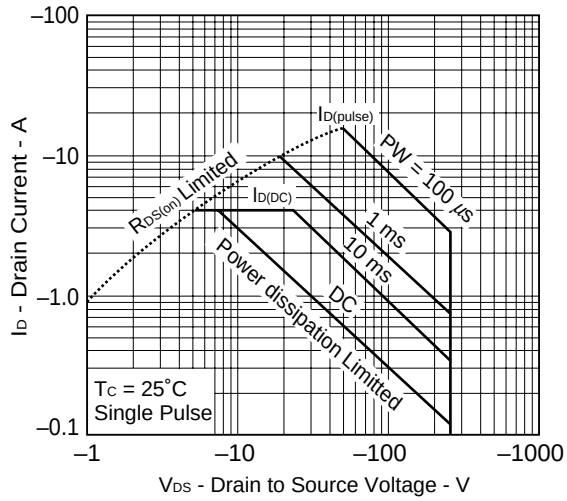
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



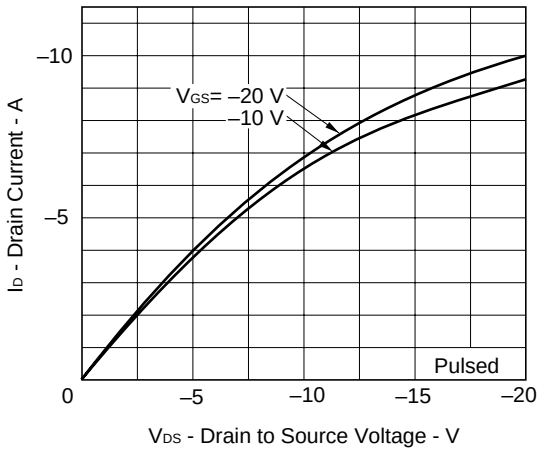
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



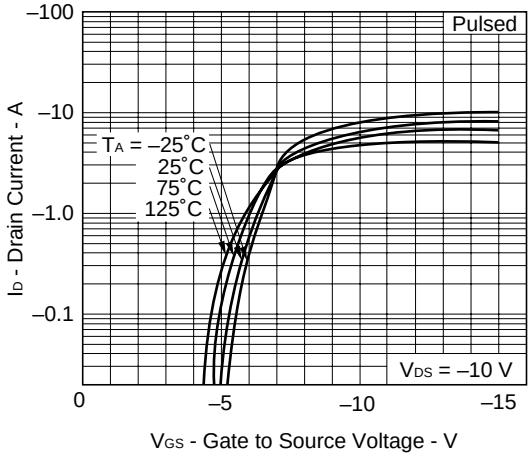
FORWARD BIAS SAFE OPERATING AREA



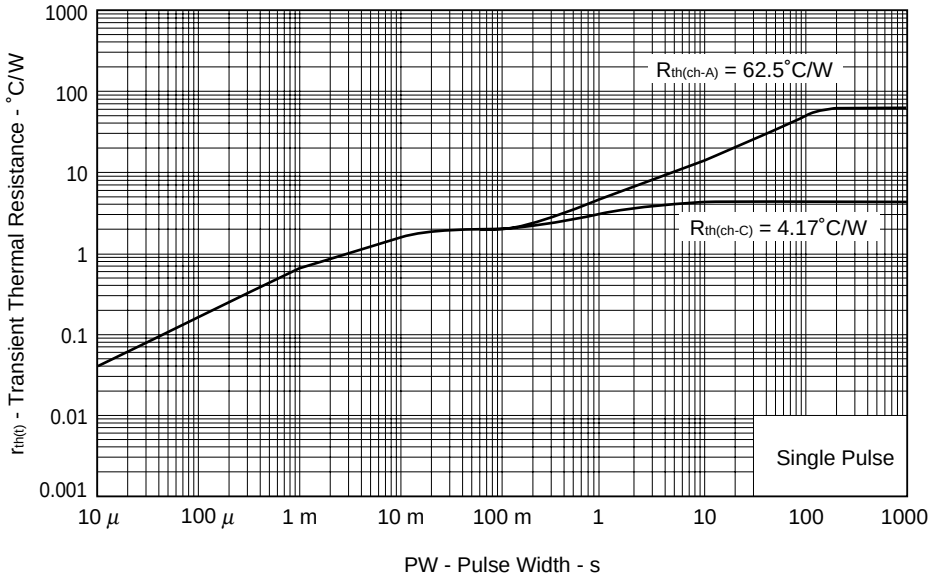
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



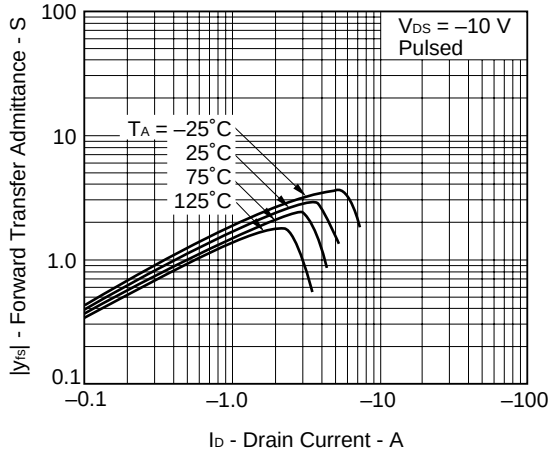
FORWARD TRANSFER CHARACTERISTICS



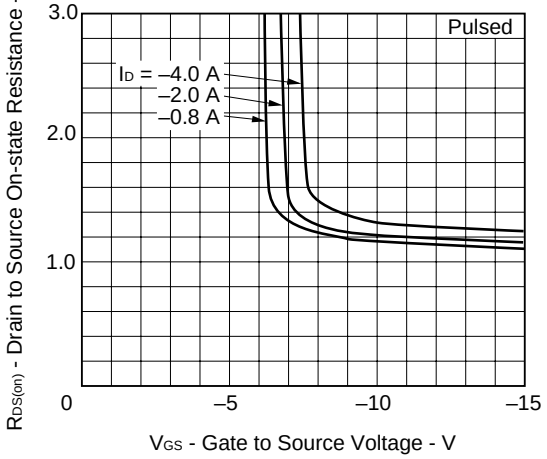
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



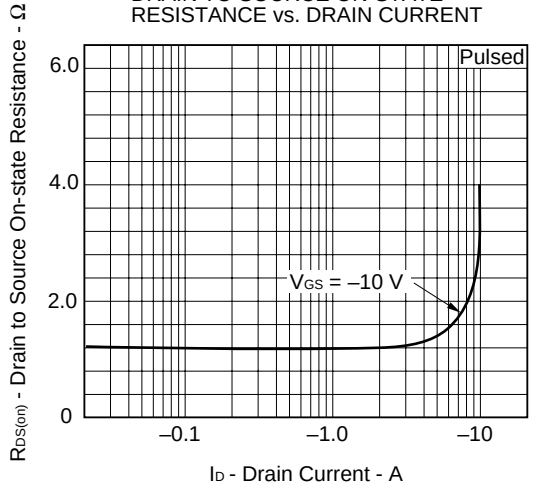
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



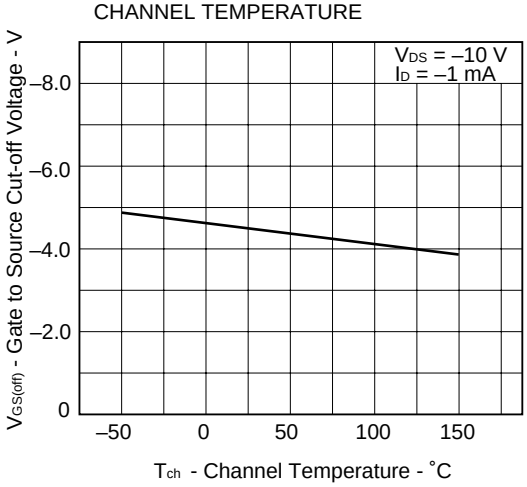
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



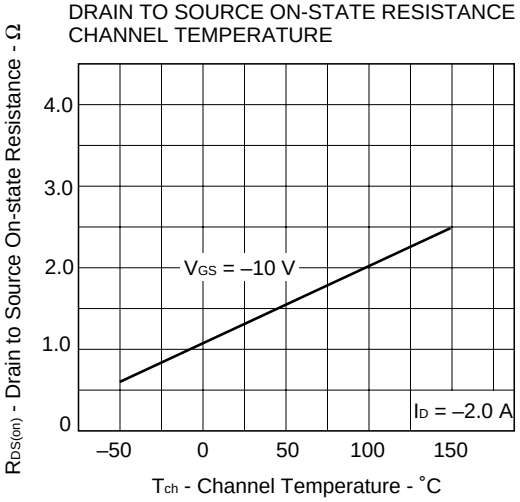
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



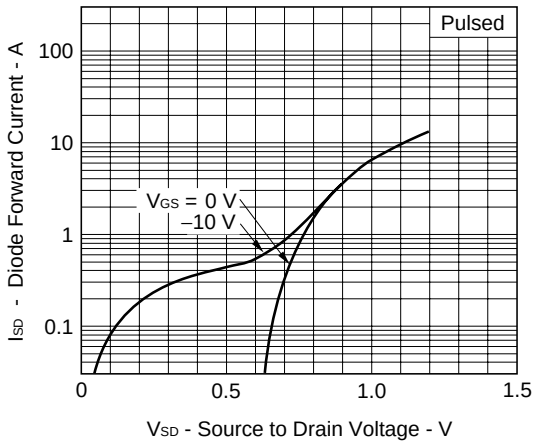
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



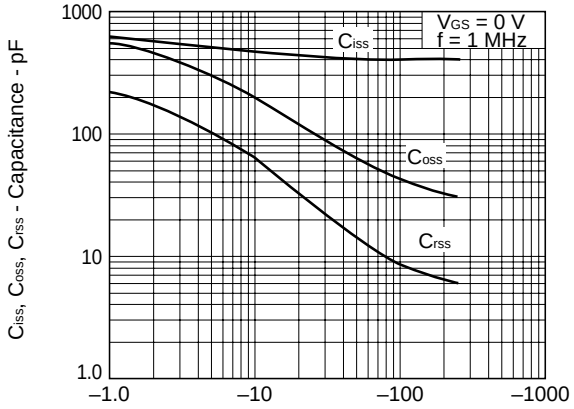
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



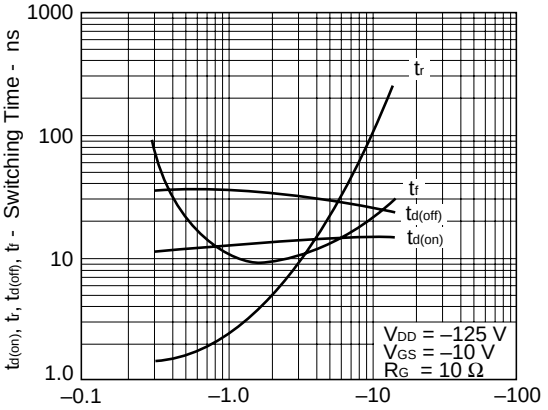
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



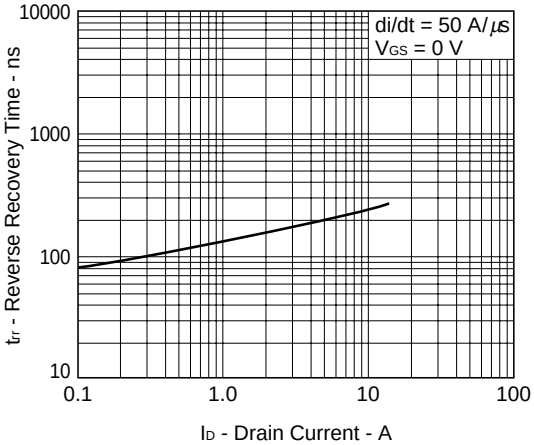
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



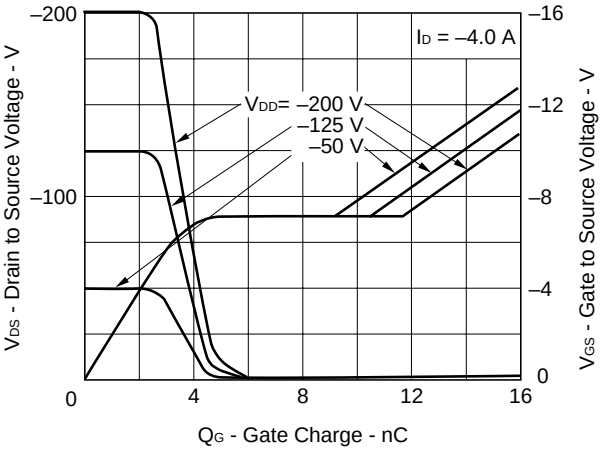
SWITCHING CHARACTERISTICS



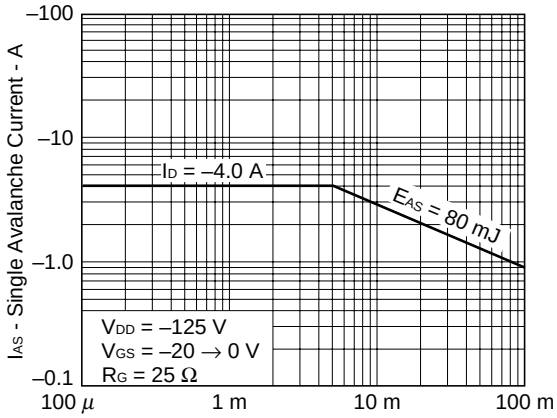
REVERSE RECOVERY TIME vs. DRAIN CURRENT



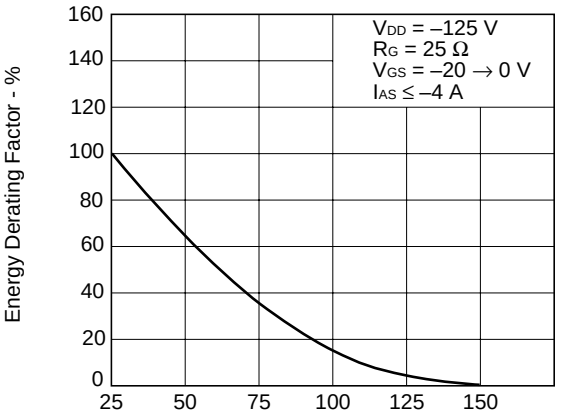
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD

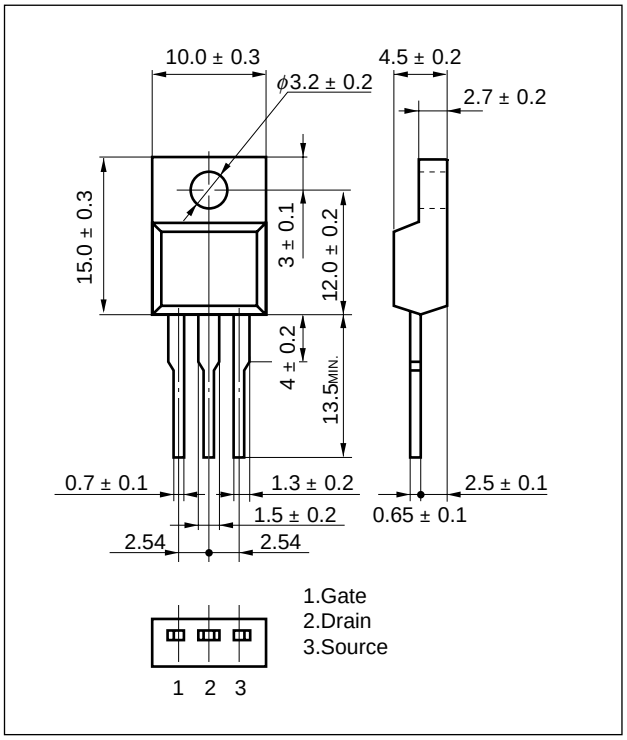


SINGLE AVALANCHE ENERGY
DERATING FACTOR

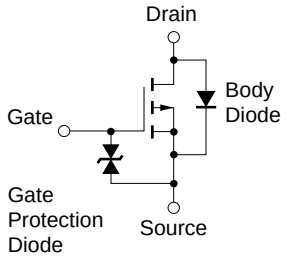


PACKAGE DRAWING (Unit: mm)

Isolated TO-220(MP-45F)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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