

To our customers,

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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2SJ484

Silicon P Channel MOS FET

REJ03G0868-0300
(Previous: ADE-208-501A)
Rev.3.00
Sep 07, 2005

Description

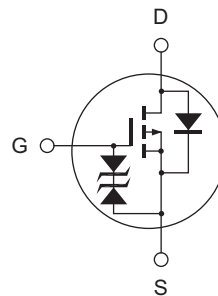
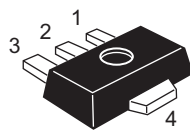
High speed power switching

Features

- Low on-resistance
 $R_{DS(on)} = 0.18 \Omega$ typ. (at $V_{GS} = -10 \text{ V}$, $I_D = -1 \text{ A}$)
- Low drive current
- High speed switching
- 4 V gate drive devices.

Outline

RENESAS Package code: PLZZ0004CA-A
(Package name: UPAK®)



1. Gate
2. Drain
3. Source
4. Drain

Note: Marking is "WY".

*UPAK is a trademark of Renesas Technology Corp.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V _{DSS}	-30	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	-2	A
Drain peak current	I _{D (pulse)} ^{Note 1}	-4	A
Body to drain diode reverse drain current	I _{DR}	-2	A
Channel dissipation	P _{ch} ^{Note 2}	1	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

Notes: 1. PW ≤ 100 μs, duty cycle ≤ 10%

2. When using the aluminium ceramic board (12.5 × 20 × 0.7 mm)

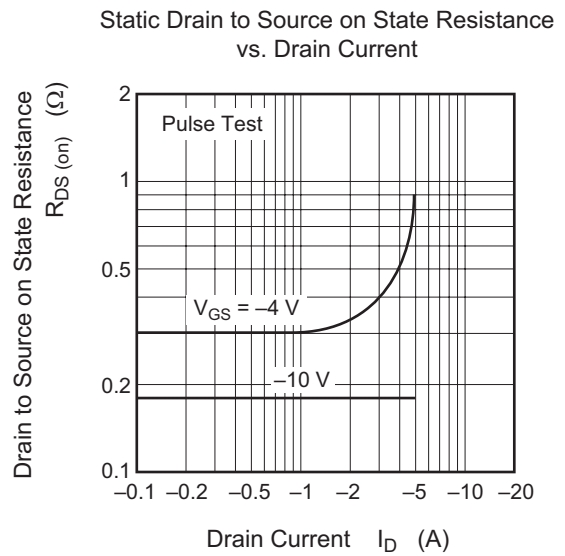
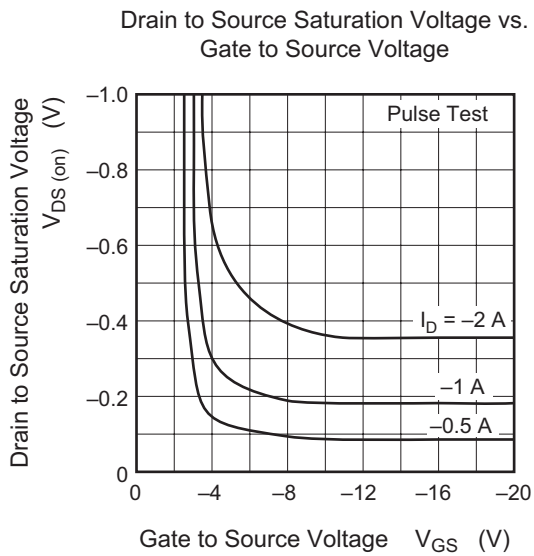
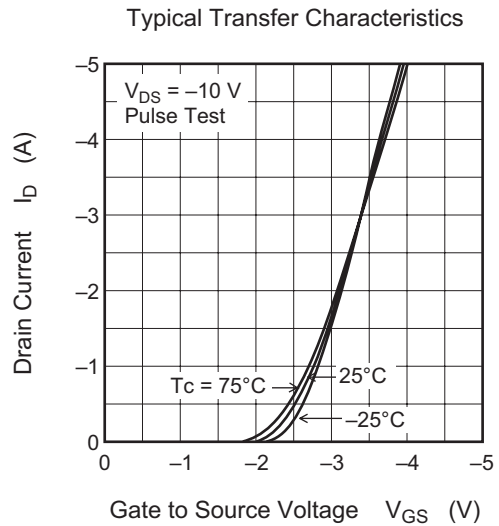
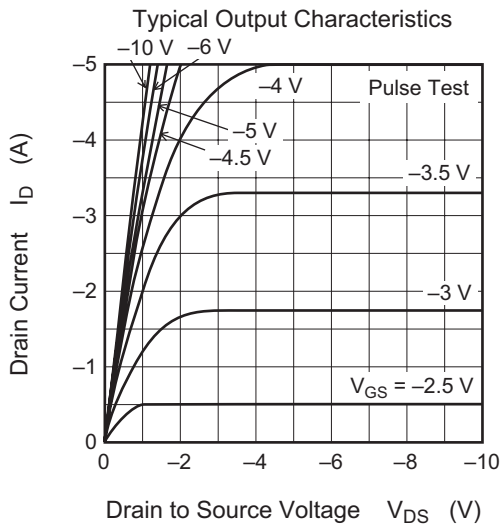
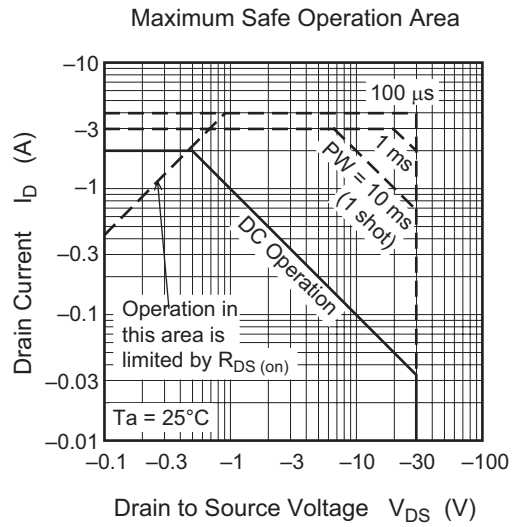
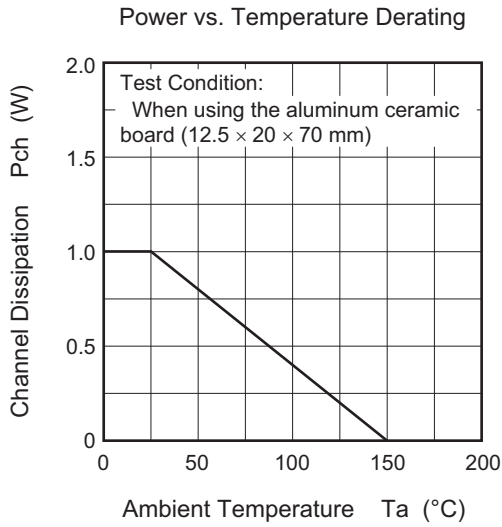
Electrical Characteristics

(Ta = 25°C)

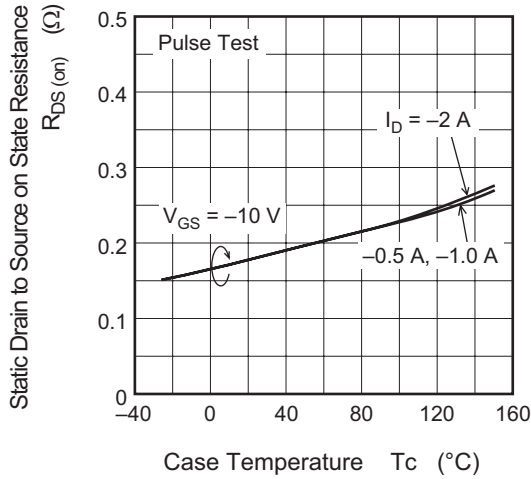
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR) DSS}	-30	—	—	V	I _D = -10 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR) GSS}	±20	—	—	V	I _G = ±100 μA, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	-10	μA	V _{DS} = -30 V, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	±10	μA	V _{GS} = ±16 V, V _{DS} = 0
Gate to source cutoff voltage	V _{GS (off)}	-1.0	—	-2.0	V	I _D = -1 mA, V _{DS} = -10 V
Static drain to source on state resistance	R _{DS (on)}	—	0.18	0.23	Ω	I _D = -1 A, V _{GS} = -10 V ^{Note 3}
	R _{DS (on)}	—	0.3	0.45	Ω	I _D = -1 A, V _{GS} = -4 V ^{Note 3}
Forward transfer admittance	y _{fs}	1.2	2.0	—	S	I _D = -1 A, V _{DS} = -10 V ^{Note 3}
Input capacitance	C _{iss}	—	230	—	pF	V _{DS} = -10 V
Output capacitance	C _{oss}	—	140	—	pF	V _{GS} = 0
Reverse transfer capacitance	C _{rss}	—	50	—	pF	f = 1 MHz
Turn-on delay time	t _{d (on)}	—	10	—	ns	V _{GS} = -10 V
Rise time	t _r	—	30	—	ns	I _D = -1 A
Turn-off delay time	t _{d (off)}	—	35	—	ns	R _L = 30 Ω
Fall time	t _f	—	30	—	ns	
Body to drain diode forward voltage	V _{DF}	—	-0.95	—	V	I _F = -2 A, V _{GS} = 0
Body to drain diode reverse recovery time	t _{rr}	—	60	—	ns	I _F = -2 A, V _{GS} = 0 di _F /dt = 50 A/μs

Note: 3. Pulse test

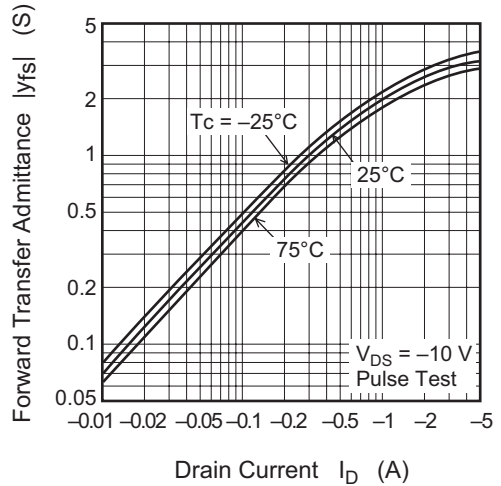
Main Characteristics



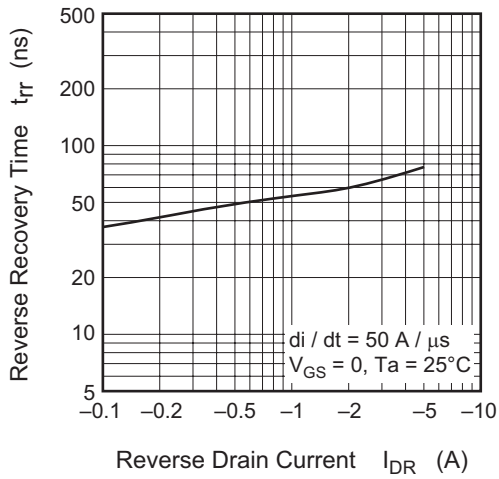
Static Drain to Source on State Resistance vs. Temperature



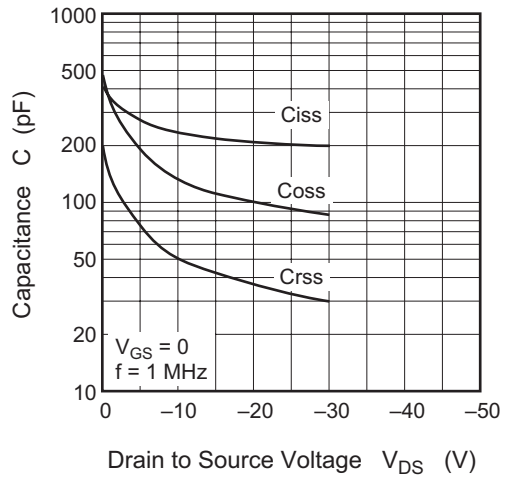
Forward Transfer Admittance vs. Drain Current



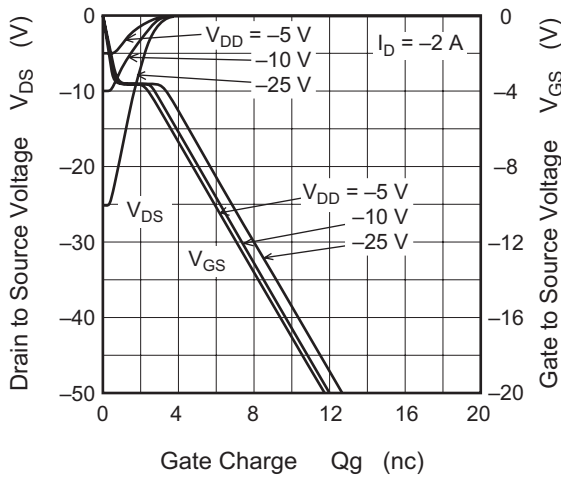
Body-Drain Diode Reverse Recovery Time



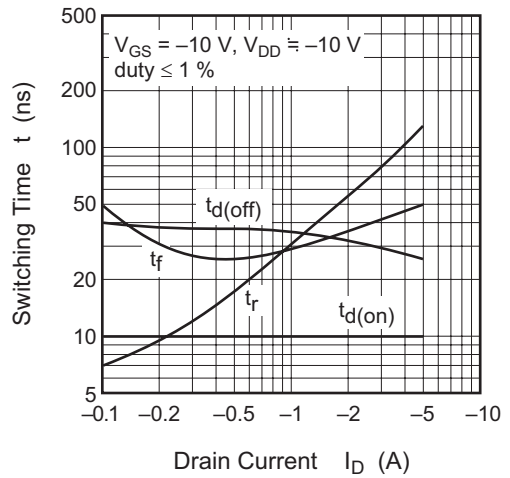
Typical Capacitance vs. Drain to Source Voltage



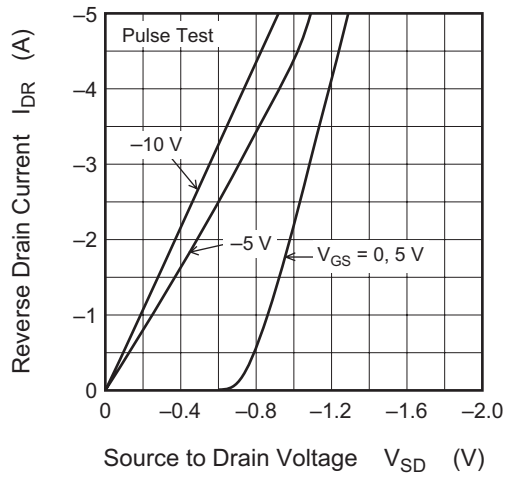
Dynamic Input Characteristics



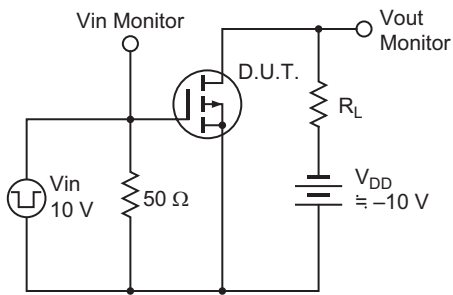
Switching Characteristics



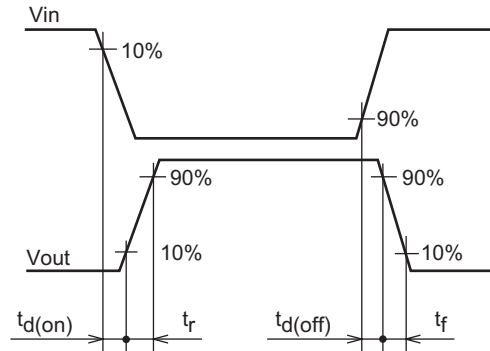
Reverse Drain Current vs. Source to Drain Voltage



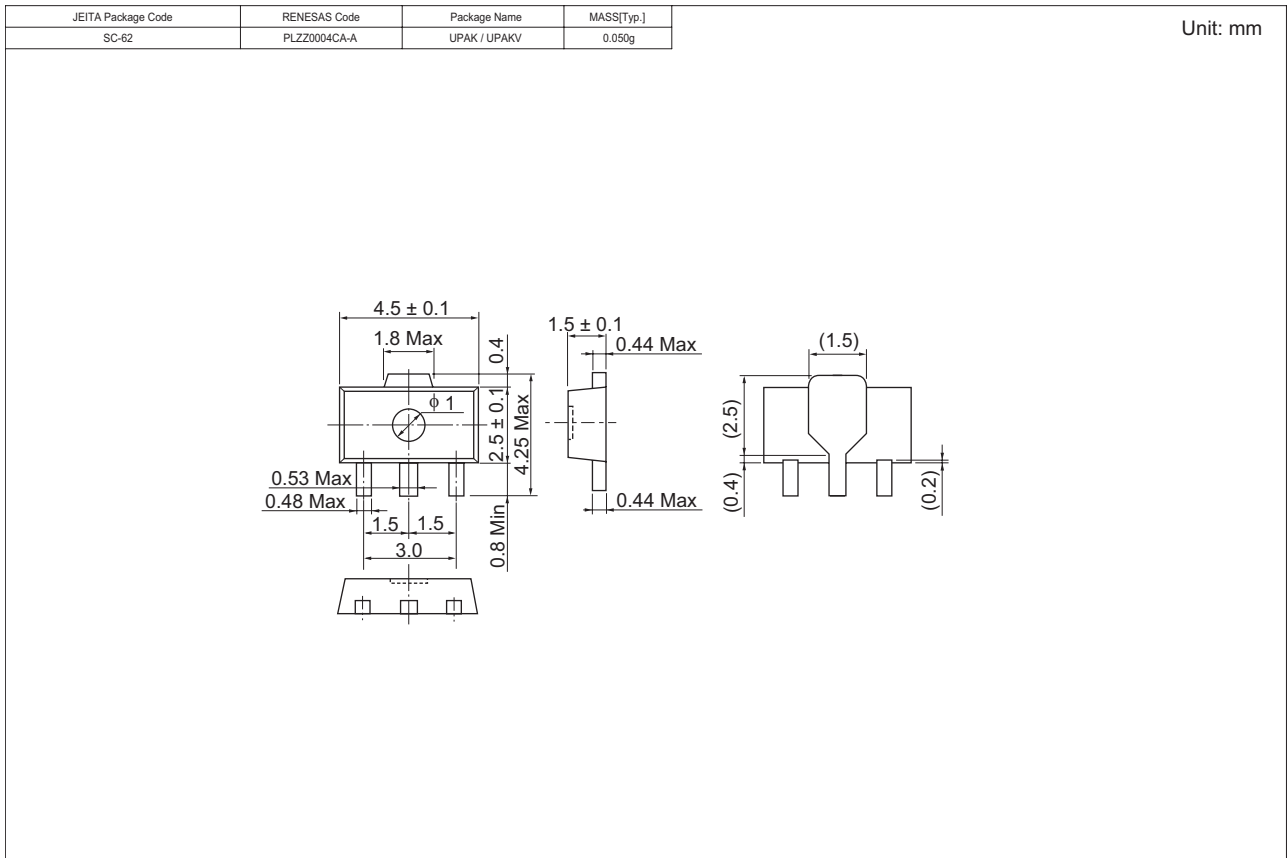
Switching Time Test Circuit



Waveform



Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
2SJ484WYTL-E	1000 pcs	Taping
2SJ484WYTR-E	1000 pcs	Taping

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