2SJ574

Silicon P Channel MOS FET
High Speed Switching

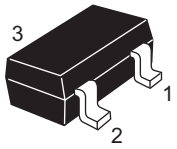
R07DS0574EJ0500
Rev.5.00
Jan 10, 2014

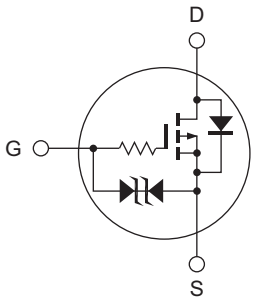
Features

- Low on-resistance
  R_{DS} = 1.1 Ω typ. (V_{GS} = –10 V, I_D = –150 mA)
  R_{DS} = 2.2 Ω typ. (V_{GS} = –4 V, I_D = –150 mA)
- 4 V gate drive device.
- Small package (MPAK)

Outline

RENESAS Package code: PLSP0003ZB-A
(Package name: MPAK)





1. Source
2. Gate
3. Drain

Note: Marking is BP

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–300	mA
Drain peak current	$I_{D(pulse)}$ Note1	–1.2	A
Body-drain diode reverse drain current	I_{DR}	–300	mA
Channel dissipation	Pch Note 2	400	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Value on the alumina ceramic board (12.5 x 20 x 0.7mm)

Electrical Characteristics

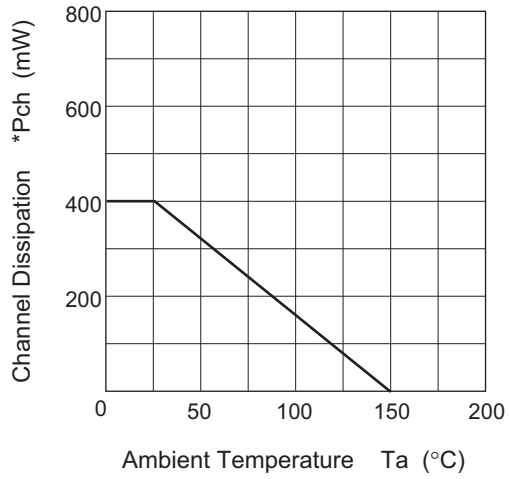
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –100 µA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–1	µA	V_{DS} = –30 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±5	µA	V_{GS} = ±16 V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.3	—	–2.3	V	I_D = –10 µA, V_{DS} = –5 V
Static drain to source on state resistance	$R_{DS(on)}$	—	1.1	1.3	Ω	I_D = –150 mA, V_{GS} = –10 V Note 3
	$R_{DS(on)}$	—	2.2	3.1	Ω	I_D = –150 mA, V_{GS} = –4 V Note 3
Forward transfer admittance	$\|y_{fs}\|$	195	300	—	mS	I_D = –150 mA, V_{DS} = –10 V Note 3
Input capacitance	Ciss	—	50	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	40	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	15	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	I_D = –150 mA, V_{GS} = –10 V
Rise time	t_r	—	50	—	ns	R_L = 66.6 Ω
Turn-off delay time	$t_{d(off)}$	—	110	—	ns	
Fall time	t_f	—	105	—	ns	

Note: 3. Pulse test

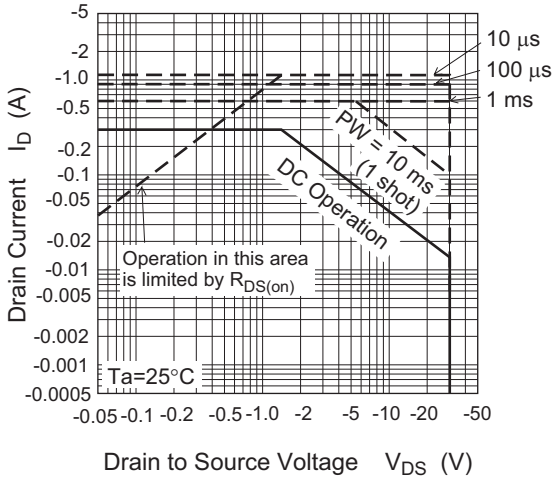
Main Characteristics

Power vs. Temperature Derating



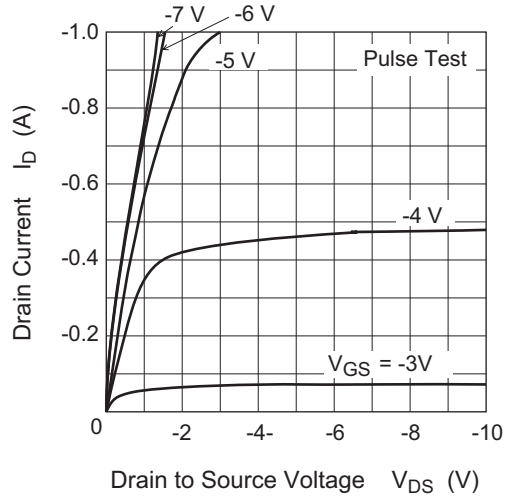
*Value on the alumina ceramic board.(12.5x20x0.7mm)

Maximum Safe Operation Area

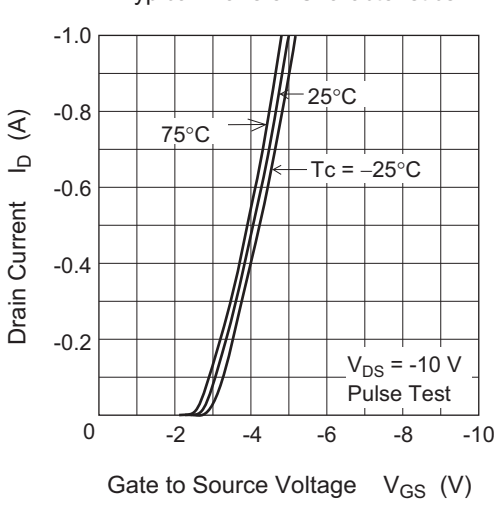


Value on the alumina ceramic board.(12.5x20x0.7mm)

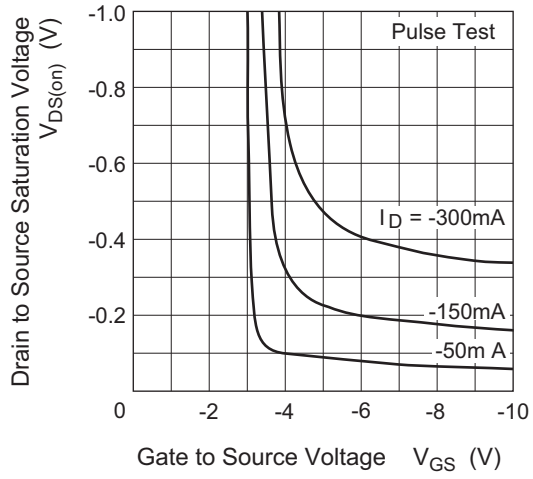
Typical Output Characteristics



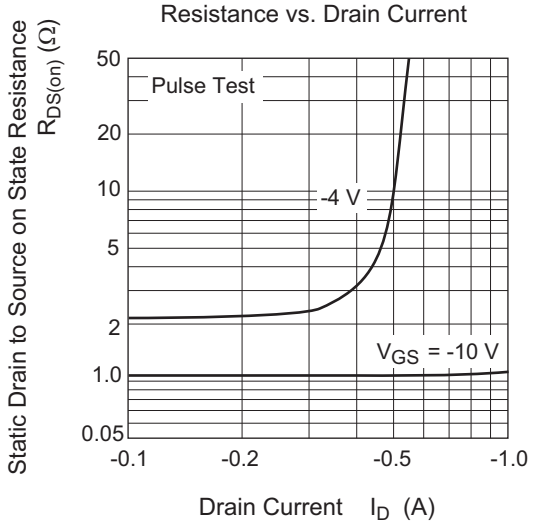
Typical Transfer Characteristics



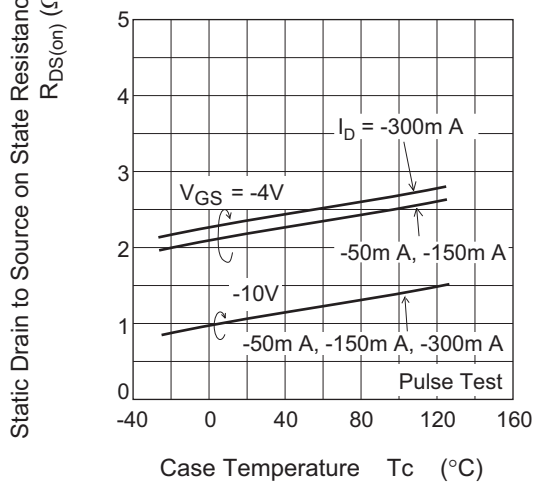
Drain to Source Saturation Voltage vs. Gate to Source Voltage



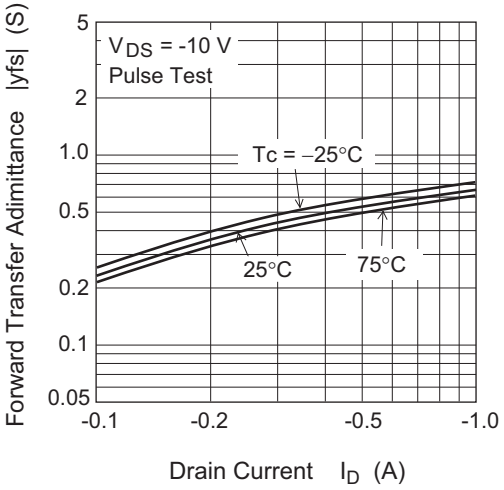
Static Drain to Source on State Resistance vs. Drain Current



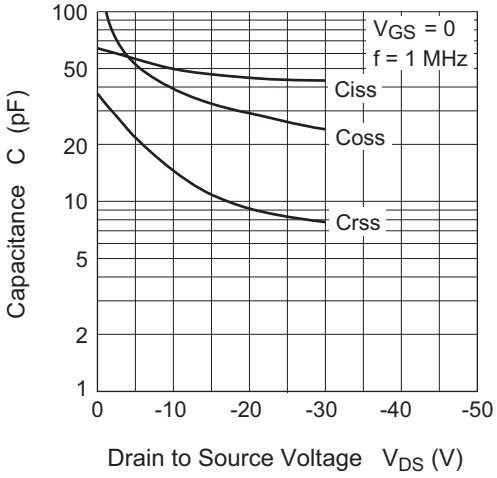
Static Drain to Source on State Resistance vs. Temperature



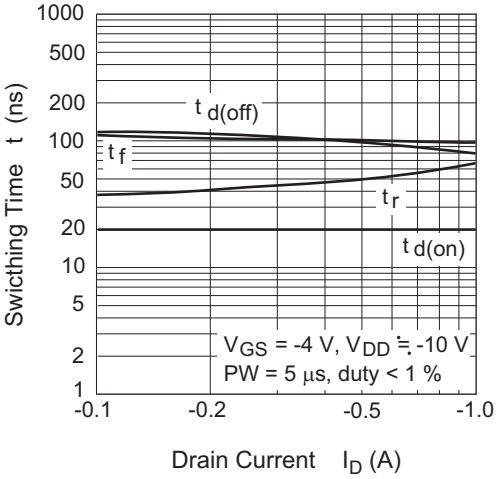
Forward Transfer Admittance vs. Drain Current



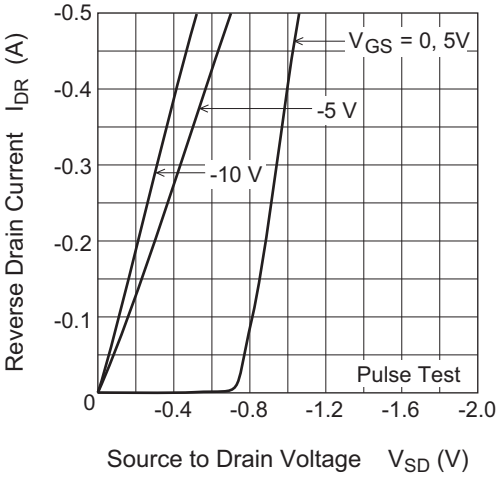
Typical Capacitance vs. Drain to Source Voltage



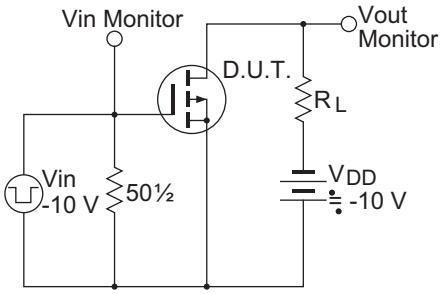
Switching Characteristics



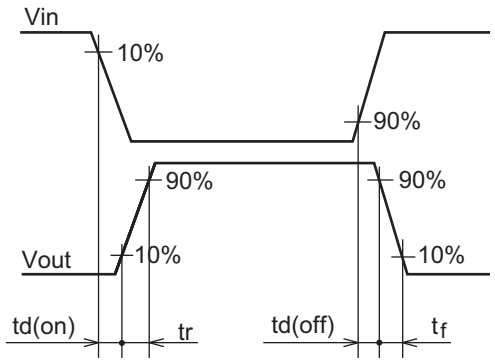
Reverse Drain Current vs. Source to Drain Voltage



Switching Time Test Circuit

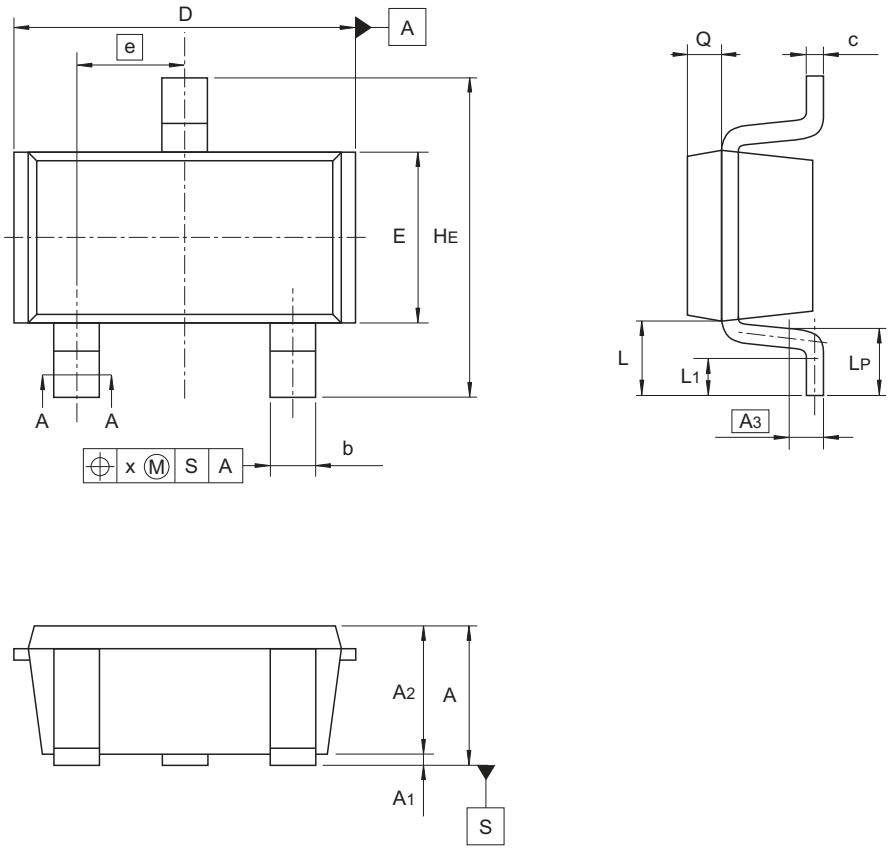


Waveforms



Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
SC-59A	PLSP0003ZB-A	MPAK(T) / MPAK(T)V	0.011



Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
A	1.0	—	1.3
A_1	0	—	0.1
A_2	1.0	1.1	1.2
$\boxed{A_3}$	—	0.25	—
b	0.35	0.4	0.5
c	0.1	0.16	0.26
D	2.7	—	3.1
E	1.35	1.5	1.65
$\boxed{e}$	—	0.95	—
H_E	2.2	2.8	3.0
L	0.35	—	0.75
L_1	0.15	—	0.55
L_P	0.25	—	0.65
x	—	—	0.05
Q	—	0.3	—

Ordering Information

Orderable Part Number	Quantity	Shipping Container
2SJ574BPTL-E	3000 pcs	ϕ178 mm reel, 12 mm Emboss taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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