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Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK1850 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} \leq 70 \text{ m}\Omega$ ($V_{GS} = 10 \text{ V}$, $I_D = 5.0 \text{ A}$)
 $R_{DS(on)} \leq 95 \text{ m}\Omega$ ($V_{GS} = 4 \text{ V}$, $I_D = 5.0 \text{ A}$)
- Low C_{iss} $C_{iss} = 1\,200 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diode

QUALITY GRADE

Standard

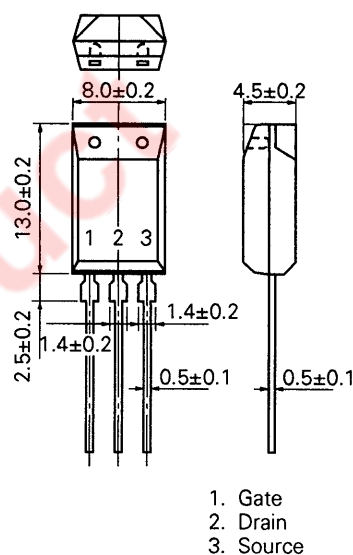
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25 \text{ }^\circ\text{C}$)

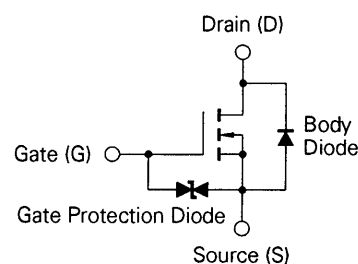
Drain to Source Voltage	V_{DSS}	60	V
Gate to Source Voltage	$V_{GSS(AC)}$	± 20	V
Gate to Source Voltage	$V_{GSS(DC)}$	+20, -10	V
Drain Current (DC)	$I_{D(DC)}$	± 10	A
Drain Current (pulse)	$I_{D(pulse)^*}$	± 40	A
Total Power Dissipation ($T_a = 25 \text{ }^\circ\text{C}$)	P_T	1.8	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

* $PW \leq 10 \text{ } \mu\text{s}$, Duty Cycle $\leq 1 \%$

PACKAGE DIMENSIONS (in millimeters)



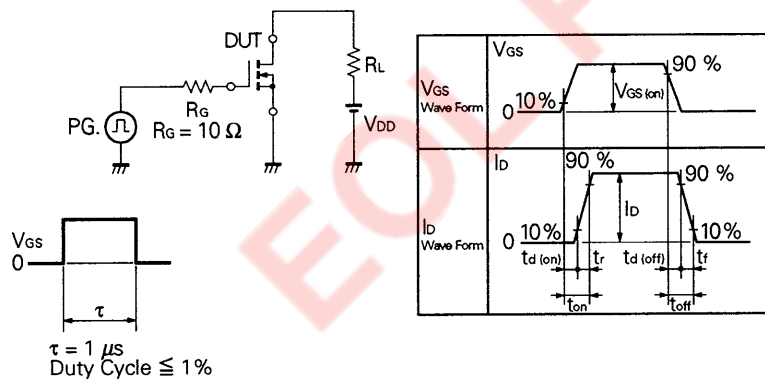
1. Gate
2. Drain
3. Source



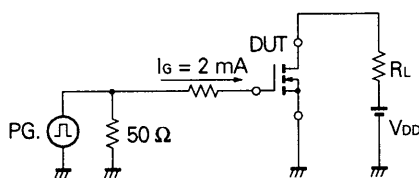
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R _{DS(on)}		55	70	mΩ	V _{GS} = 10 V, I _D = 5 A
Drain to Source On-state Resistance	R _{DS(on)}		80	95	mΩ	V _{GS} = 4 V, I _D = 5 A
Gate to Source Cutoff Voltage	V _{GS(off)}	1.0		2.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	5.5			S	V _{DS} = 10 V, I _D = 5 A
Drain Leakage Current	I _{DSS}			10	μA	V _{DS} = 60 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±20 V, V _{DS} = 0
Input Capacitance	C _{iss}		1 200		pF	V _{DS} = 10 V V _{GS} = 0 f = 1 MHz
Output Capacitance	C _{oss}		500		pF	
Reverse Transfer Capacitance	C _{rss}		120		pF	
Turn-On Delay Time	t _{d(on)}		20		ns	V _{GS(on)} = 10 V V _{DD} = 30 V
Rise Time	t _r		90		ns	
Turn-Off Delay Time	t _{d(off)}		250		ns	I _D = 5 A, R _G = 10 Ω R _L = 6.0 Ω
Fall Time	t _f		110		ns	
Total Gate Charge	Q _G		27		nC	V _{GS} = 10 V I _D = 10 A V _{DD} = 48 V
Gate to Source Charge	Q _{GS}		2.5		nC	
Gate to Drain Charge	Q _{GD}		8.0		nC	
Diode Forward Voltage	V _{F(S-D)}		1.0		V	V _{GS} = 0, I _D = 10 A
Reverse Recovery Time	t _{rr}		110		ns	I _F = 10 A, V _{GS} = 0
Reverse Recovery Charge	Q _{rr}		150		nC	di/dt = 50 A/μs

Test Circuit 1: Switching Time

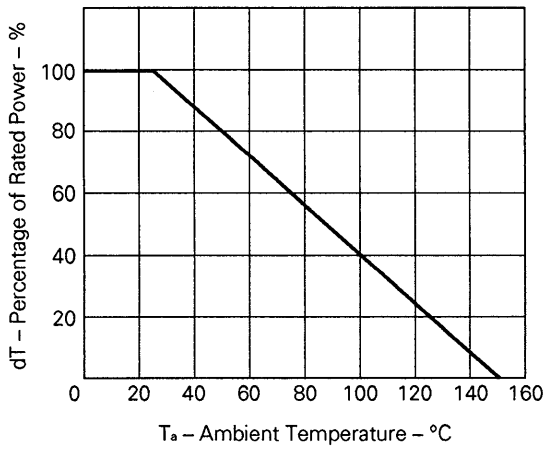


Test Circuit 2: Gate Charge

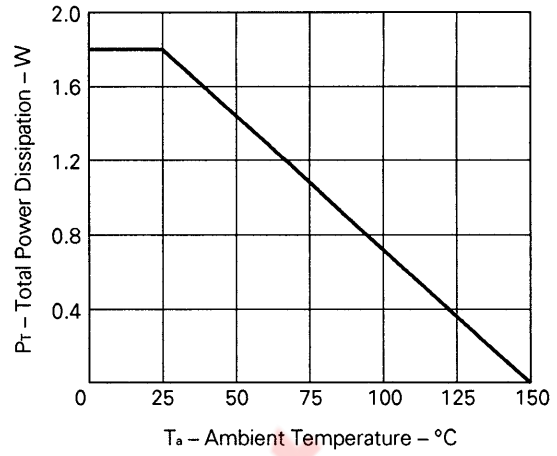


TYPICAL CHARACTERISTICS ($T_a = 25\text{ }^\circ\text{C}$)

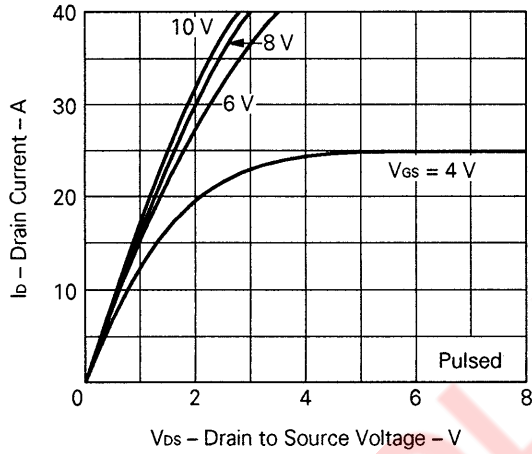
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



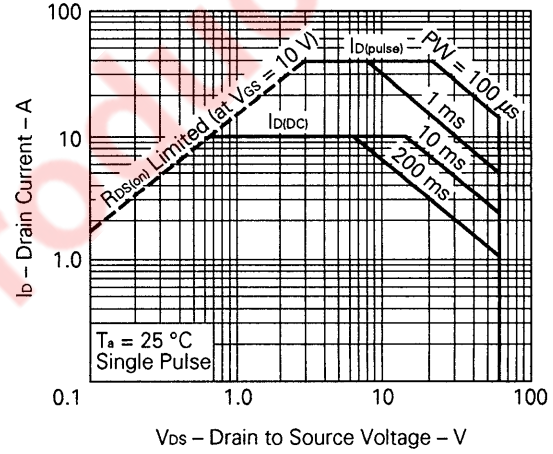
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



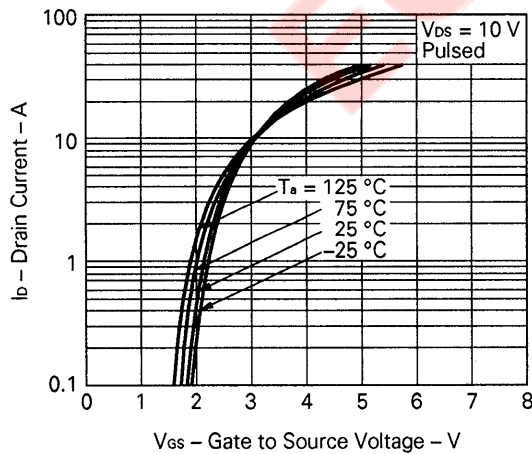
FORWARD BIAS SAFE OPERATING AREA



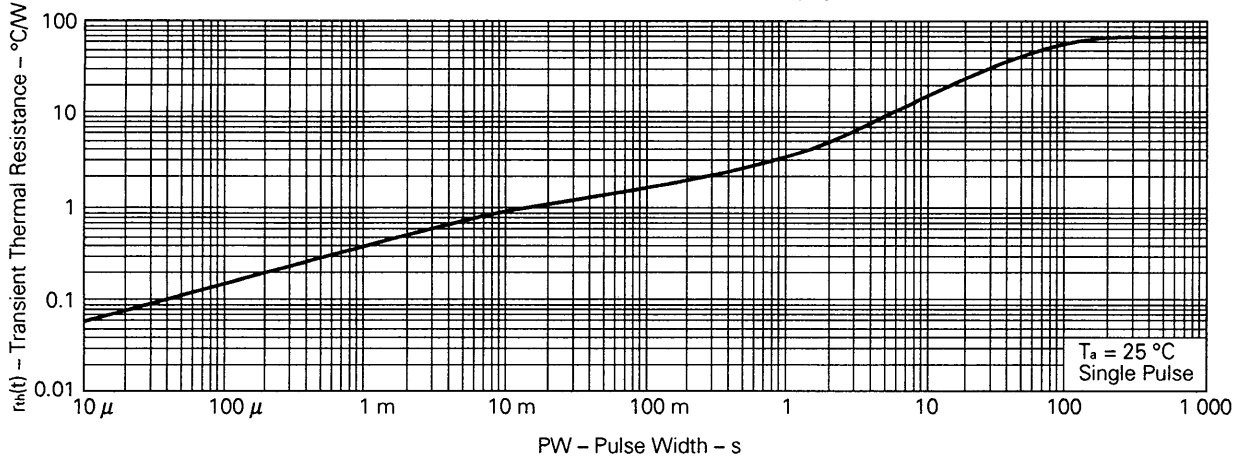
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



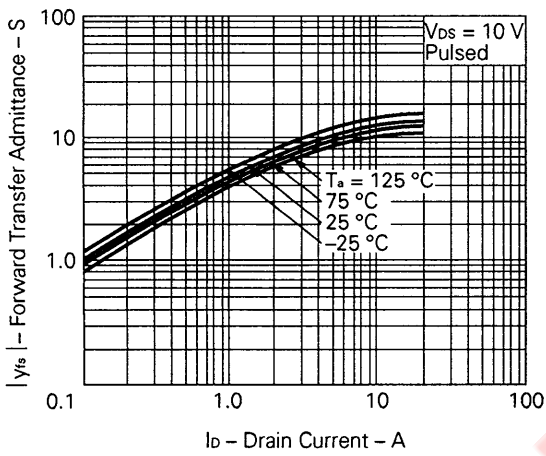
TRANSFER CHARACTERISTICS



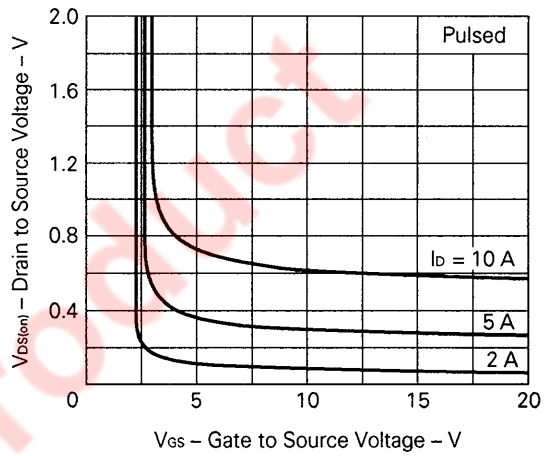
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



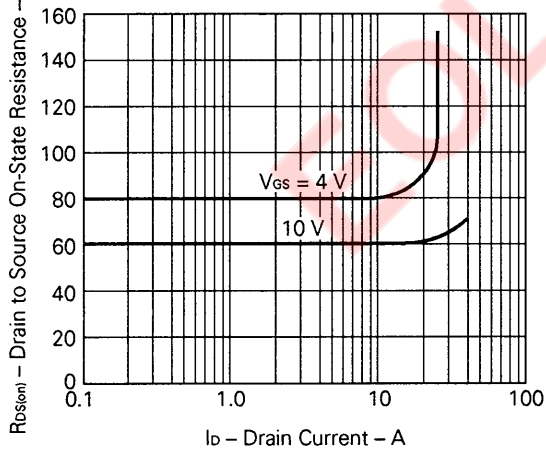
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



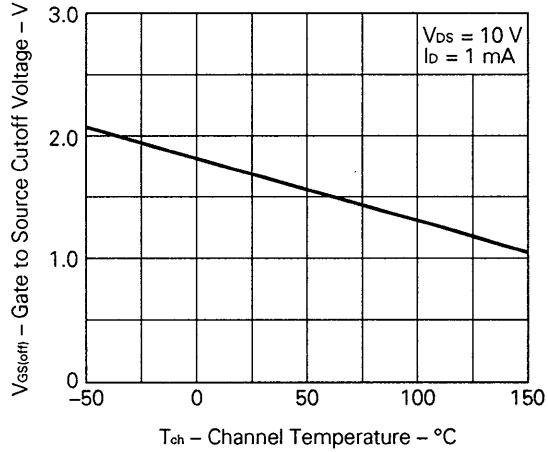
DRAIN TO SOURCE VOLTAGE vs. GATE TO SOURCE VOLTAGE

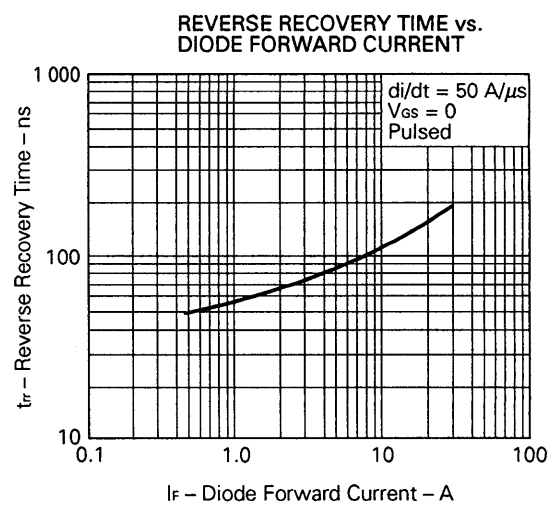
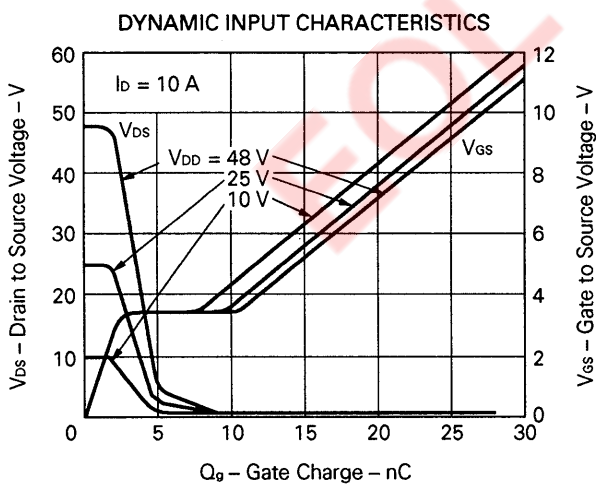
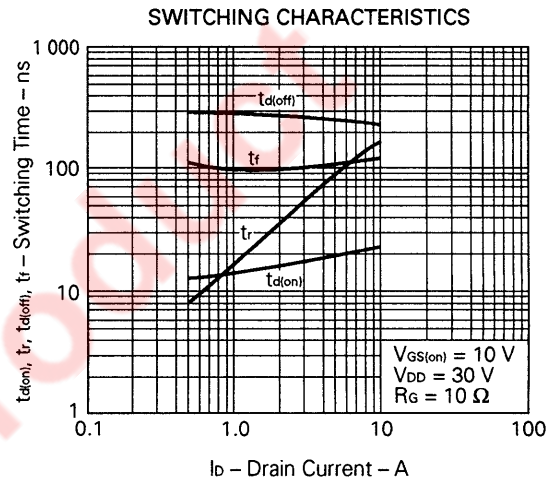
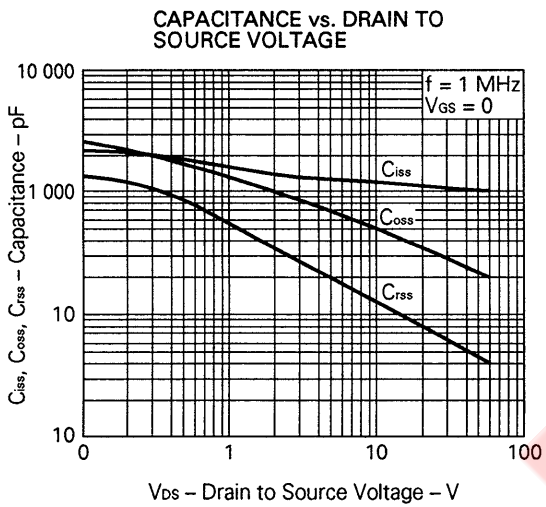
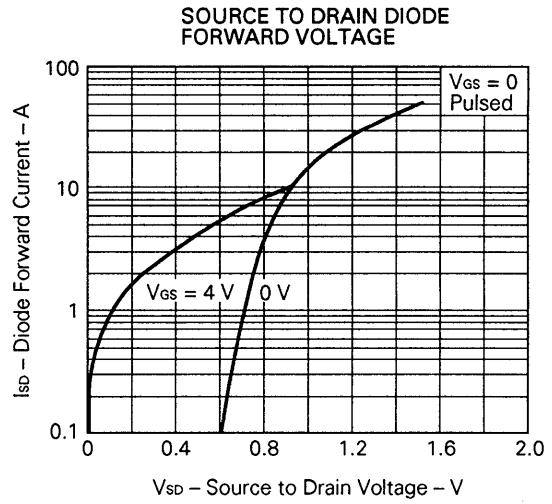
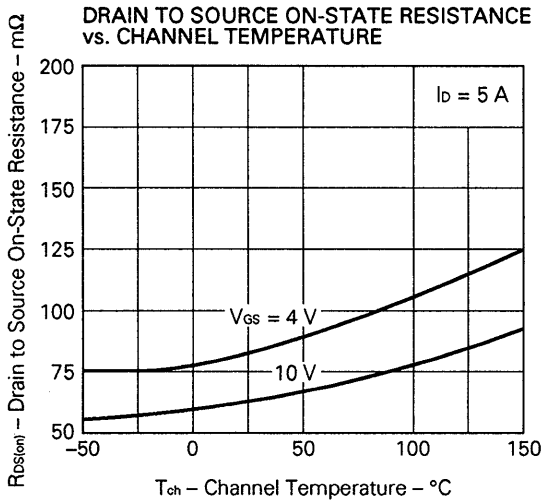


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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