

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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EOL announced Product

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N-CHANNEL MOSFET
FOR HIGH-SPEED SWITCHING

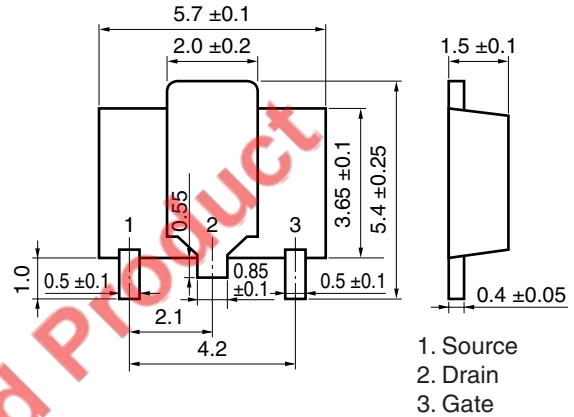
DESCRIPTION

The 2SK2053 is an N-channel vertical MOS FET. Because it can be driven by a voltage as low as 1.5 V and it is not necessary to consider a drive current, this FET is ideal as an actuator for low-current portable systems such as headphone stereos and video cameras.

FEATURES

- New package intermediate between small signal and power types
- Gate can be driven by 1.5 V
- Low ON resistance
 $R_{DS(on)} = 0.40 \Omega$ MAX. ($V_{GS} = 1.5 \text{ V}$, $I_D = 0.5 \text{ A}$)
 $R_{DS(on)} = 0.12 \Omega$ MAX. ($V_{GS} = 4.0 \text{ V}$, $I_D = 2.5 \text{ A}$)

PACKAGE DRAWING (Unit: mm)



ORDERING INFORMATION

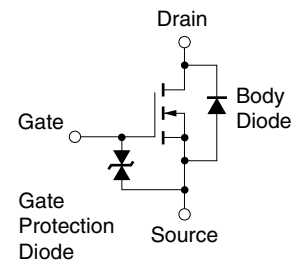
PART NUMBER	PACKAGE
2SK2053	SC-84 (MP-2)

Marking: NA1

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	16	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 7.0	V
Drain Current (DC)	$I_{D(DC)}$	± 5.0	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 10.0	A
Total Power Dissipation ^{Note2}	P_T	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

EQUIVALENT CIRCUIT



Notes 1. $PW \leq 10 \text{ ms}$, Duty Cycle $\leq 50\%$

2. Mounted on ceramic substrate of $7.5 \text{ cm}^2 \times 0.7 \text{ mm}$

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

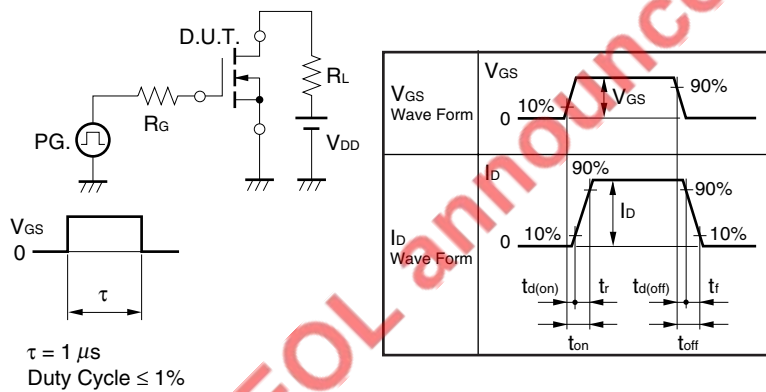
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

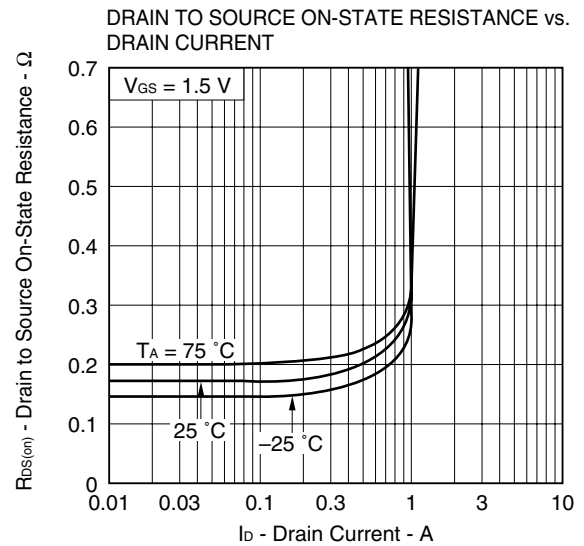
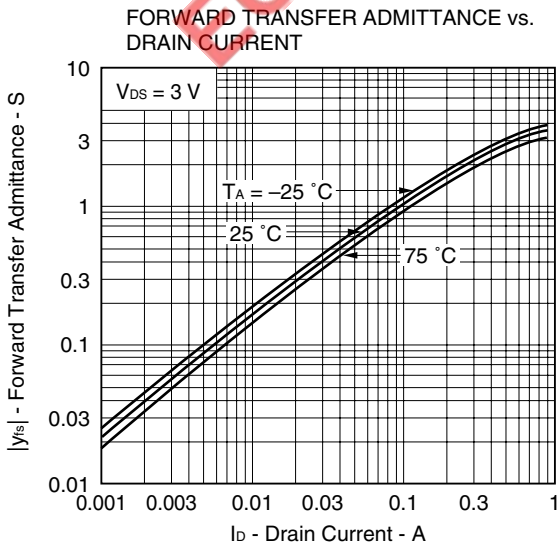
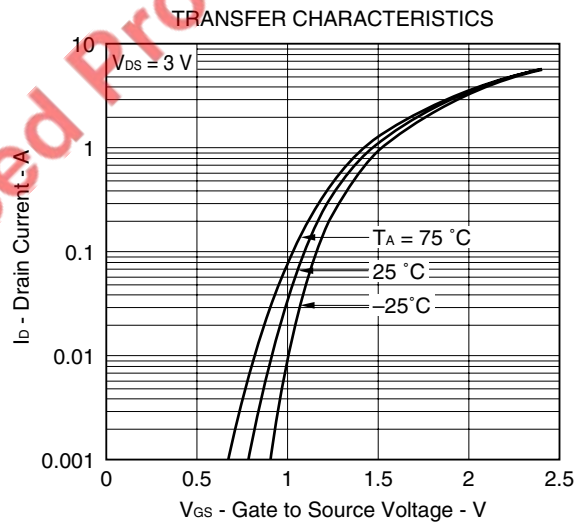
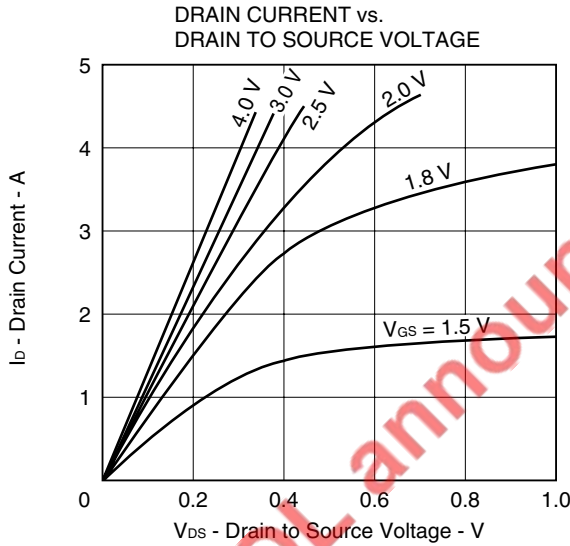
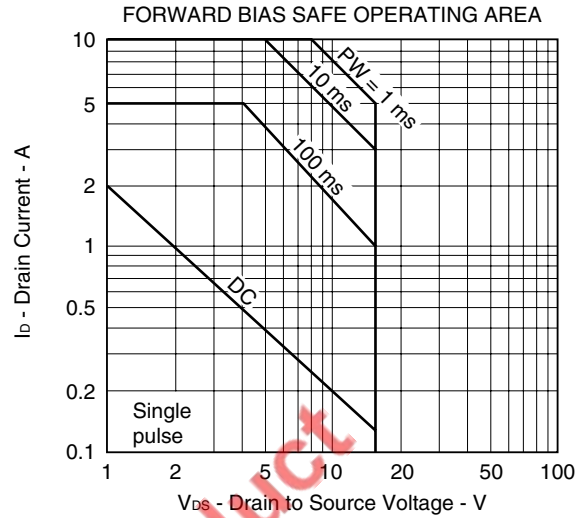
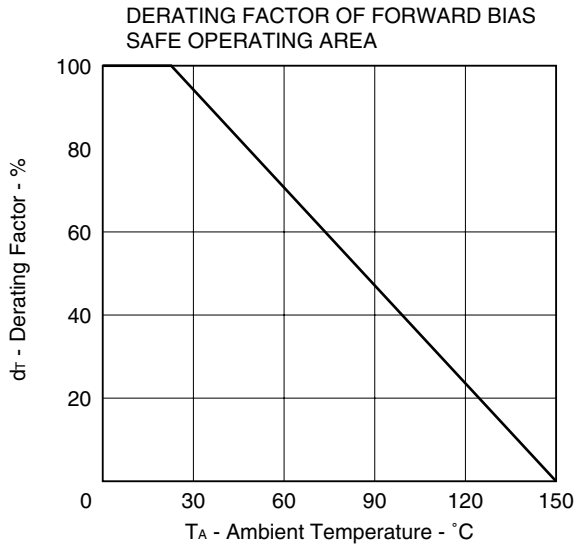
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 16 V, V _{GS} = 0 V			1.0	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±7.0 V, V _{DS} = 0 V			±3.0	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 3 V, I _D = 1 mA	0.5	0.8	1.1	V
Forward Transfer Admittance ^{Note}	y _{fs}	V _{DS} = 3 V, I _D = 2.5 A	4			S
Drain to Source On-state Resistance ^{Note}	R _{DS(on)1}	V _{GS} = 1.5 V, I _D = 0.5 A		0.19	0.40	Ω
	R _{DS(on)2}	V _{GS} = 2.5 V, I _D = 2.5 A		0.08	0.15	Ω
	R _{DS(on)3}	V _{GS} = 4.0 V, I _D = 2.5 A		0.06	0.12	Ω
Input Capacitance	C _{iss}	V _{DS} = 3 V		730		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		640		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		230		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 3 V, I _D = 2.5 A		85		ns
Rise Time	t _r	V _{GS} = 3 V		450		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		280		ns
Fall Time	t _f			310		ns

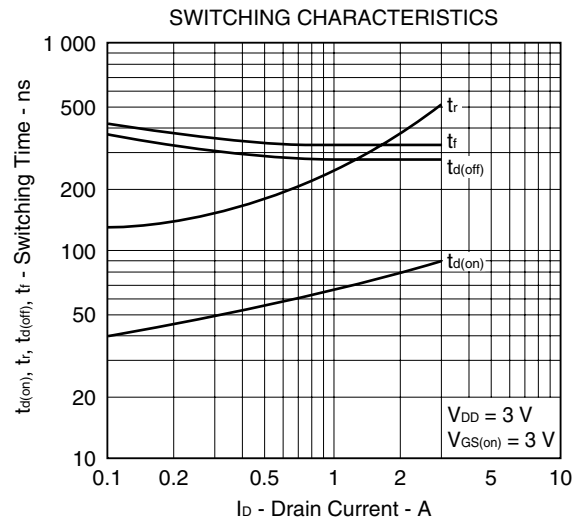
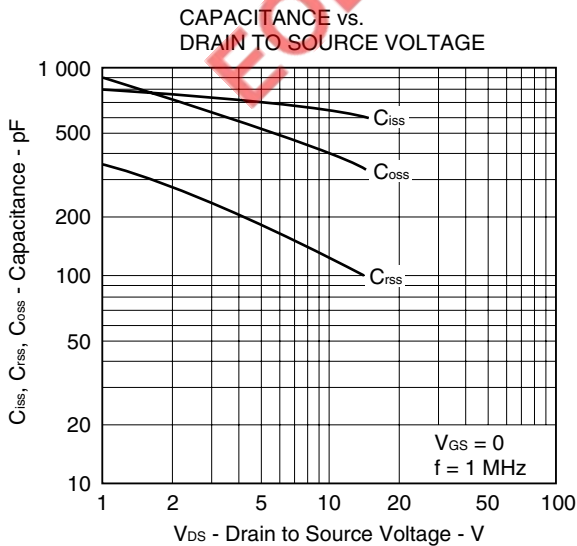
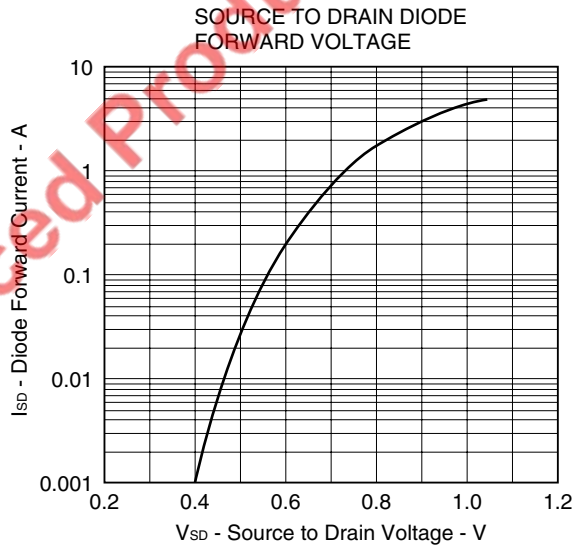
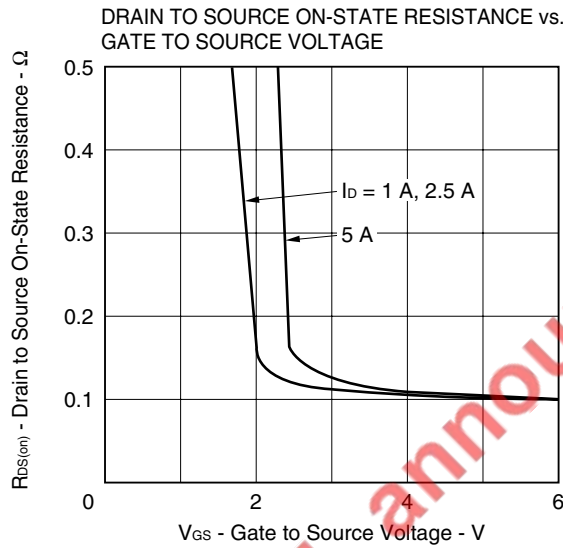
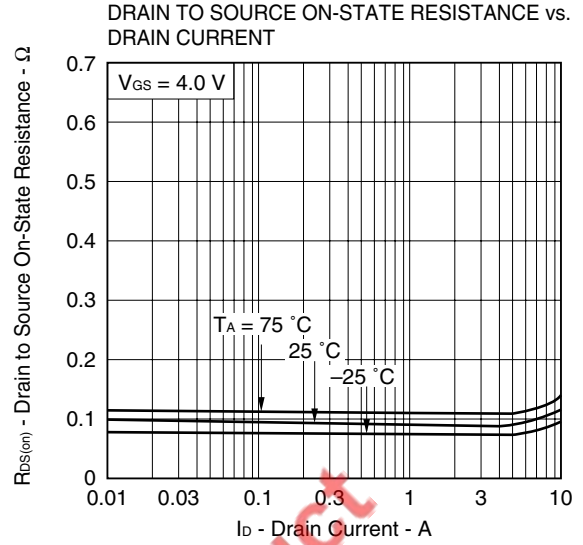
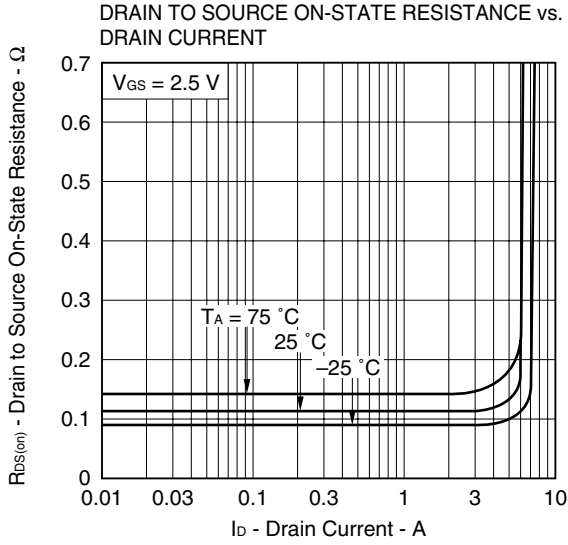
Note Pulsed

TEST CIRCUIT SWITCHING TIME



TYPICAL CHARACTERISTICS (T_A = 25°C)





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