

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Not recommended  
for new design

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**Phase-out/Discontinued**

**SWITCHING  
N-CHANNEL POWER MOS FET  
INDUSTRIAL USE**

**DESCRIPTION**

The 2SK2484 is N-Channel MOS Field Effect Transistor designed for high voltage switching applications.

**FEATURES**

- Low On-Resistance  
 $R_{DS(on)} = 2.8 \Omega$  ( $V_{GS} = 10 V, I_D = 3.0 A$ )
- Low  $C_{iss}$   $C_{iss} = 1\ 200\ pF$  TYP.
- High Avalanche Capability Ratings

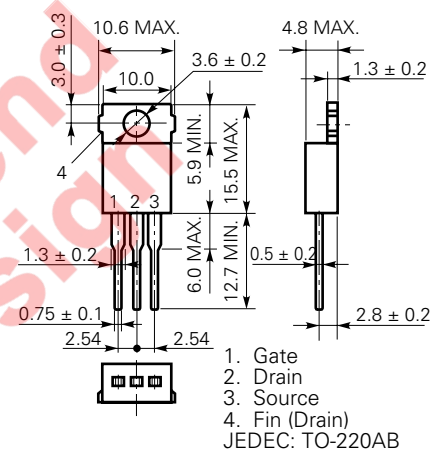
**ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\ ^\circ C$ )**

Drain to Source Voltage	$V_{DSS}$	900	V
Gate to Source Voltage	$V_{GSS}$	$\pm 30$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 5.0$	A
Drain Current (pulse)*	$I_{D(pulse)}$	$\pm 10$	A
Total Power Dissipation ( $T_c = 25\ ^\circ C$ )	$P_{T1}$	75	W
Total Power Dissipation ( $T_A = 25\ ^\circ C$ )	$P_{T2}$	1.5	W
Channel Temperature	$T_{ch}$	150	$^\circ C$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ C$
Single Avalanche Current**	$I_{AS}$	5.0	A
Single Avalanche Energy**	$E_{AS}$	75	mJ

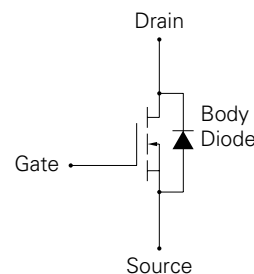
\*  $PW \leq 10\ \mu s, Duty\ Cycle \leq 1\ %$

\*\* Starting  $T_{ch} = 25\ ^\circ C, R_G = 25\ \Omega, V_{GS} = 20\ V \rightarrow 0$

**PACKAGE DIMENSIONS  
(in millimeters)**



**MP-25 (TO-220)**

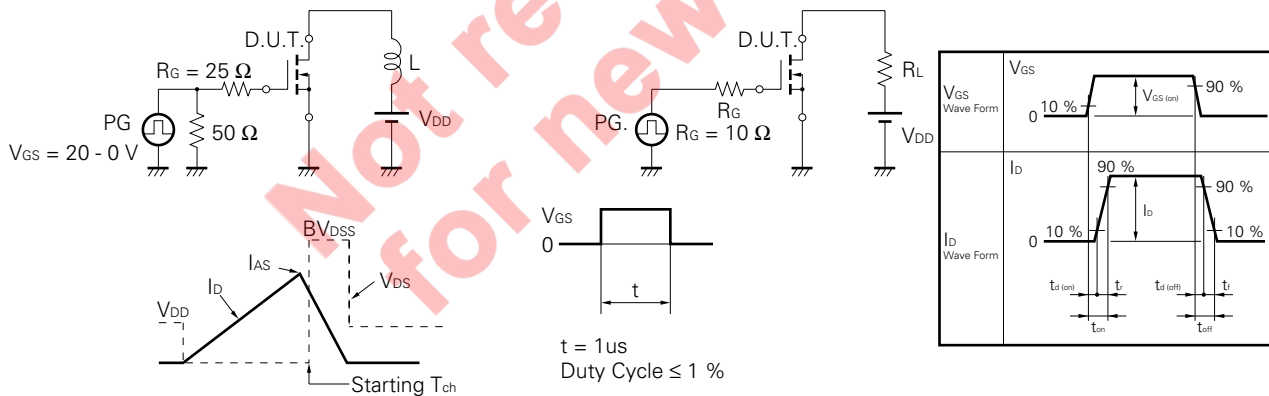


**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)**

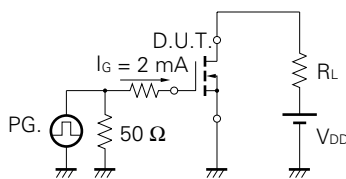
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-State Resistance	R <sub>DS(on)</sub>		2.2	2.8	Ω	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.0 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	2.5		3.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	2.0			S	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 3.0 A
Drain Leakage Current	I <sub>DSS</sub>			100	μA	V <sub>DS</sub> = V <sub>DSS</sub> , V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±100	nA	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		1 200		pF	V <sub>DS</sub> = 10 V
Output Capacitance	C <sub>oss</sub>		170		pF	V <sub>GS</sub> = 0
Reverse Transfer Capacitance	C <sub>rss</sub>		30		pF	f = 1 MHz
Turn-On Delay Time	t <sub>d(on)</sub>		20		ns	I <sub>D</sub> = 3.0 A
Rise Time	t <sub>r</sub>		10		ns	V <sub>GS</sub> = 10 V
Turn-Off Delay Time	t <sub>d(off)</sub>		70		ns	V <sub>DD</sub> = 150 V
Fall Time	t <sub>f</sub>		15		ns	R <sub>G</sub> = 10 Ω
Total Gate Charge	Q <sub>G</sub>		40		nC	I <sub>D</sub> = 5.0 A
Gate to Source Charge	Q <sub>GS</sub>		7		nC	V <sub>DD</sub> = 450 V
Gate to Drain Charge	Q <sub>GD</sub>		17		nC	V <sub>GS</sub> = 10 V
Body Diode Forward Voltage	V <sub>F(S-D)</sub>		1.0		V	I <sub>F</sub> = 5.0 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		670		ns	I <sub>F</sub> = 5.0 A, V <sub>GS</sub> = 0
Reverse Recovery Charge	Q <sub>rr</sub>		3.5		μC	di/dt = 50 A/μs

**Test Circuit 1 Avalanche Capability**

**Test Circuit 2 Switching Time**



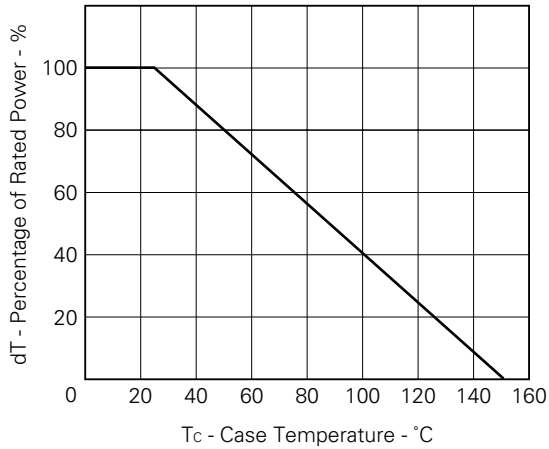
**Test Circuit 3 Gate Charge**



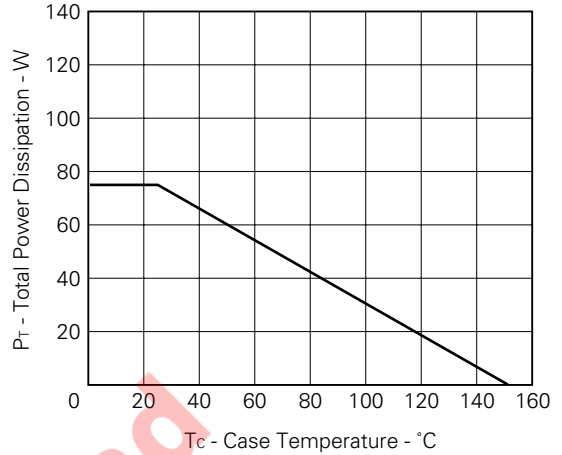
The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

**TYPICAL CHARACTERISTICS (TA = 25 °C)**

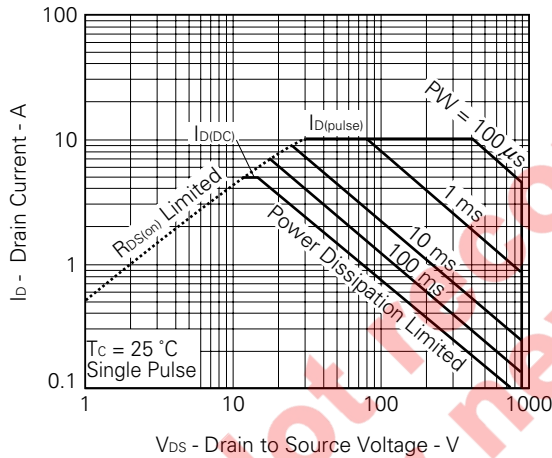
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



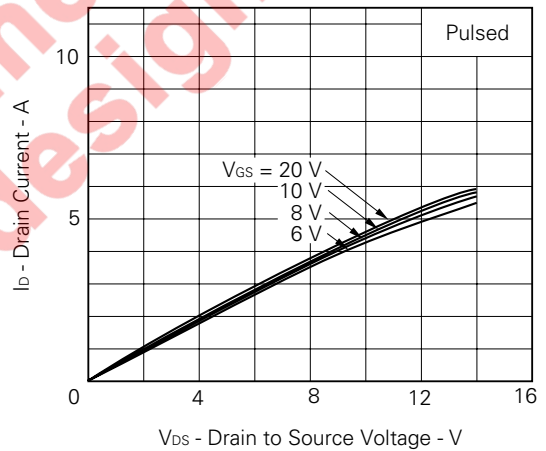
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



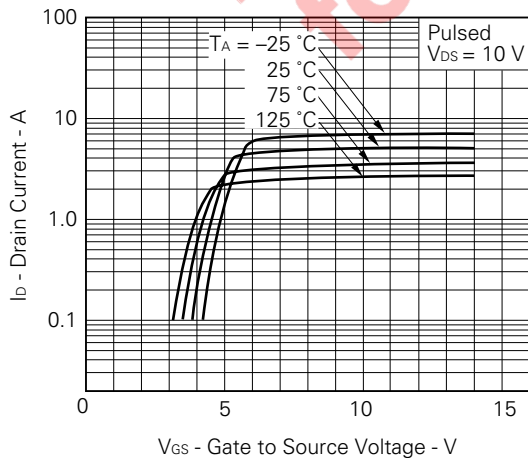
FORWARD BIAS SAFE OPERATING AREA



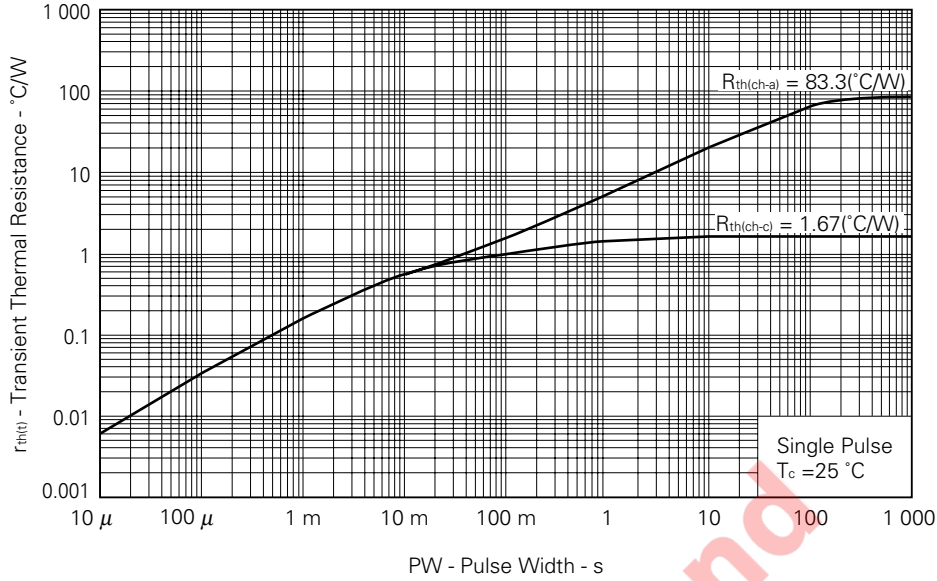
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



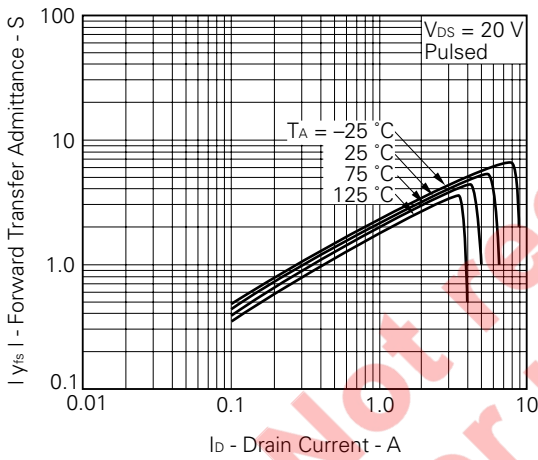
FORWARD TRANSFER CHARACTERISTICS



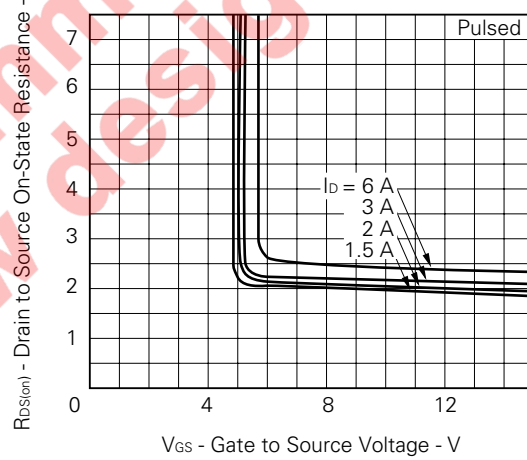
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



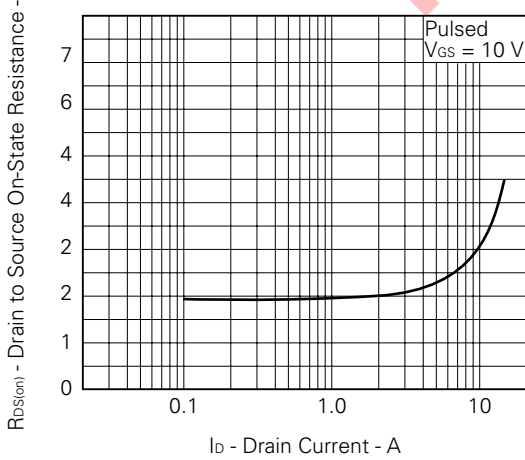
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



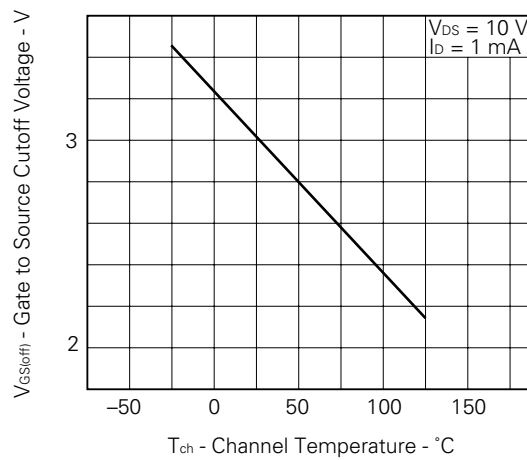
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

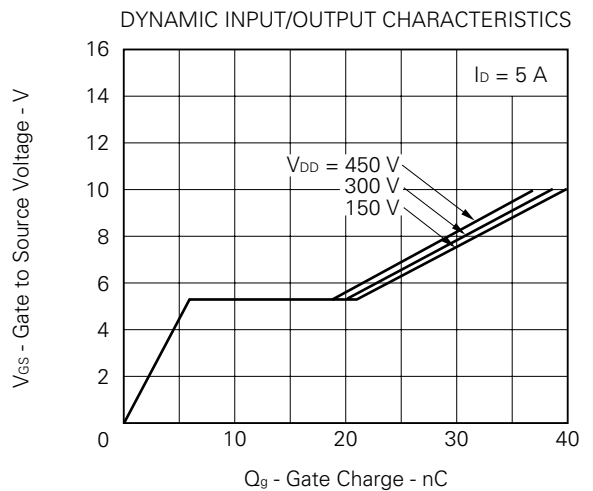
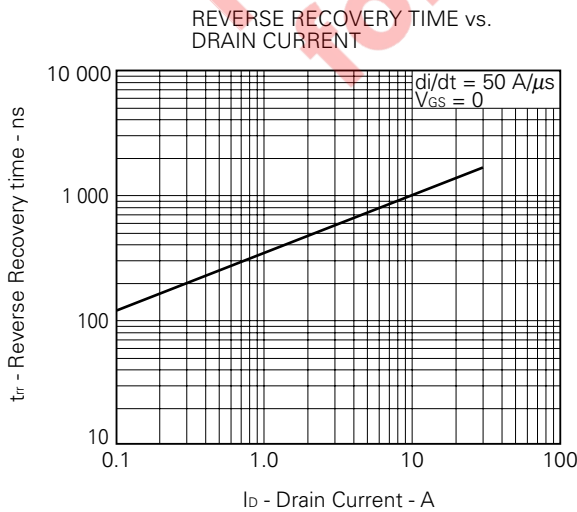
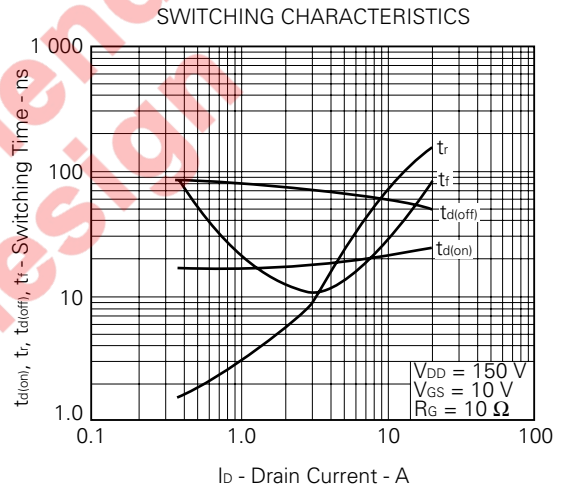
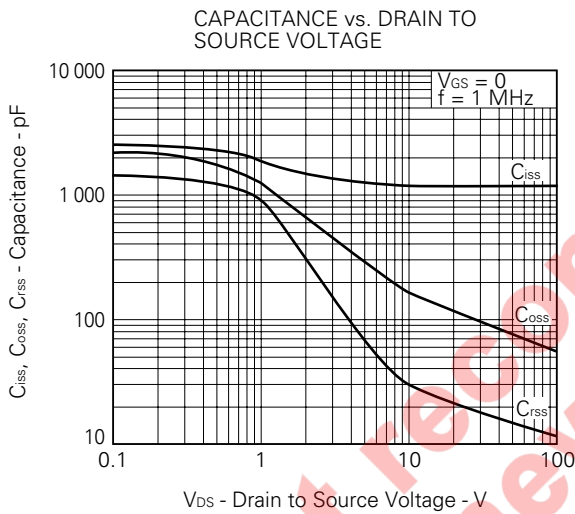
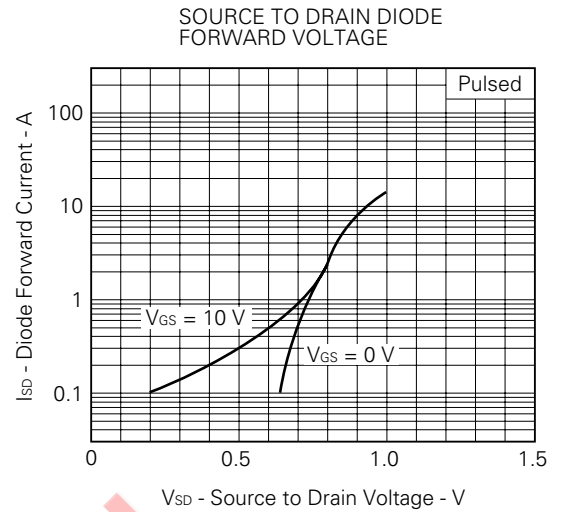
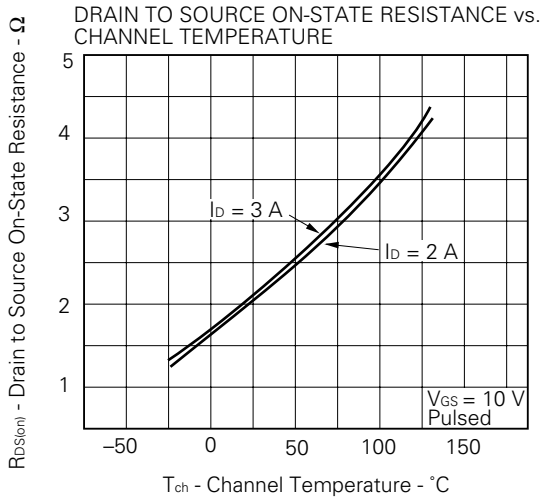


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

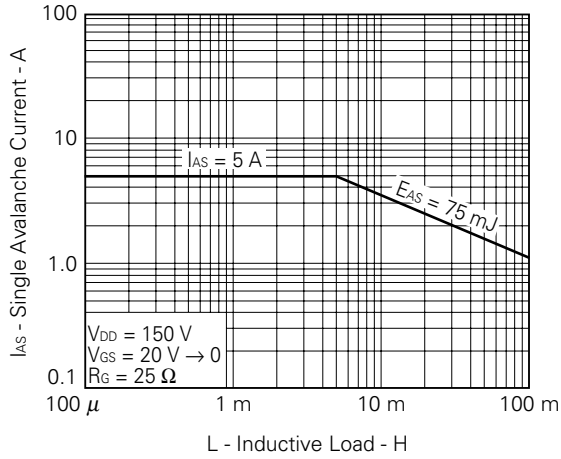


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

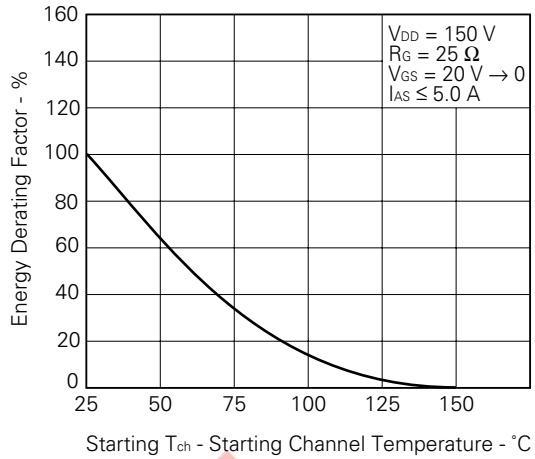




SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR



Not recommend  
for new design



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

**Not recommend  
for new design**

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