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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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2SK3150(L), 2SK3150(S)

Silicon N Channel MOS FET
High Speed Power Switching

REJ03G1075-0400
(Previous: ADE-208-750B)
Rev.4.00
Sep 07, 2005

Features

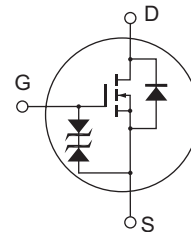
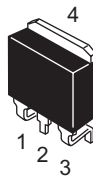
- Low on-resistance
 $R_{DS} = 45 \text{ m}\Omega$ typ.
- High speed switching
- 4 V gate drive device can be driven from 5 V source

Outline

RENESAS Package code: PRSS0004AE-A
(Package name: LDKPAK(L))



RENESAS Package code: PRSS0004AE-B
(Package name: LDKPAK(S)-(1))



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	20	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	80	A
Body-drain diode reverse drain current	I_{DR}	20	A
Avalanche current	I_{AP} ^{Note3}	20	A
Avalanche energy	E_{AR} ^{Note3}	40	mJ
Channel dissipation	P_{ch} ^{Note2}	50	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. $PW \leq 10\mu s$, duty cycle $\leq 1\%$
 2. Value at $T_c = 25^\circ C$
 3. Value at $T_{ch} = 25^\circ C$, $R_g \geq 50 \Omega$

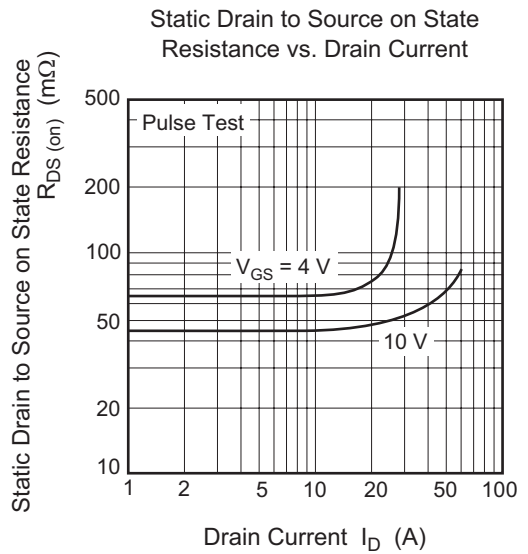
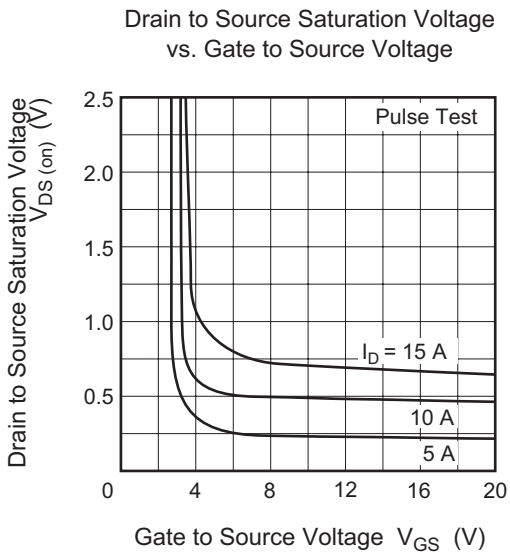
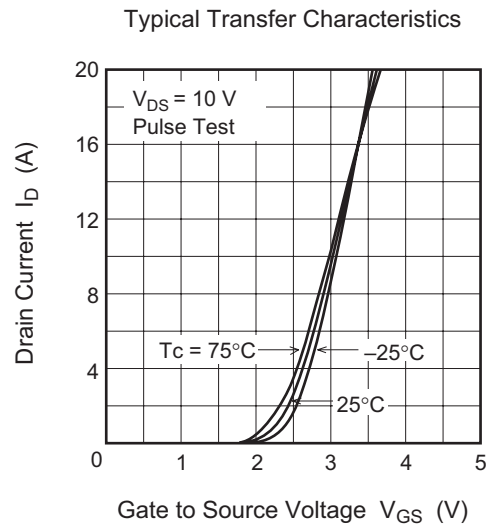
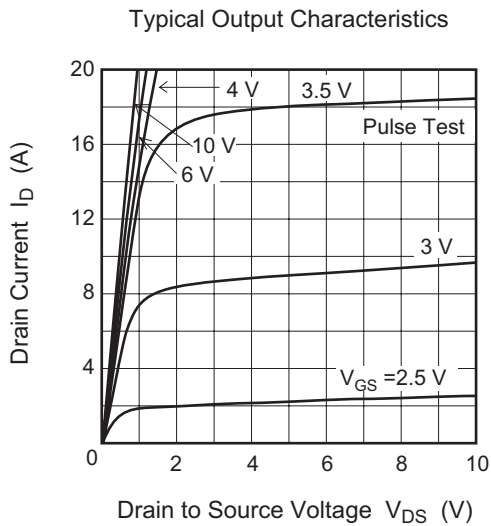
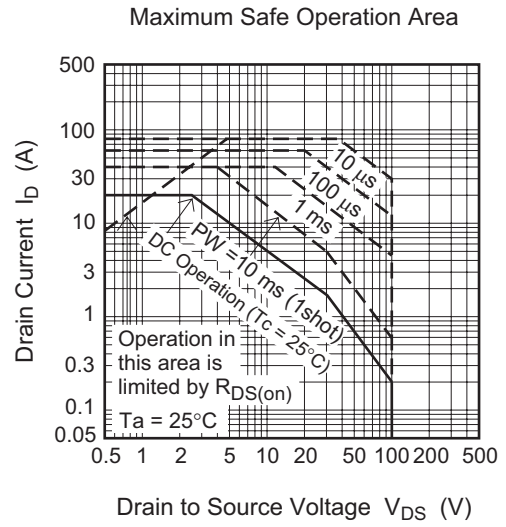
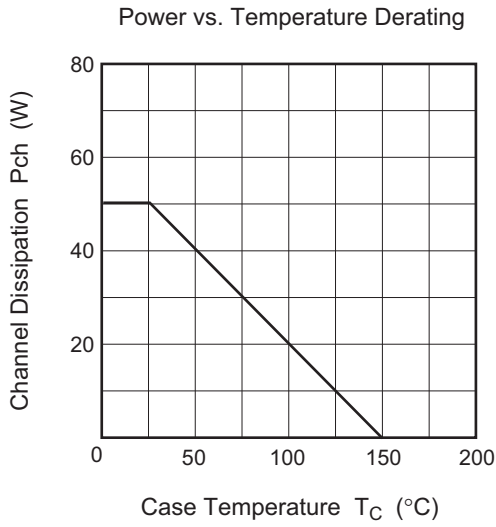
Electrical Characteristics

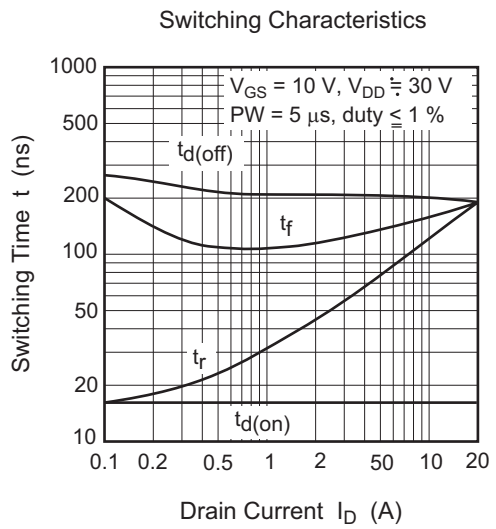
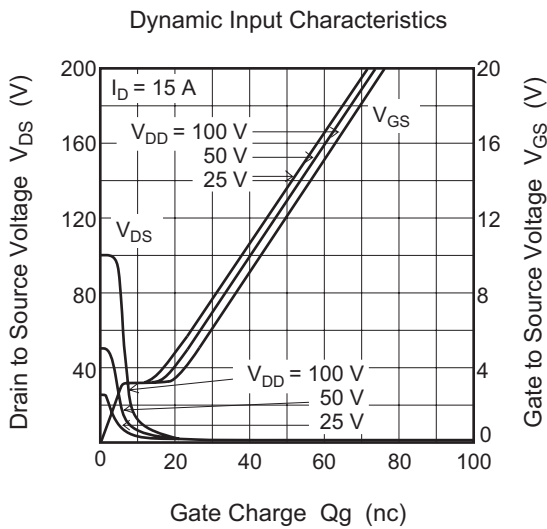
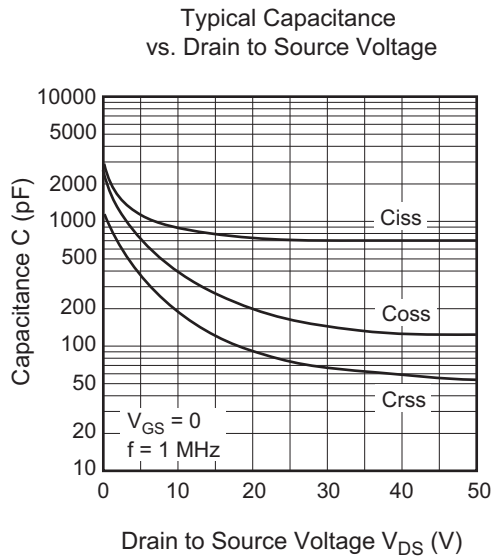
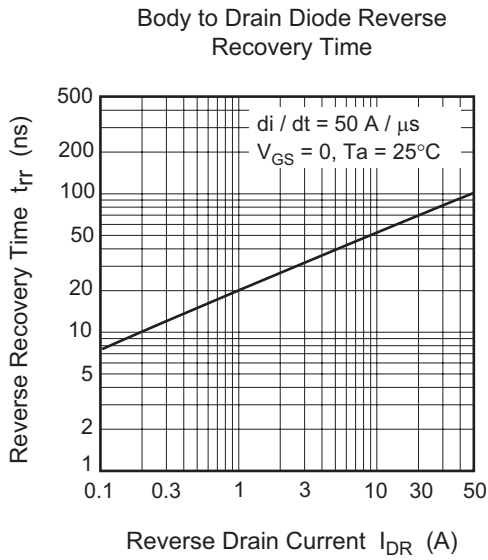
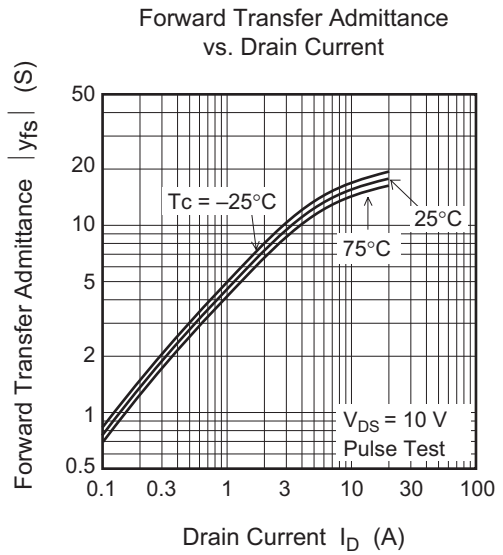
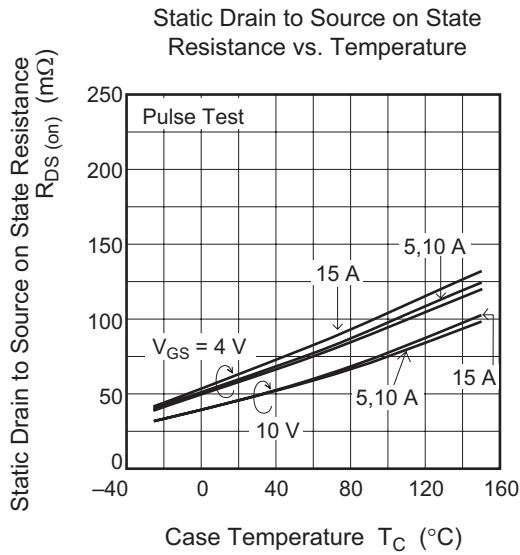
(Ta = 25°C)

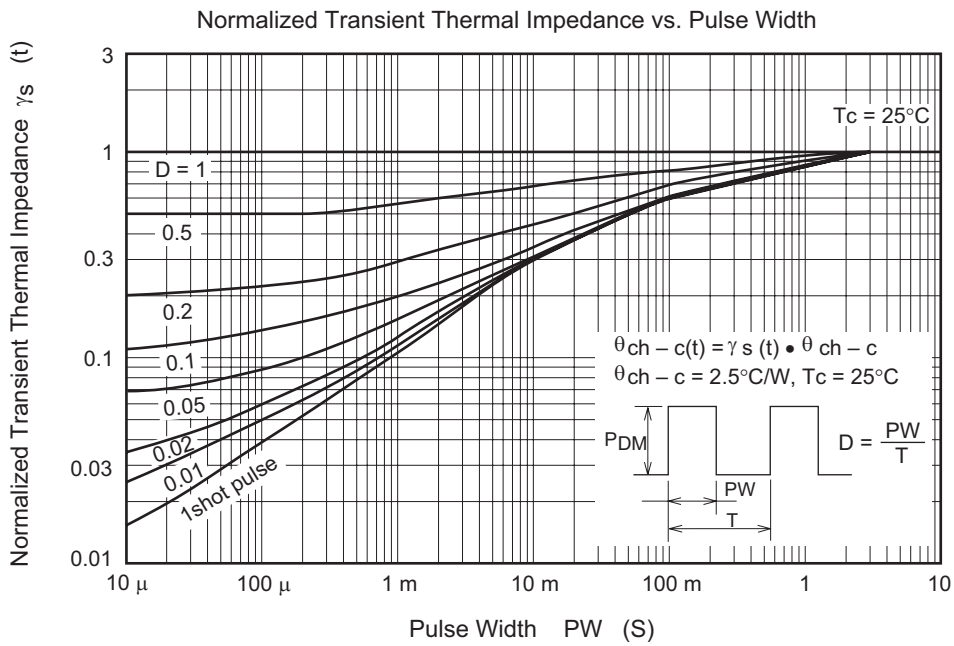
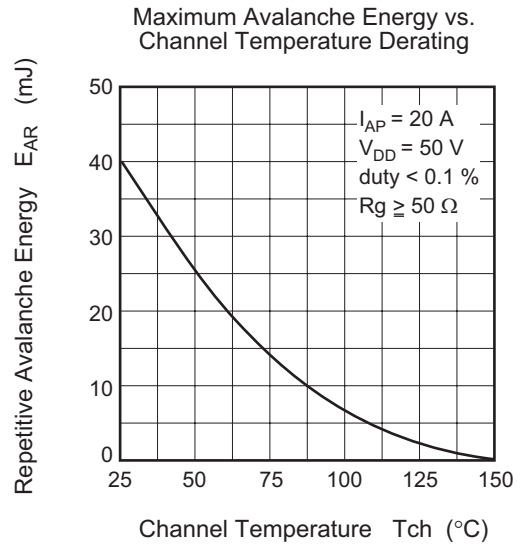
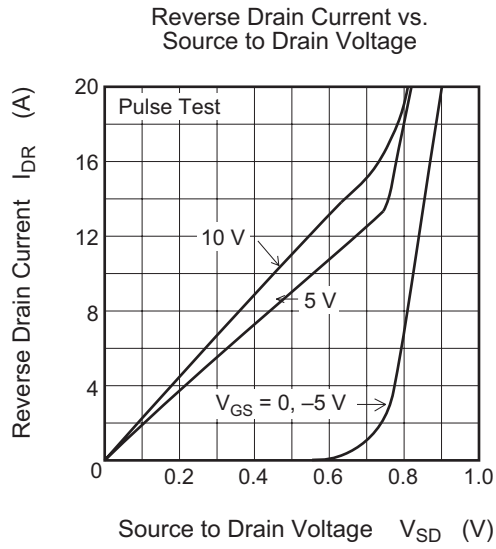
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100 \mu A$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 100 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$I_D = 1 \text{ mA}$, $V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	45	60	mΩ	$I_D = 10 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	65	85	mΩ	$I_D = 10 \text{ A}$, $V_{GS} = 4 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	8.5	14	—	S	$I_D = 10 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	900	—	pF	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	400	—	pF	
Reverse transfer capacitance	C_{rss}	—	210	—	pF	
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	$I_D = 10 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_L = 3 \Omega$
Rise time	t_r	—	120	—	ns	
Turn-off delay time	$t_{d(off)}$	—	200	—	ns	
Fall time	t_f	—	150	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.9	—	V	$I_F = 20 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	90	—	ns	$I_F = 20 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 50 \text{ A}/\mu s$

Note: 4. Pulse test

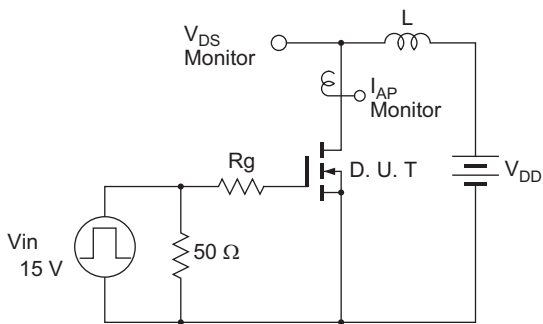
Main Characteristics



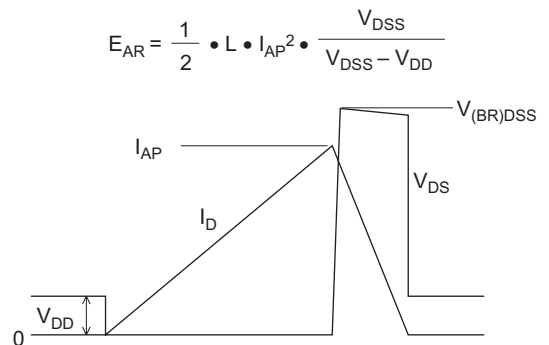


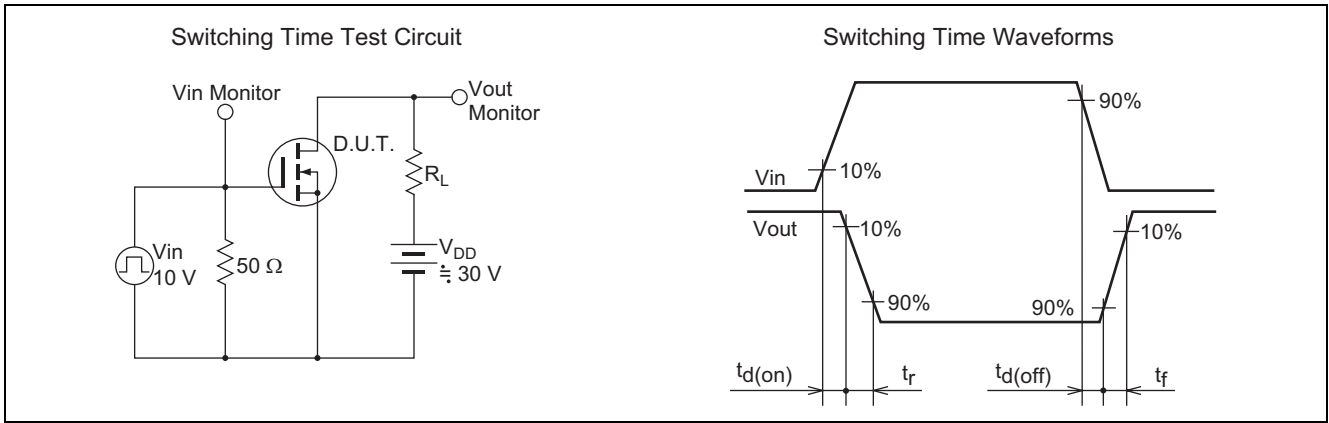


Avalanche Test Circuit

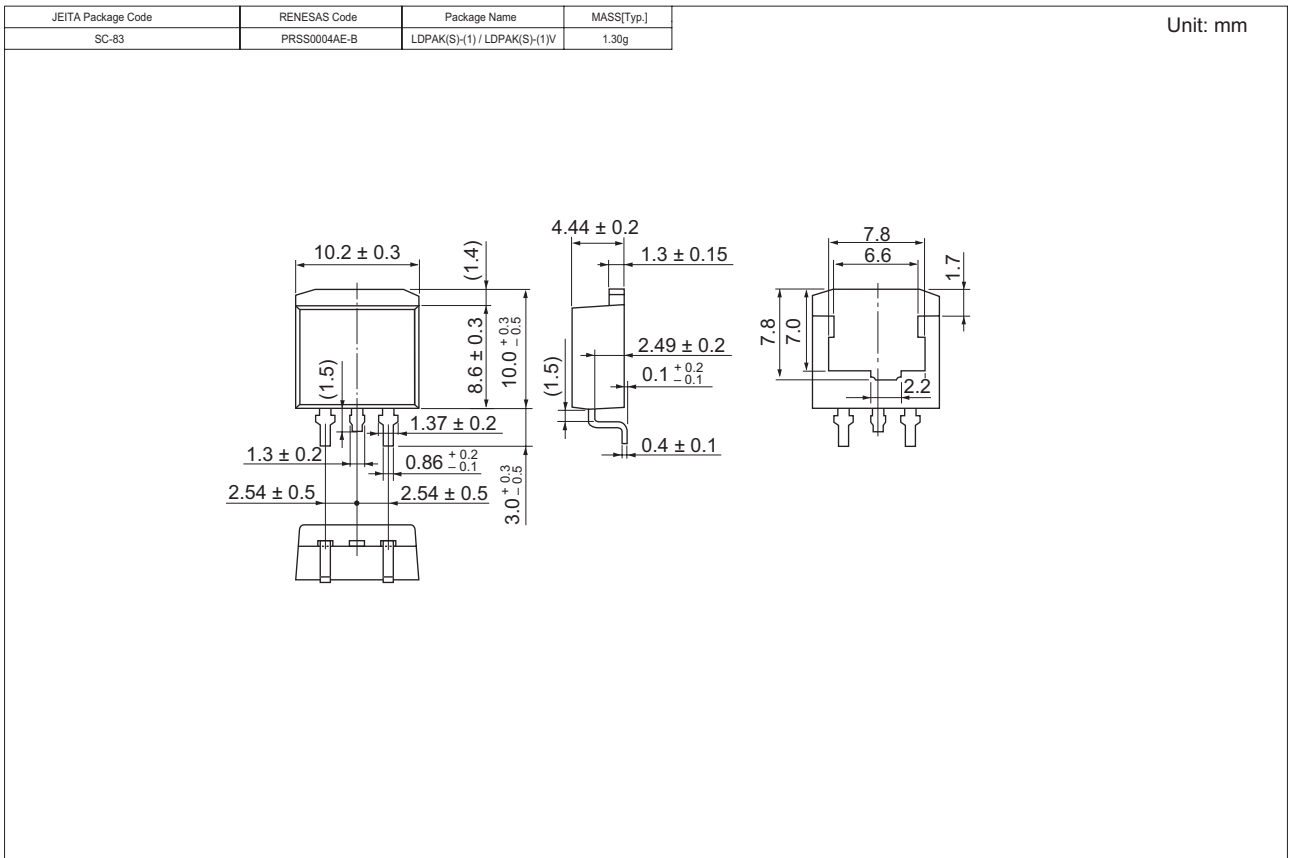
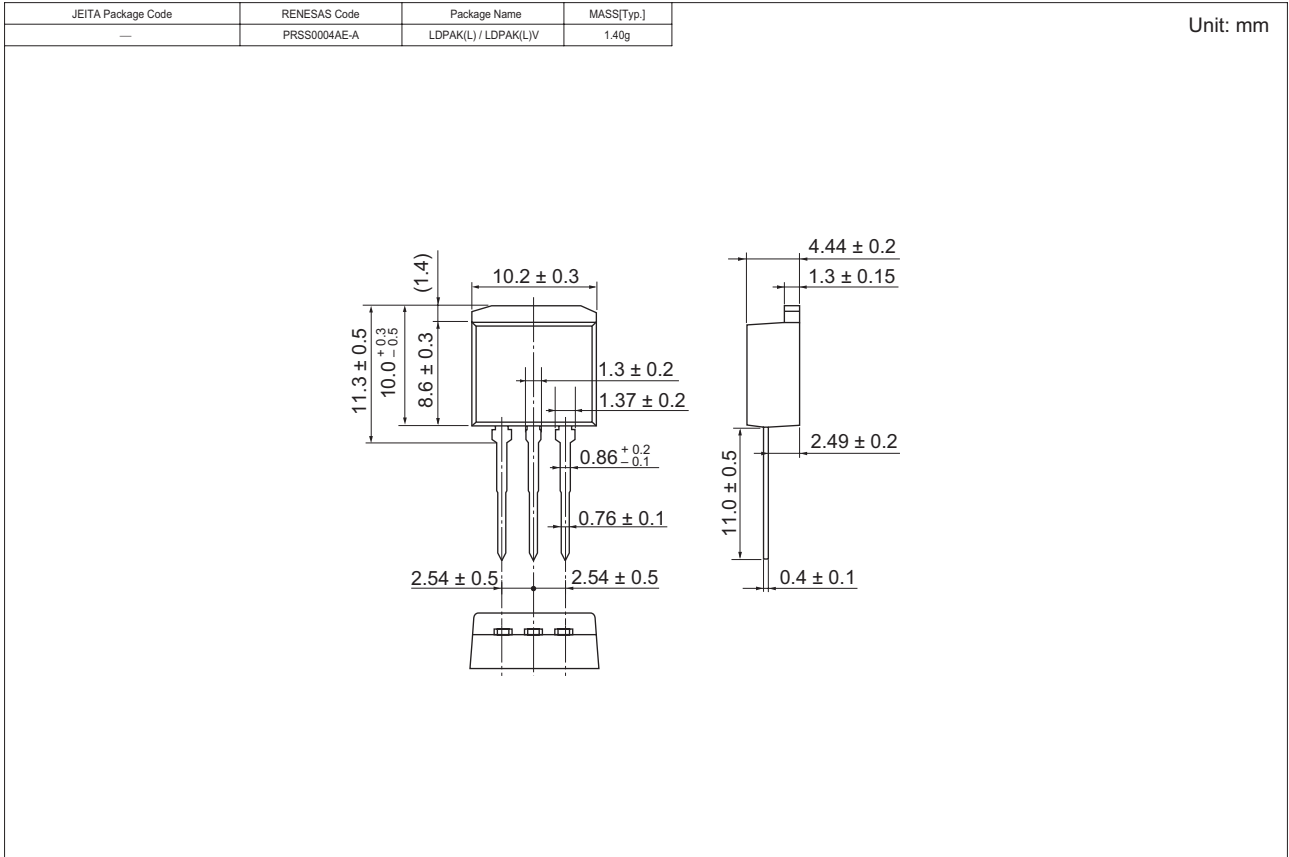


Avalanche Waveform





Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
2SK3150L-E	500 pcs	Box (Sack)
2SK3150STL-E	1000 pcs	Taping

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