To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS FIELD EFFECT TRANSISTOR

Phase-out/Discontinued

2SK3304

SWITCHING
N-CHANNEL POWER MOS FET

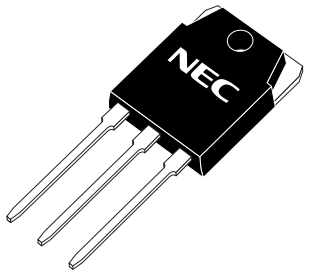
DESCRIPTION

The 2SK3304 is N-Channel MOS FET device that features a Low gate charge and excellent switching characteristics, and designed for high voltage applications such as switching power supply.

FEATURES

- Low gate charge :
  Q_G = 44 nC TYP. (V_{DD} = 450 V, V_{GS} = 10 V, I_D = 7.0 A)
- Gate voltage rating : ±30 V
- Low on-state resistance :
  $R_{DS(on)}$ = 2.0 Ω MAX. (V_{GS} = 10 V, I_D = 4.0 A)
- Avalanche capability ratings

(TO-3P)



ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3304	TO-3P

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage	V_{DSS}	900	V
Gate to Source Voltage	$V_{GSS(AC)}$	±30	V
Drain Current (DC)	$I_{D(DC)}$	±7	A
Drain Current (Pulse) Note1	$I_{D(pulse)}$	±21	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	130	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	3.0	W
Storage Temperature	T_{stg}	−55 to +150	°C
Single Avalanche Current Note2	I_{AS}	7	A
Single Avalanche Energy Note2	E_{AS}	147	mJ

Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1 %

2. Starting T_{ch} = 25°C, V_{DD} = 150 V, R_G = 25 Ω, V_{GS} = 20 → 0 V

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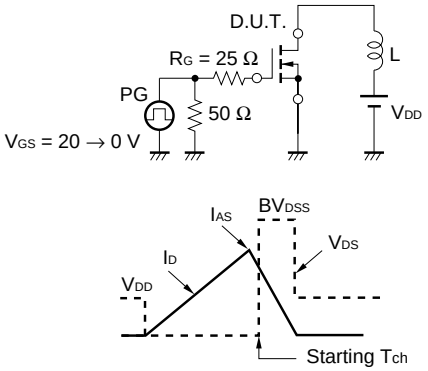
Date Published November 2006 NS CP(K)
Printed in Japan

The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

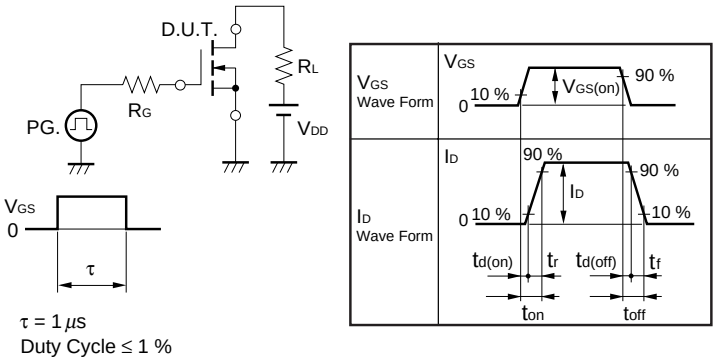
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Leakage Current	I_{DSS}	V_{DS} = 900 V, V_{GS} = 0 V			100	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1.0 mA	2.5		3.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 20 V, I_D = 4.0 A	2.5	4.7		S
Drain to Source On-state Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 4.0 A		1.6	2.0	Ω
Input Capacitance	C_{iss}	V_{DS} = 10 V		1300		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		240		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		55		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 150 V		20		ns
Rise Time	t_r	I_D = 4.0 A		44		ns
Turn-off Delay Time	$t_{d(off)}$	V_{GS} = 10 V		73		ns
Fall Time	t_f	R_G = 10 Ω, R_L ≅ 36 Ω		45		ns
Total Gate Charge	Q_G	V_{DD} = 450 V		44		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		6		nC
Gate to Drain Charge	Q_{GD}	I_D = 7.0 A		28		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 7.0 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 7.0 A, V_{GS} = 0 V		2.4		μs
Reverse Recovery Charge	Q_{rr}	di/dt = 50 A/μs		13.5		μC

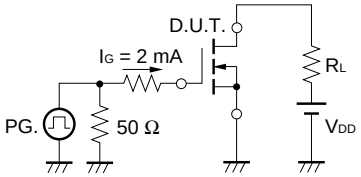
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

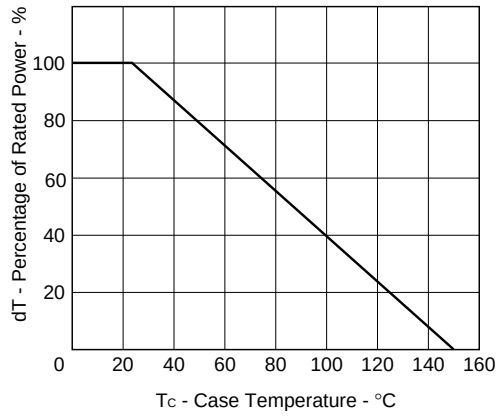


TEST CIRCUIT 3 GATE CHARGE

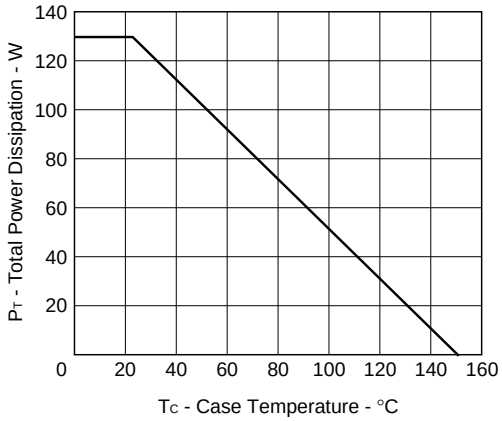


TYPICAL CHARACTERISTICS (T_A = 25°C)

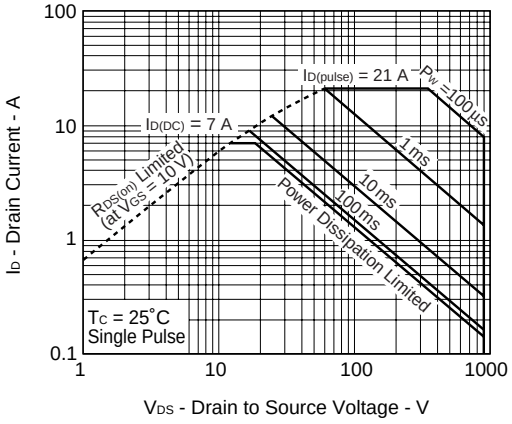
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



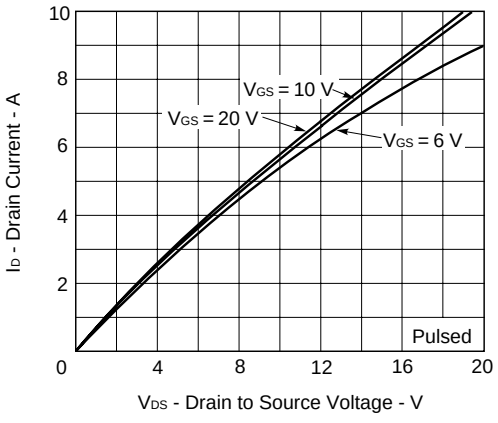
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



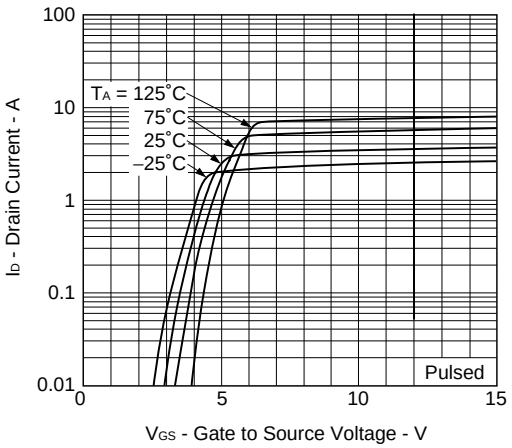
FORWARD BIAS SAFE OPERATING AREA



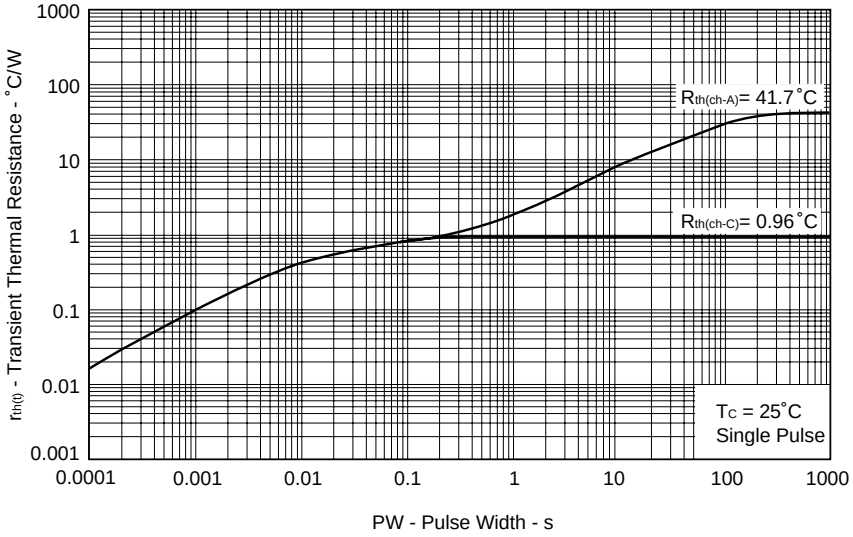
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



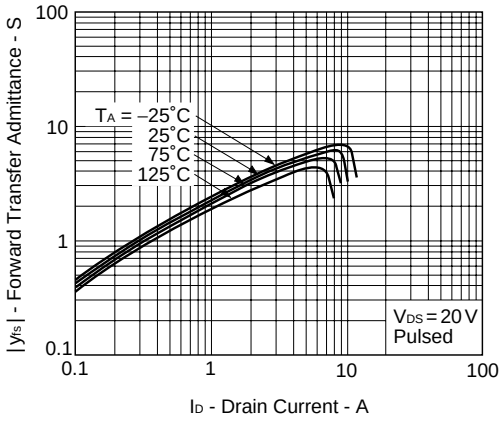
FORWARD TRANSFER CHARACTERISTICS



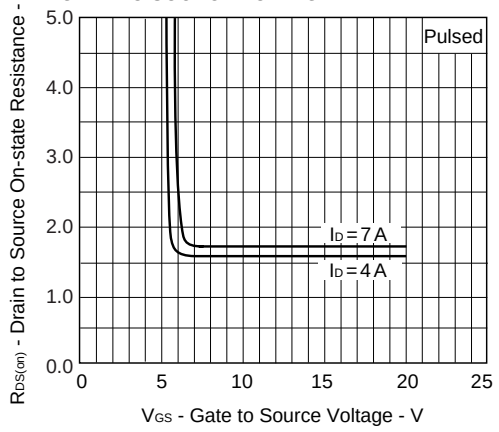
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



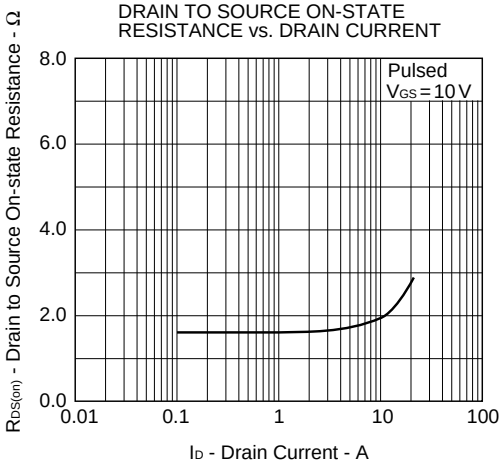
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



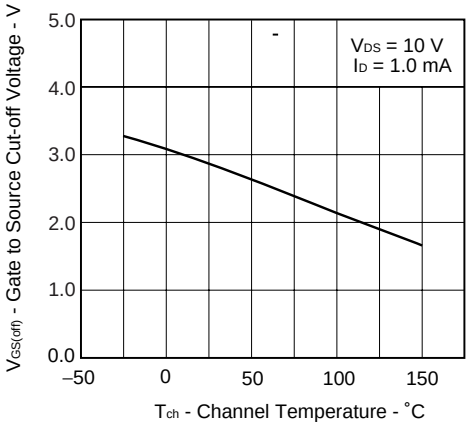
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



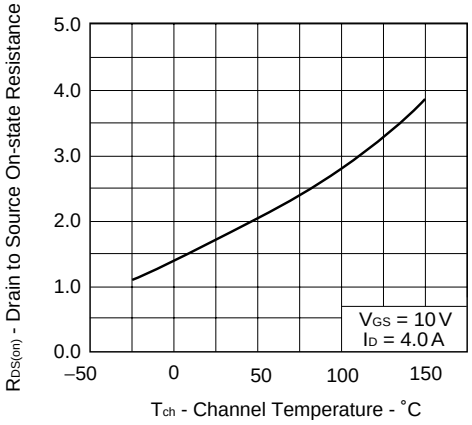
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



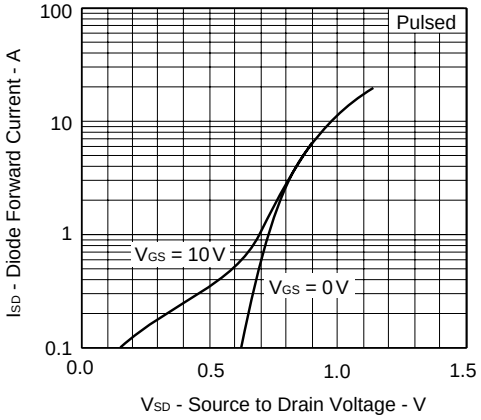
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



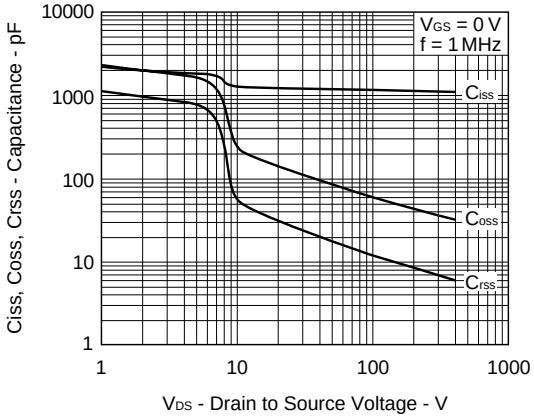
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



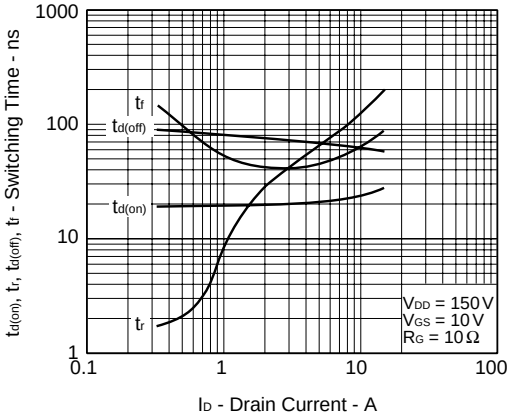
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



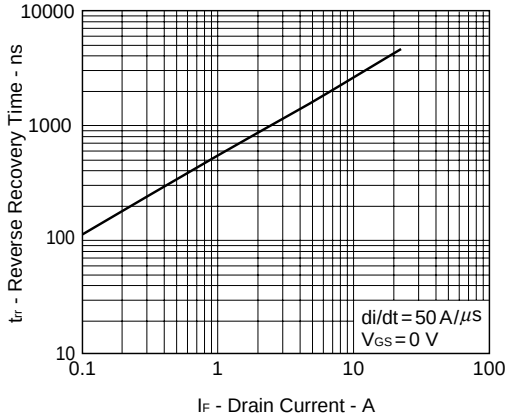
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



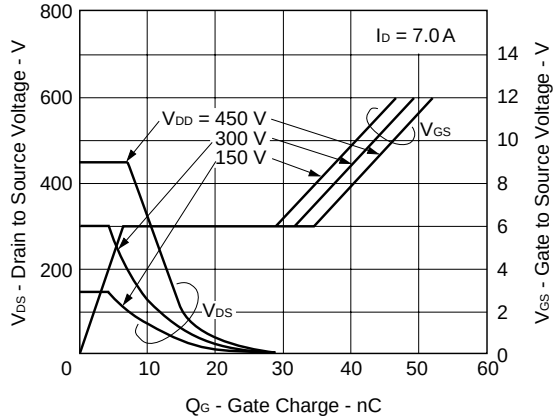
SWITCHING CHARACTERISTICS



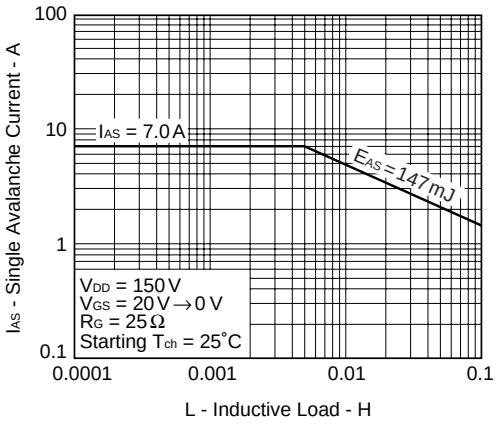
REVERSE RECOVERY TIME vs. DRAIN CURRENT



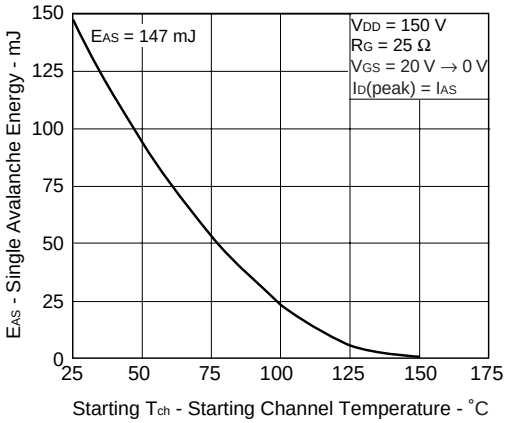
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD

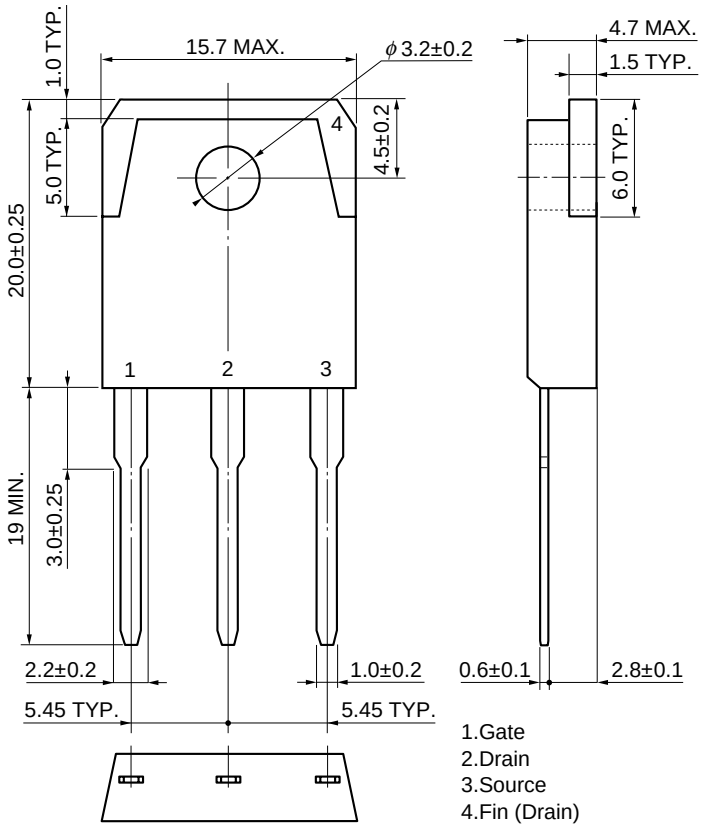


SINGLE AVALANCHE ENERGY vs
STARTING CHANNEL TEMPERATURE

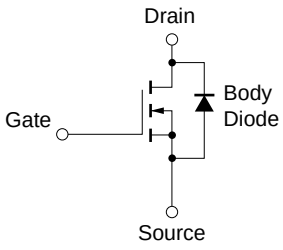


PACKAGE DRAWING (Unit : mm)

<R> **TO-3P (MP-88)**



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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